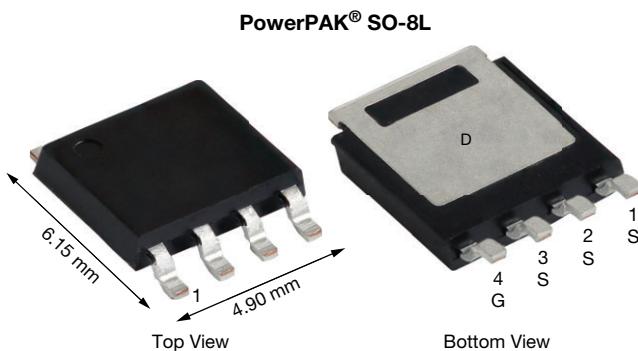


Automotive N-Channel 80 V (D-S) 175 °C MOSFET

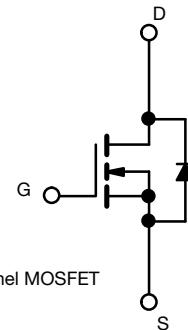


FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Material categorization:
for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE



PRODUCT SUMMARY	
V_{DS} (V)	80
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.015
I_D (A)	60
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK SO-8L
Lead (Pb)-free and halogen-free	SQJ186EP (for detailed order number please see www.vishay.com/doc?79776)

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	80	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current	I_D	60	A
$T_C = 125$ °C		35	
Continuous source current (diode conduction) ^a	I_S	122	
Pulsed drain current ^b	I_{DM}	112	
Single pulse avalanche current	I_{AS}	22.5	mJ
Single pulse avalanche energy		25	
Maximum power dissipation	P_D	135	W
$T_C = 125$ °C		45	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^d		260	

THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	R_{thJA}	42	°C/W
Junction-to-case (drain)		1.1	

Notes

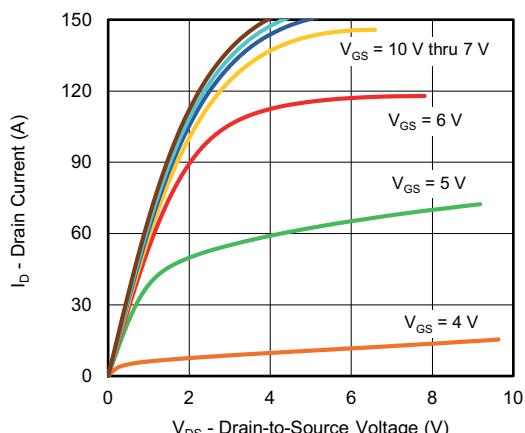
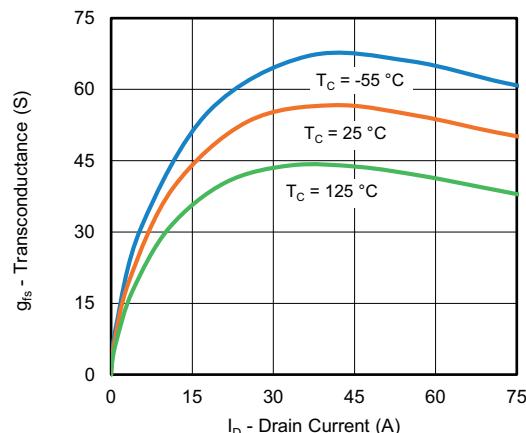
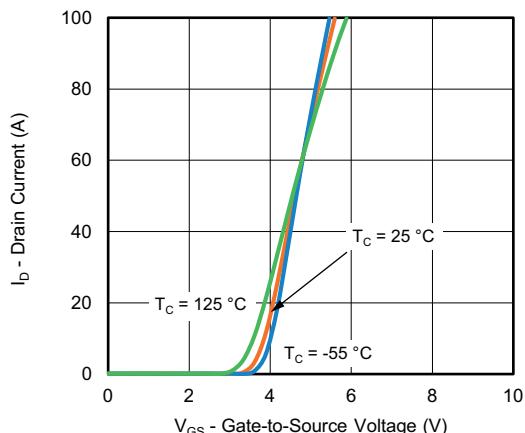
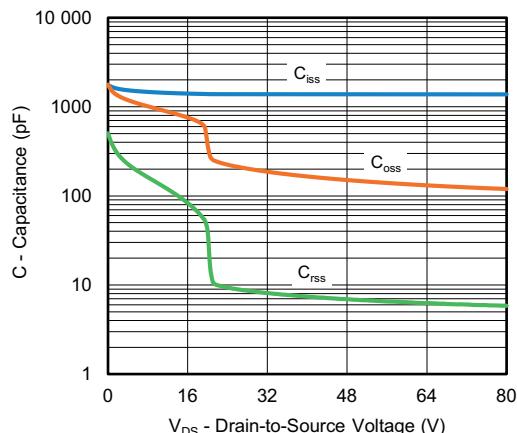
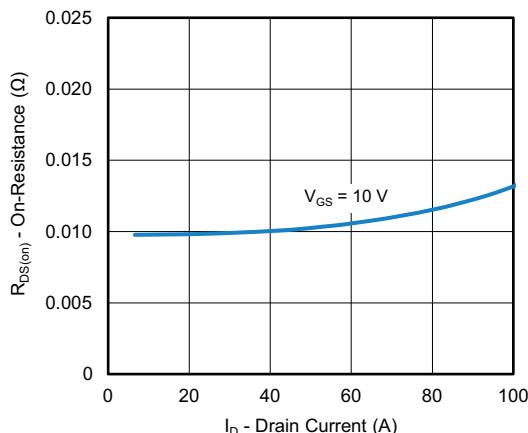
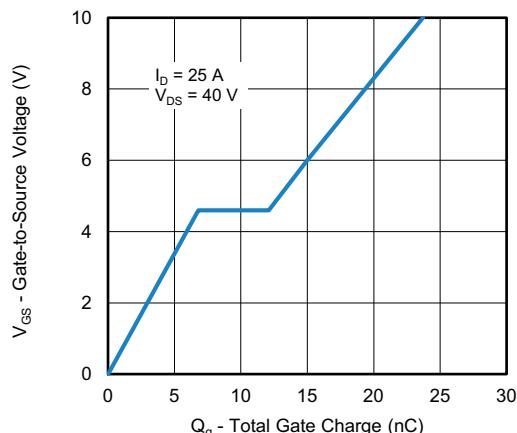
- Package limited
- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

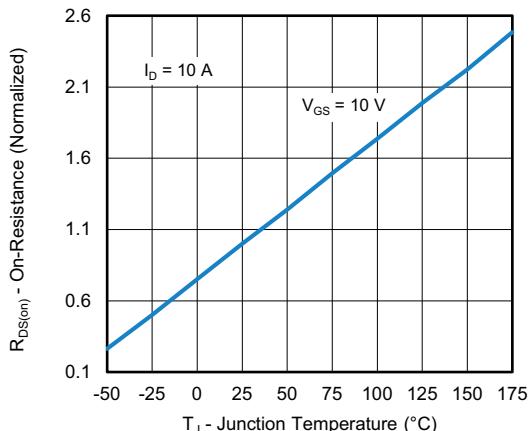
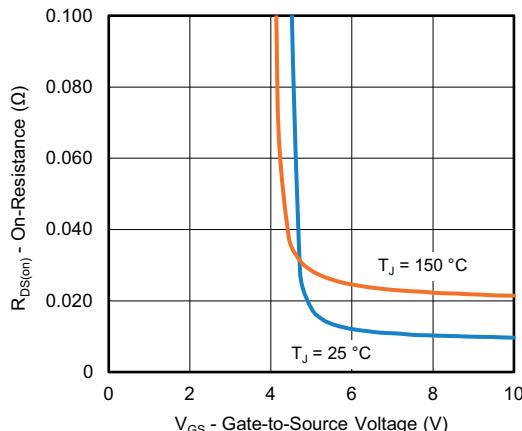
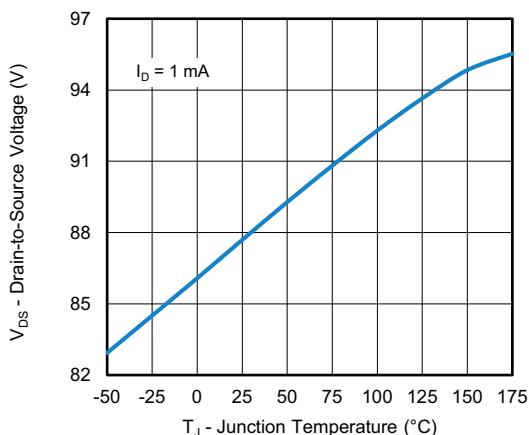
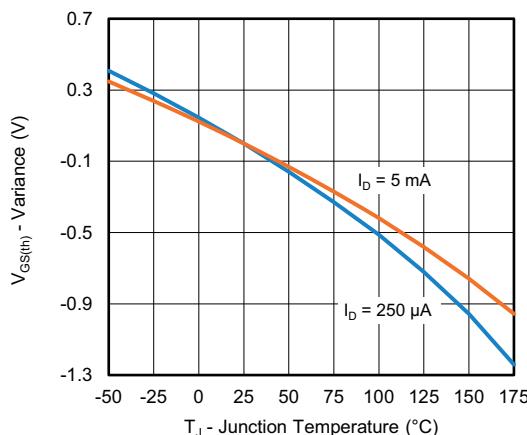
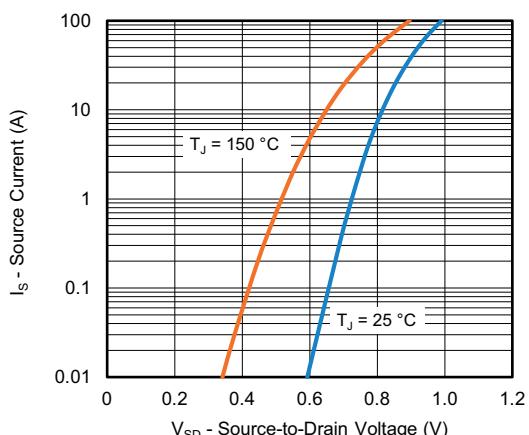
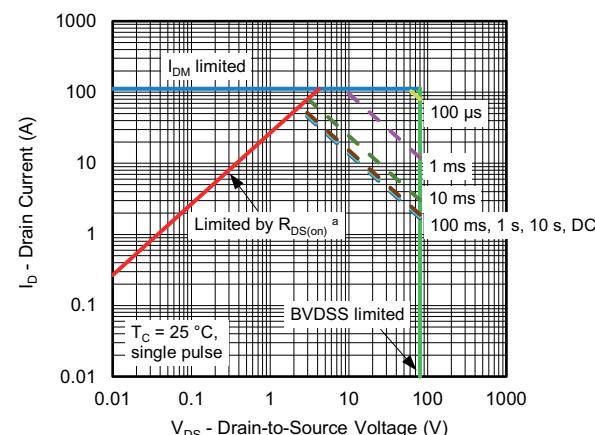
SPECIFICATIONS ($T_C = 25^\circ\text{C}$, unless otherwise noted)								
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0$, $I_D = 250 \mu\text{A}$		80	-	-	V	
Gate-source threshold voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$		2.5	3.0	3.5		
Gate-source leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA	
Zero gate voltage drain current	I_{DSS}	$V_{GS} = 0 \text{ V}$	$V_{DS} = 80 \text{ V}$	-	-	10	μA	
		$V_{GS} = 0 \text{ V}$	$V_{DS} = 80 \text{ V}$, $T_J = 125^\circ\text{C}$	-	-	50		
		$V_{GS} = 0 \text{ V}$	$V_{DS} = 80 \text{ V}$, $T_J = 175^\circ\text{C}$	-	-	250		
On-state drain current ^a	$I_{D(\text{on})}$	$V_{GS} = 10 \text{ V}$	$V_{DS} \geq 5 \text{ V}$	30	-	-	A	
Drain-source on-state resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}$	$I_D = 20 \text{ A}$	-	0.0110	0.0150	Ω	
		$V_{GS} = 10 \text{ V}$	$I_D = 20 \text{ A}$, $T_J = 125^\circ\text{C}$	-	-	0.0300		
		$V_{GS} = 10 \text{ V}$	$I_D = 20 \text{ A}$, $T_J = 175^\circ\text{C}$	-	-	0.0380		
Forward transconductance ^b	g_{fs}	$V_{DS} = 15 \text{ V}$, $I_D = 10 \text{ A}$		-	30	-	S	
Dynamic ^b								
Input capacitance	C_{iss}	$V_{GS} = 0 \text{ V}$	$V_{DS} = 25 \text{ V}$, $f = 1 \text{ MHz}$	-	1387	1942	pF	
Output capacitance	C_{oss}			-	228	320		
Reverse transfer capacitance	C_{rss}			-	12	17		
Total gate charge ^c	Q_g	$V_{GS} = 10 \text{ V}$	$V_{DS} = 40 \text{ V}$, $I_D = 25 \text{ A}$	-	24	36	nC	
Gate-source charge ^c	Q_{gs}			-	7	-		
Gate-drain charge ^c	Q_{gd}			-	6	-		
Gate resistance	R_g	$f = 1 \text{ MHz}$		0.7	1.5	2.3	Ω	
Turn-on delay time ^c	$t_{d(\text{on})}$	$V_{DD} = 40 \text{ V}$, $R_L = 1.6 \Omega$ $I_D \approx 25 \text{ A}$, $V_{GEN} = 10 \text{ V}$, $R_g = 1 \Omega$		-	9	14	ns	
Rise time ^c	t_r			-	3	6		
Turn-off delay time ^c	$t_{d(\text{off})}$			-	19	29		
Fall time ^c	t_f			-	4	8		
Source-Drain Diode Ratings and Characteristics ^b								
Pulsed current ^a	I_{SM}			-	-	488	A	
Forward voltage	V_{SD}	$I_F = 15 \text{ A}$, $V_{GS} = 0 \text{ V}$		-	-	1.3	V	
Body diode reverse recovery time	t_{rr}	$I_F = 10 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$		-	39	78	ns	
Body diode reverse recovery charge	Q_{rr}			-	53	106	nC	
Reverse recovery fall time	t_a			-	27	-	ns	
Reverse recovery rise time	t_b			-	12	-		
Body diode peak reverse recovery current	$I_{RM(\text{REC})}$			-	2.6	-	A	

Notes

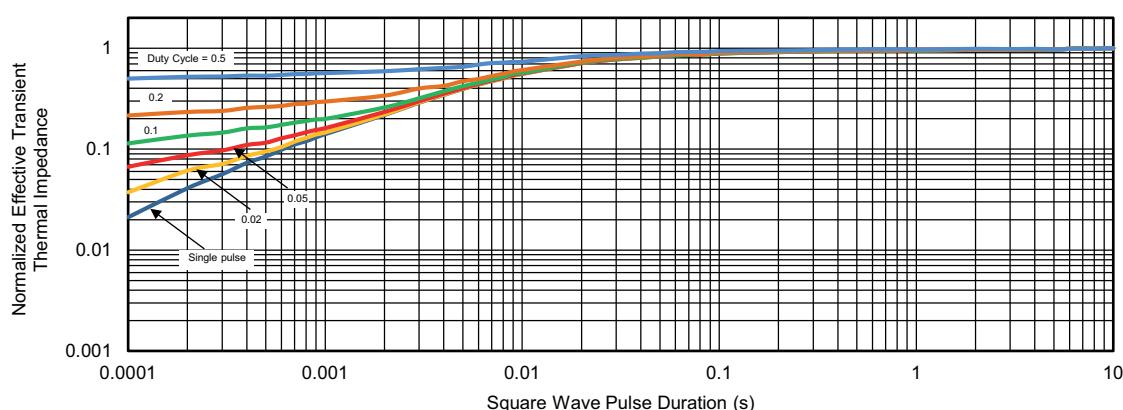
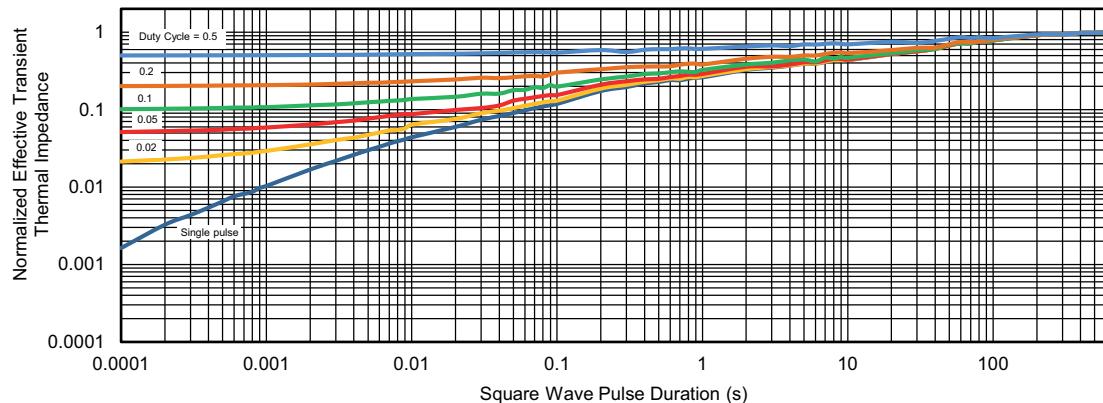
e. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$
f. Guaranteed by design, not subject to production testing
g. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Output Characteristics

Transconductance

Transfer Characteristics

Capacitance

On-Resistance vs. Drain Current

Gate Charge

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

On-Resistance vs. Junction Temperature

On-Resistance vs. Gate-to-Source Voltage

Drain Source Breakdown vs. Junction Temperature

Threshold Voltage

Source Drain Diode Forward Voltage

Safe Operating Area
Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

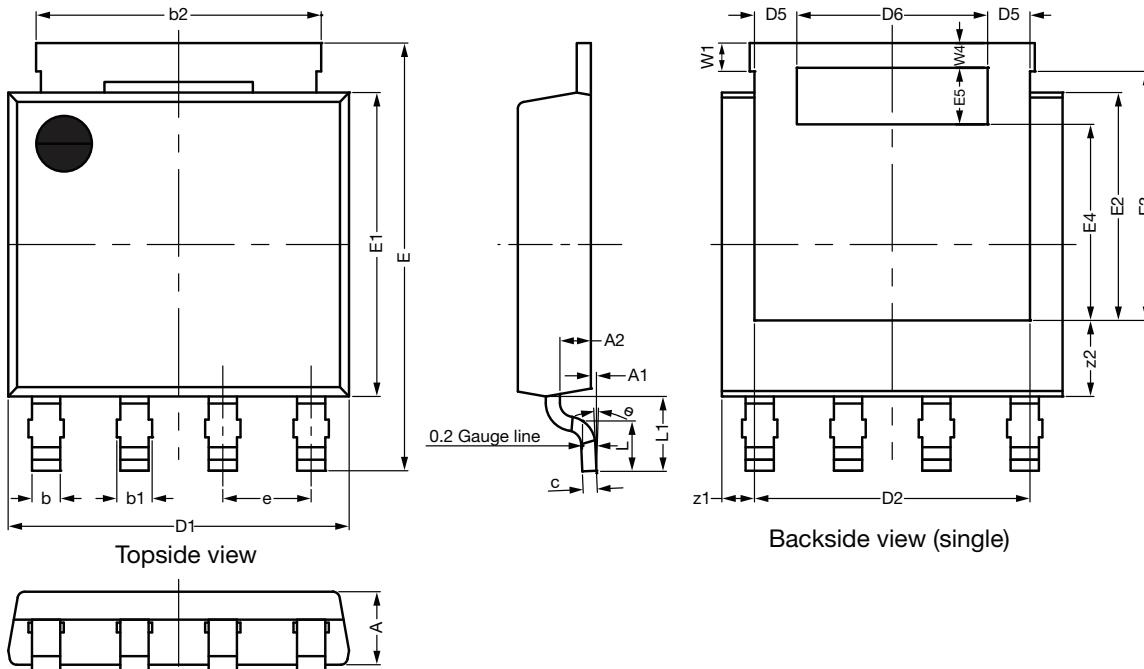
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25°C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25°C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

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PowerPAK® SO-8L Case Outline 3



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.05	1.10	0.039	0.041	0.043
A1	0.00	---	0.127	0.000	---	0.005
A2	0.40	0.45	0.50	0.016	0.018	0.020
b	0.33	0.41	0.49	0.013	0.016	0.019
b1	0.43	0.51	0.59	0.017	0.020	0.023
b2	4.00	4.10	4.20	0.157	0.161	0.165
c	0.15	0.20	0.25	0.006	0.008	0.010
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D5	0.51	0.61	0.71	0.020	0.024	0.028
D6	2.64	2.74	2.84	0.104	0.108	0.112
e	1.27 BSC			0.050 BSC		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	3.18	3.28	3.38	0.125	0.129	0.133
E3	3.48	3.58	3.68	0.137	0.141	0.145
E4	2.72	2.82	2.92	0.107	0.111	0.115
E5	0.71	0.81	0.91	0.028	0.032	0.036
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
W1	0.31	0.41	0.51	0.012	0.016	0.020
W4	0.31	0.36	0.41	0.012	0.014	0.016
z1	0.37	0.47	0.57	0.015	0.019	0.022
z2	0.99	1.09	1.19	0.039	0.043	0.047
θ	0°	---	5°	0°	---	5°

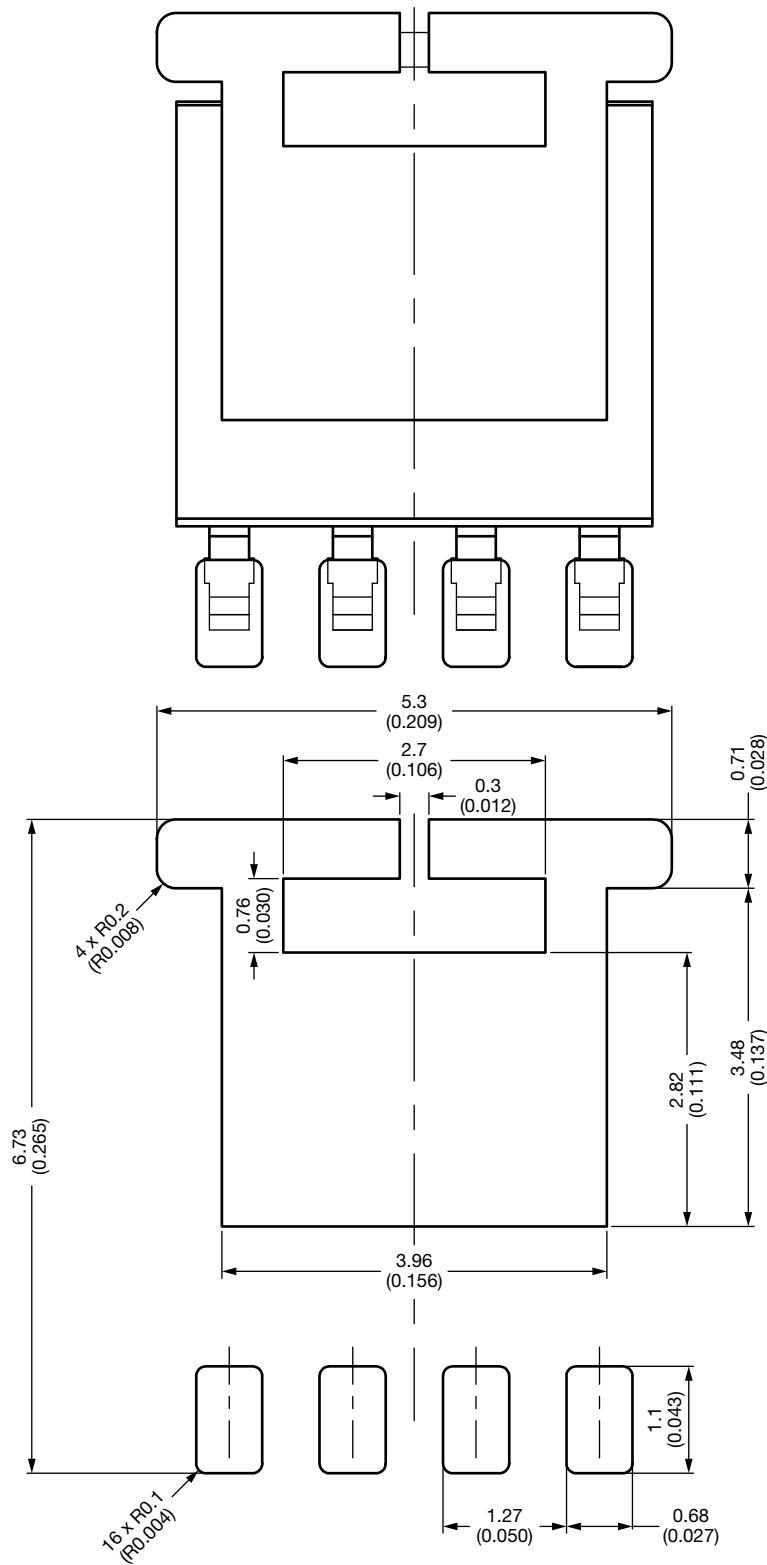
ECN: S19-0643-Rev. B, 05-Aug-2019

DWG: 6067

Note

- Millimeter will govern

Recommended Land Pattern PowerPAK® SO-8L Single Short Ear



Dimensions in Millimeters (Inches)

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