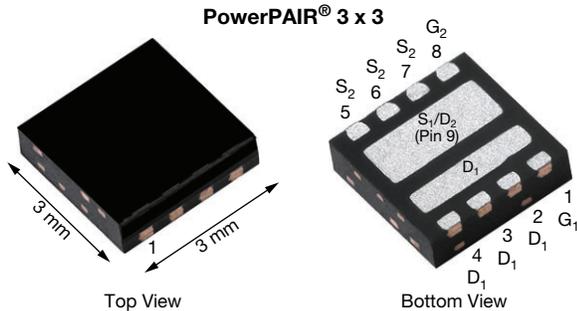


Dual N-Channel 30 V (D-S) MOSFET



FEATURES

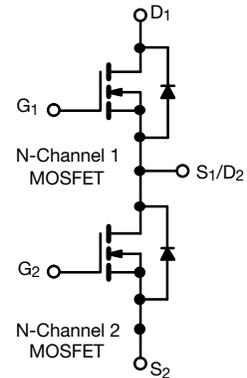
- TrenchFET® Gen IV power MOSFET
- High side and low side MOSFETs form optimized combination for 50 % duty cycle
- Optimized $R_{DS} - Q_g$ and $R_{DS} - Q_{gd}$ FOM elevates efficiency for high frequency switching
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Synchronous buck
- DC/DC conversion
- Half bridge
- POL



PRODUCT SUMMARY	
MOSFET CHANNEL-1 AND CHANNEL-2	
V_{DS} (V)	30
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.0094
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.0144
Q_g typ. (nC)	3.7
I_D (A)	33.4 ^a
Configuration	Dual

ORDERING INFORMATION	
Package	PowerPAIR 3 x 3
Lead (Pb)-free and halogen-free	SiZ342ADT-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)			
PARAMETER	CHANNEL-1 AND CHANNEL-2		
	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	30	V
Gate-source voltage	V_{GS}	+20 / -16	
Continuous drain current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	A
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Pulsed drain current ($t = 100$ μ s)	I_{DM}	100	A
Continuous source current (MOSFET diode conduction)	I_S	$T_C = 25$ °C	
		$T_A = 25$ °C	
Single pulse avalanche current	I_{AS}	10	
Single pulse avalanche energy	E_{AS}	5	
Maximum power dissipation	P_D	$T_C = 25$ °C	W
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature)		260	

Notes

- $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s



THERMAL RESISTANCE RATINGS						
PARAMETER		CHANNEL-1 AND CHANNEL-2				
		SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient ^{a, b}	$t \leq 10$ s	R_{thJA}	27	34	°C/W	
Maximum junction-to-case (drain)	Steady state	R_{thJC}	6	7.5		

Notes

- a. Surface mounted on 1" x 1" FR4 board
- b. Maximum under steady state conditions is 69 °C/W

SPECIFICATIONS ($T_J = 25$ °C, unless otherwise noted)						
PARAMETER	CHANNEL-1 AND CHANNEL-2					
	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0$ V, $I_D = 250$ μ A	30	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250$ μ A	1	-	2.4	
Gate-source leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = +20$ V / -16 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 30$ V, $V_{GS} = 0$ V	-	-	1	μ A
		$V_{DS} = 30$ V, $V_{GS} = 0$ V, $T_J = 55$ °C	-	-	5	
On-state drain current ^a	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 10$ V	30	-	-	A
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 10$ A	-	0.0078	0.0094	Ω
		$V_{GS} = 4.5$ V, $I_D = 7$ A	-	0.0120	0.0144	
Forward transconductance ^a	g_{fs}	$V_{DS} = 10$ V, $I_D = 10$ A	-	57	-	S
Dynamic ^b						
Input capacitance	C_{iss}	$V_{DS} = 15$ V, $V_{GS} = 0$ V, $f = 1$ MHz	-	580	-	pF
Output capacitance	C_{oss}		-	250	-	
Reverse transfer capacitance	C_{rss}		-	30	-	
C_{rss}/C_{iss} ratio			-	0.052	0.103	
Total gate charge	Q_g	$V_{DS} = 15$ V, $V_{GS} = 10$ V, $I_D = 15.7$ A	-	8.1	12.2	nC
Gate-source charge	Q_{gs}	$V_{DS} = 15$ V, $V_{GS} = 4.5$ V, $I_D = 15.7$ A	-	3.7	4.5	
Gate-drain charge	Q_{gd}		-	2.4	-	
Gate resistance	R_g		$f = 1$ MHz	-	0.67	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 15$ V, $R_L = 1.2$ Ω , $I_D \cong 12.5$ A, $V_{GEN} = 10$ V, $R_g = 1$ Ω	0.24	1.2	2.4	ns
Rise time	t_r		-	10	20	
Turn-off delay time	$t_{d(off)}$		-	6	12	
Fall time	t_f		-	18	36	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 15$ V, $R_L = 1.2$ Ω , $I_D \cong 12.5$ A, $V_{GEN} = 4.5$ V, $R_g = 1$ Ω	-	8	16	
Rise time	t_r		-	15	30	
Turn-off delay time	$t_{d(off)}$		-	180	360	
Fall time	t_f		-	20	40	
			-	15	30	



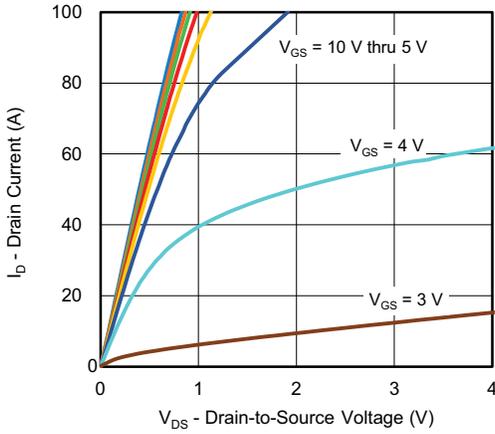
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	CHANNEL-1 AND CHANNEL-2					
	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain-source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25°C	-	-	13.9	A
Pulse diode forward current	I _{SM}		-	-	100	
Body diode voltage	V _{SD}	I _S = 12.5 A, V _{GS} = 0 V	-	0.85	1.2	V
Body diode reverse recovery time	t _{rr}	I _F = 12.5 A, di/dt = 100 A/μs, T _J = 25 °C	-	15	30	ns
Body diode reverse recovery charge	Q _{rr}		-	4.3	8.6	nC
Reverse recovery fall time	t _a		-	8	-	ns
Reverse recovery rise time	t _b		-	7	-	

Notes

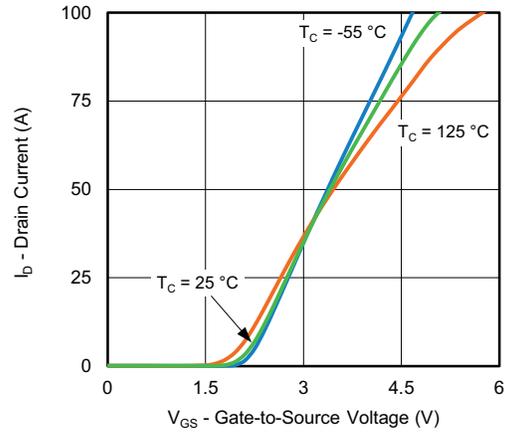
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

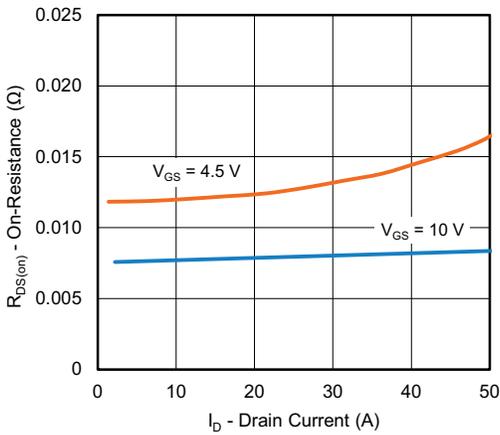
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



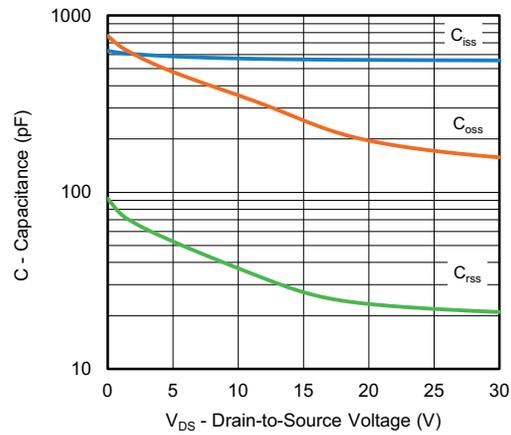
Output Characteristics



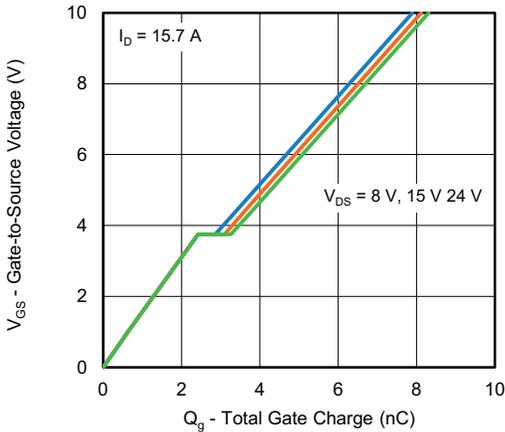
Transfer Characteristics



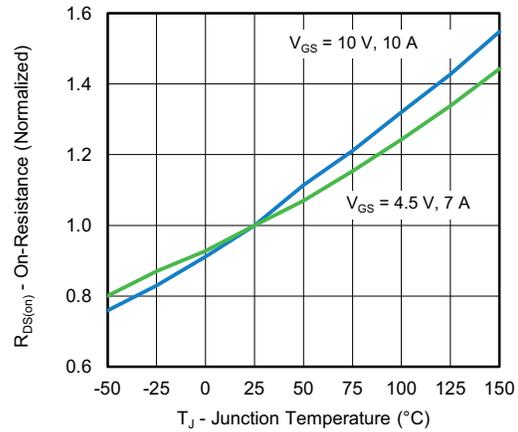
On-Resistance vs. Drain Current and Gate



Capacitance



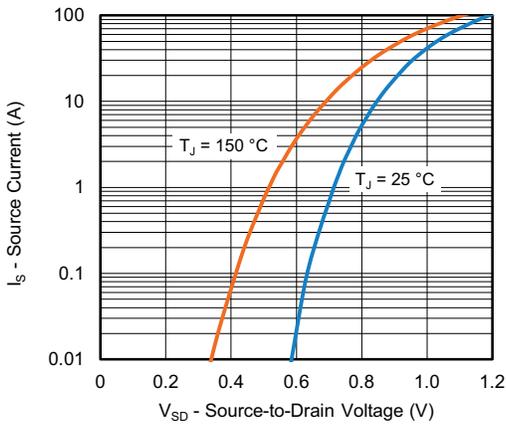
Gate Charge



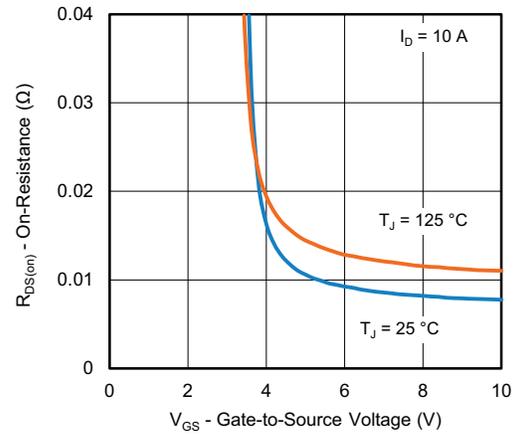
On-Resistance vs. Junction Temperature



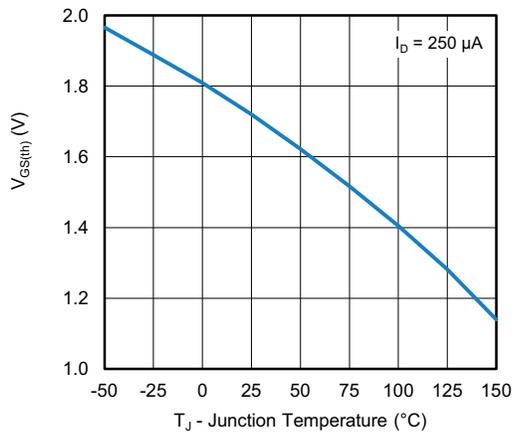
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



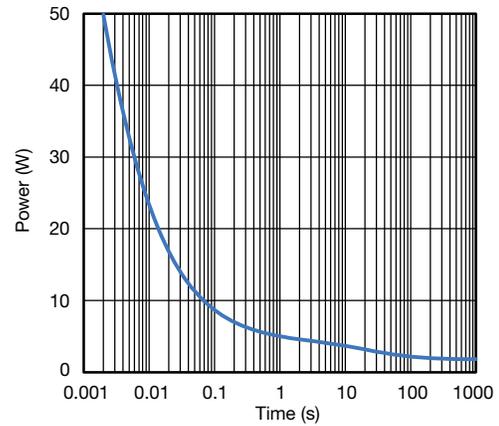
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



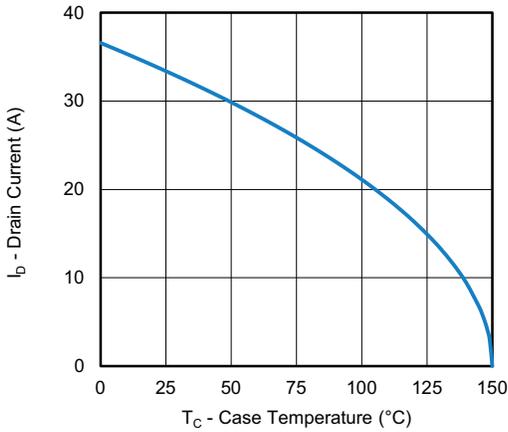
Threshold Voltage



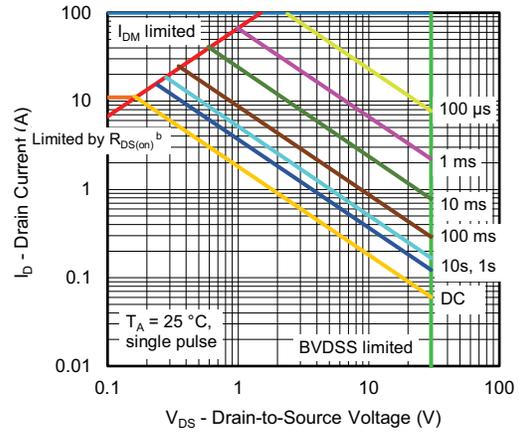
Single Pulse Power



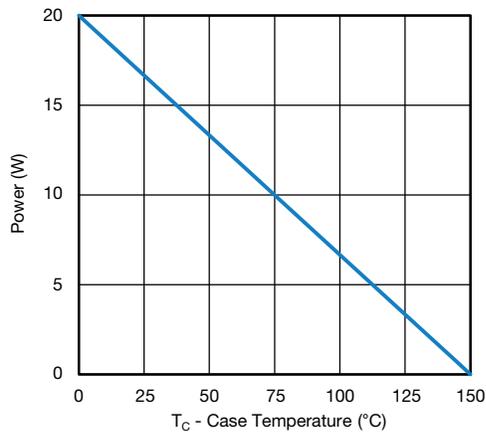
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



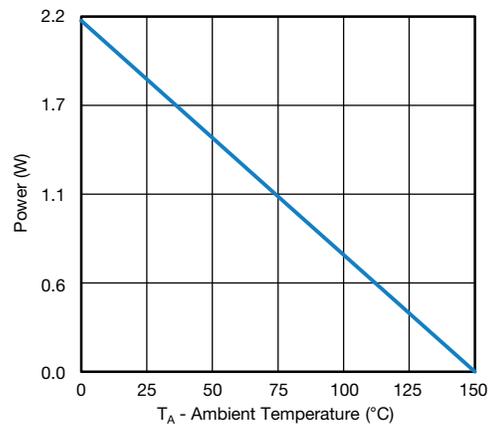
Current Derating ^a



Safe Operating Area, Junction-to-Ambient



Power, Junction-to-Case



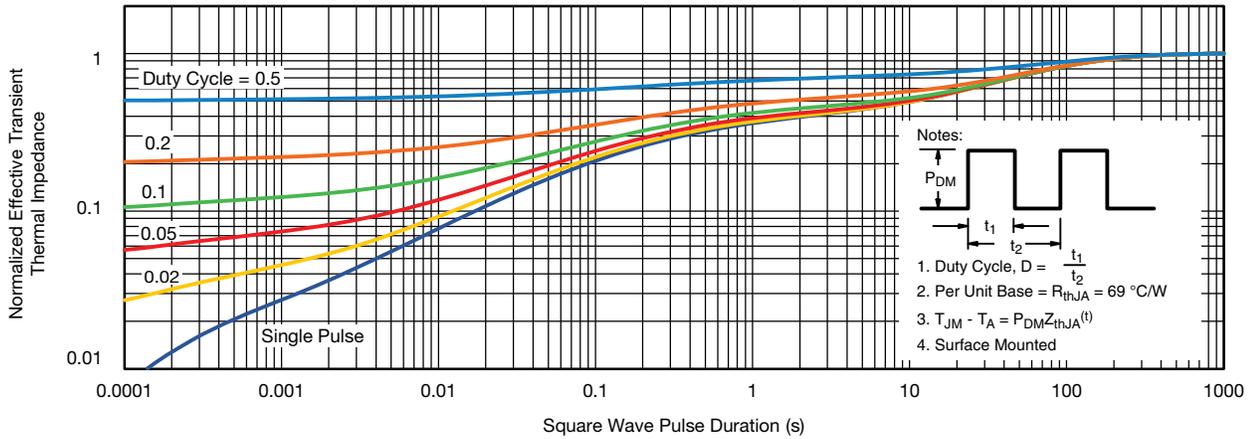
Power, Junction-to-Ambient

Notes

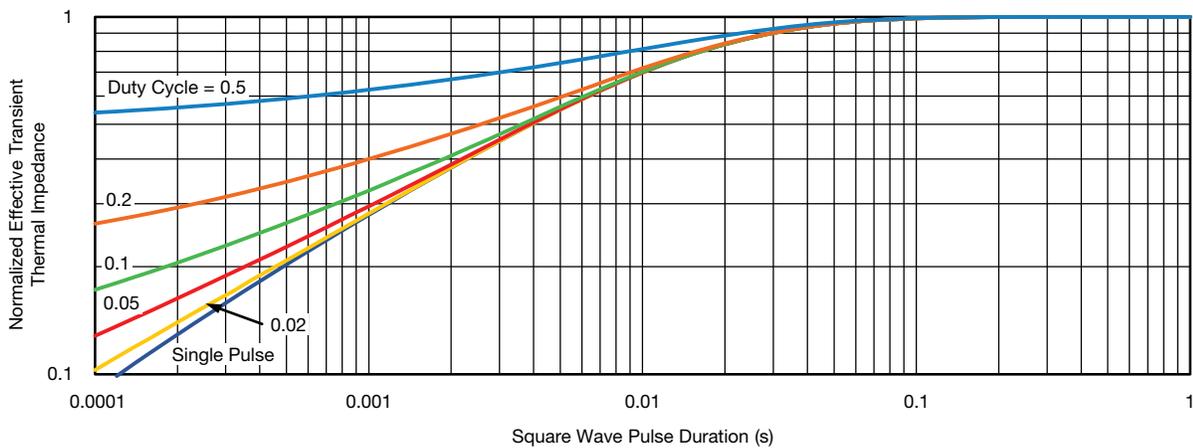
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-ambient thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit
- b. V_{GS} > minimum V_{GS} at which R_{DS(on)} is specified



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

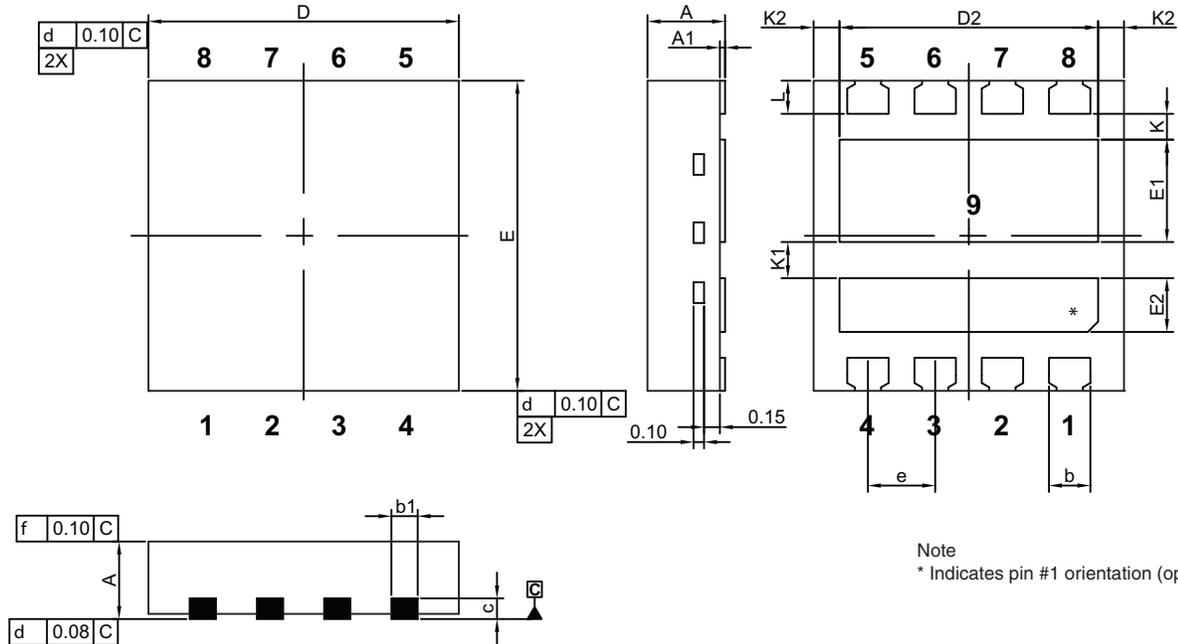


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?76711.



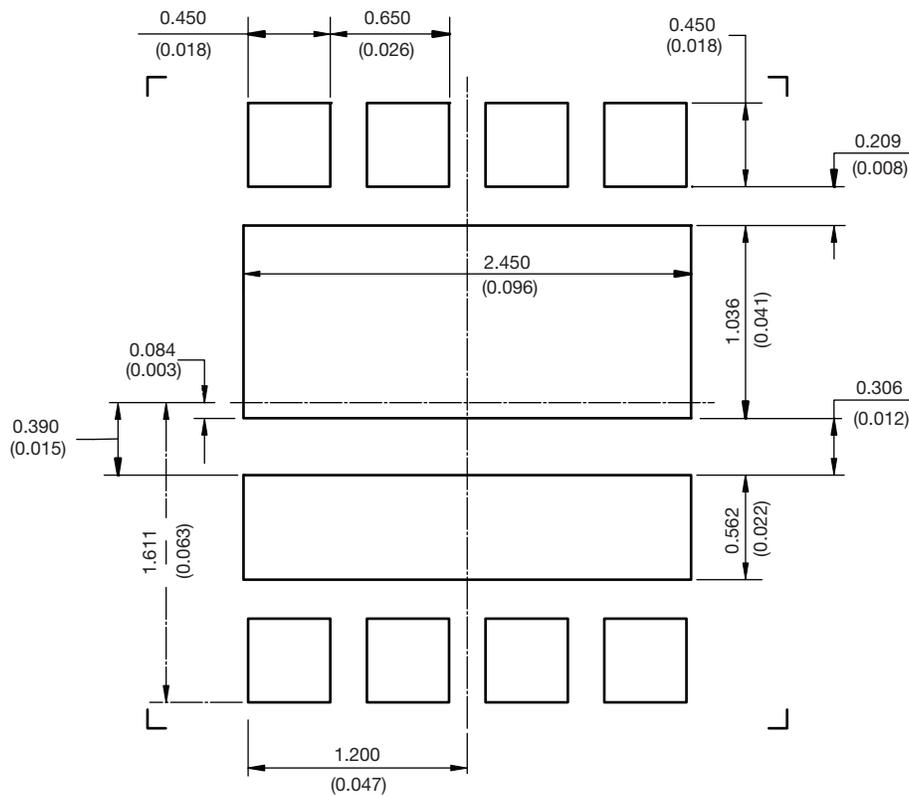
PowerPAIR® 3 x 3 Case Outline



Note
* Indicates pin #1 orientation (optional)

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00		0.05	0.000		0.002
b	0.35	0.40	0.45	0.014	0.016	0.018
b1	0.20	0.25	0.38	0.008	0.010	0.015
C	0.18	0.20	0.23	0.007	0.008	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
D2	2.35	2.40	2.45	0.093	0.094	0.096
E	2.90	3.00	3.10	0.114	0.118	0.122
E1	0.94	0.99	1.04	0.037	0.039	0.041
E2	0.47	0.52	0.57	0.019	0.020	0.022
e	0.65 BSC			0.026 BSC		
K	0.25 typ.			0.010 typ.		
K1	0.35 typ.			0.014 typ.		
K2	0.30 typ.			0.012 typ.		
L	0.27	0.32	0.37	0.011	0.013	0.015
ECN: T12-0347-Rev. C, 18-Jun-12						
DWG: 5998						

RECOMMENDED MINIMUM PAD FOR PowerPAIR® 3 x 3



Recommended PAD for PowerPAIR 3 x 3

Dimensions in millimeters (inches)

Keep-Out 3.5 mm x 3.5 mm for non terminating traces



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