

## E Series Power MOSFET

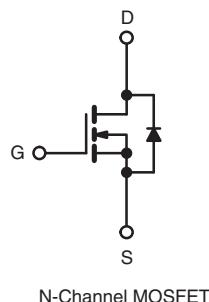
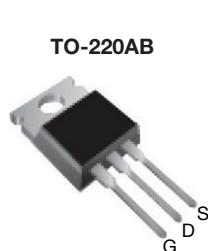
PRODUCT SUMMARY	
$V_{DS}$ (V) at $T_J$ max.	550
$R_{DS(on)}$ max. at 25 °C (Ω)	$V_{GS} = 10$ V 0.184
$Q_g$ max. (nC)	92
$Q_{gs}$ (nC)	10
$Q_{gd}$ (nC)	19
Configuration	Single

### FEATURES

- Low figure-of-merit (FOM)  $R_{on} \times Q_g$
- Low input capacitance ( $C_{iss}$ )
- Reduced switching and conduction losses
- Low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
**HALOGEN**  
**FREE**



### APPLICATIONS

- Computing
  - PC silver box / ATX power supplies
- Lighting
  - Two stage LED lighting
- Consumer electronics
- Applications using hard switched topologies
  - Power factor correction (PFC)
  - Two switch forward converter
  - Flyback converter
- Switch mode power supplies (SMPS)

### ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free and Halogen-free	SiHP20N50E-GE3

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	500	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	
Continuous Drain Current ( $T_J = 150$ °C)	$V_{GS}$ at 10 V	19	A
		12	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	42	
Linear Derating Factor		1.4	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	204	mJ
Maximum Power Dissipation	$P_D$	179	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	°C
Drain-Source Voltage Slope	$V_{DS} = 0$ V to 80 % $V_{DS}$	dV/dt	V/ns
Reverse Diode dV/dt <sup>d</sup>		70	
Reverse Diode dV/dt <sup>d</sup>		32	
Soldering Recommendations (Peak Temperature) <sup>c</sup>	for 10 s	300	°C

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$  Ω,  $I_{AS} = 3.8$  A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$ ,  $dI/dt = 100$  A/μs, starting  $T_J = 25$  °C.

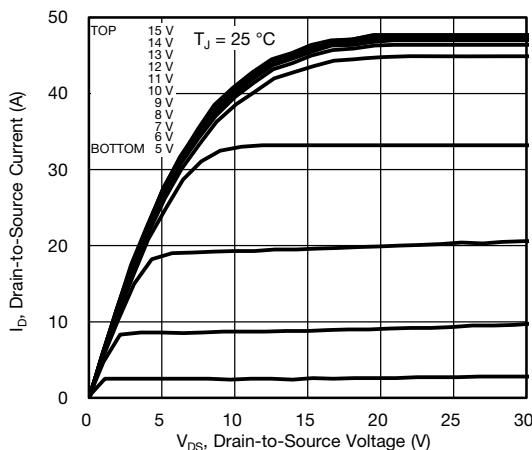
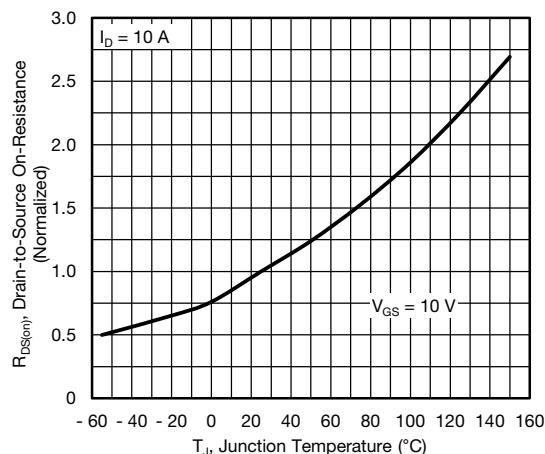
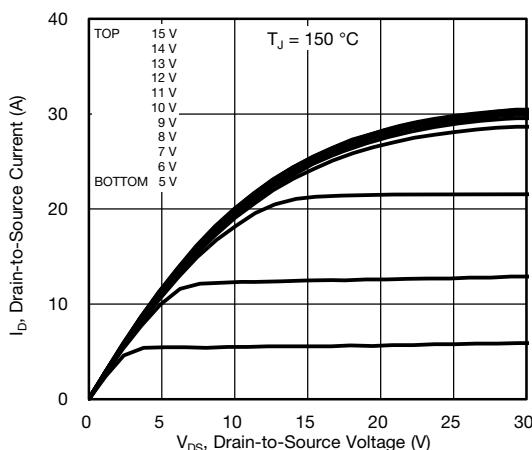
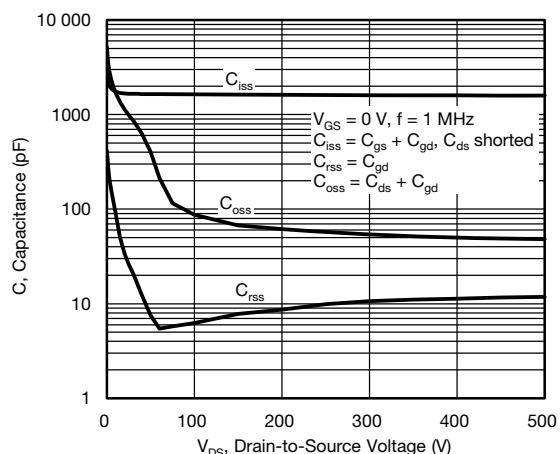
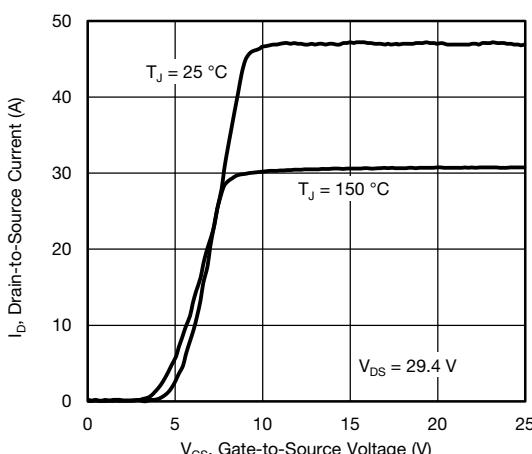
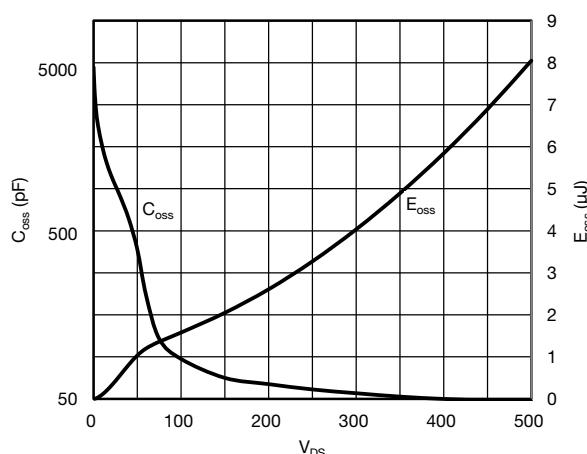
### THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.7	

<b>SPECIFICATIONS</b> ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}$ , $I_D = 250 \mu\text{A}$		500	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25^\circ\text{C}$ , $I_D = 1 \text{ mA}$		-	0.59	-	$\text{V}/^\circ\text{C}$
Gate-Source Threshold Voltage (N)	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$ , $I_D = 250 \mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20 \text{ V}$		-	-	$\pm 100$	nA
		$V_{GS} = \pm 30 \text{ V}$		-	-	$\pm 1$	$\mu\text{A}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 500 \text{ V}$ , $V_{GS} = 0 \text{ V}$		-	-	1	$\mu\text{A}$
		$V_{DS} = 400 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $T_J = 125^\circ\text{C}$		-	-	10	
Drain-Source On-State Resistance	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}$	$I_D = 10 \text{ A}$	-	0.160	0.184	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 30 \text{ V}$ , $I_D = 10 \text{ A}$		-	4.4	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0 \text{ V}$ , $V_{DS} = 100 \text{ V}$ , $f = 1 \text{ MHz}$		-	1640	-	$\text{pF}$
Output Capacitance	$C_{oss}$			-	87	-	
Reverse Transfer Capacitance	$C_{rss}$			-	6	-	
Effective Output Capacitance, Energy Related <sup>a</sup>	$C_{o(er)}$	$V_{DS} = 0 \text{ V to } 400 \text{ V}$ , $V_{GS} = 0 \text{ V}$		-	73	-	
Effective Output Capacitance, Time Related <sup>b</sup>	$C_{o(tr)}$			-	222	-	
Total Gate Charge	$Q_g$			-	46	92	$\text{nC}$
Gate-Source Charge	$Q_{gs}$	$V_{GS} = 10 \text{ V}$	$I_D = 10 \text{ A}$ , $V_{DS} = 400 \text{ V}$	-	10	-	
Gate-Drain Charge	$Q_{gd}$			-	19	-	
Turn-On Delay Time	$t_{d(on)}$			-	17	34	$\text{ns}$
Rise Time	$t_r$	$V_{DD} = 400 \text{ V}$ , $I_D = 10 \text{ A}$ , $V_{GS} = 10 \text{ V}$ , $R_g = 9.1 \Omega$		-	27	54	
Turn-Off Delay Time	$t_{d(off)}$			-	48	96	
Fall Time	$t_f$			-	25	50	
Gate Input Resistance	$R_g$	$f = 1 \text{ MHz}$ , open drain		-	0.83	-	$\Omega$
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_s$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	19	$\text{A}$
Pulsed Diode Forward Current	$I_{SM}$			-	-	42	
Diode Forward Voltage	$V_{SD}$	$T_J = 25^\circ\text{C}$ , $I_S = 10 \text{ A}$ , $V_{GS} = 0 \text{ V}$		-	-	1.2	V
Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ\text{C}$ , $I_F = I_S = 10 \text{ A}$ , $dl/dt = 100 \text{ A}/\mu\text{s}$ , $V_R = 25 \text{ V}$		-	293	-	ns
Reverse Recovery Charge	$Q_{rr}$			-	4.0	-	$\mu\text{C}$
Reverse Recovery Current	$I_{RRM}$			-	26	-	A

**Notes**

a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .  
b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics**

**Fig. 4 - Normalized On-Resistance vs. Temperature**

**Fig. 2 - Typical Output Characteristics**

**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 6 -  $C_{oss}$  and  $E_{oss}$  vs.  $V_{DS}$**

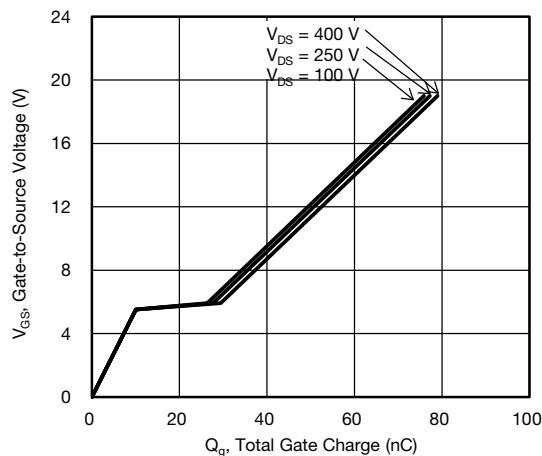


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

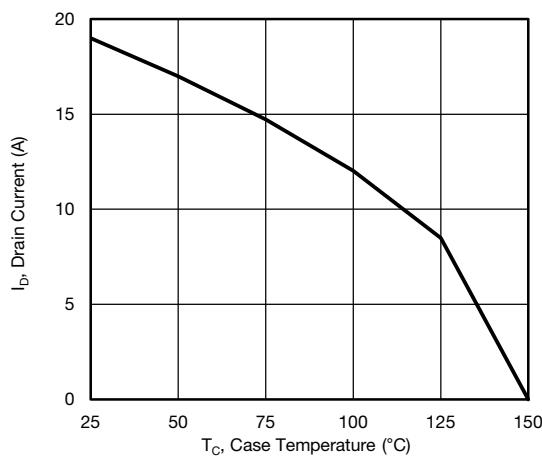


Fig. 10 - Maximum Drain Current vs. Case Temperature

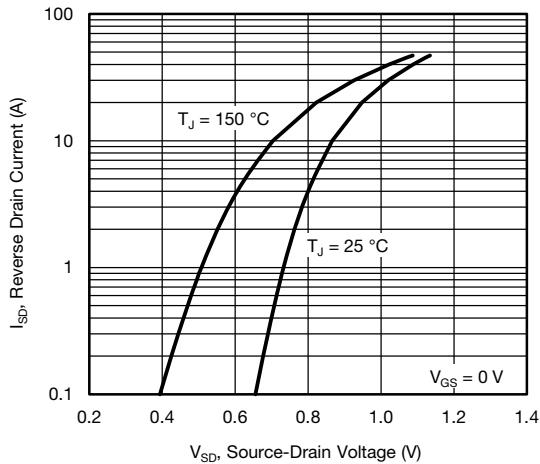


Fig. 8 - Typical Source-Drain Diode Forward Voltage

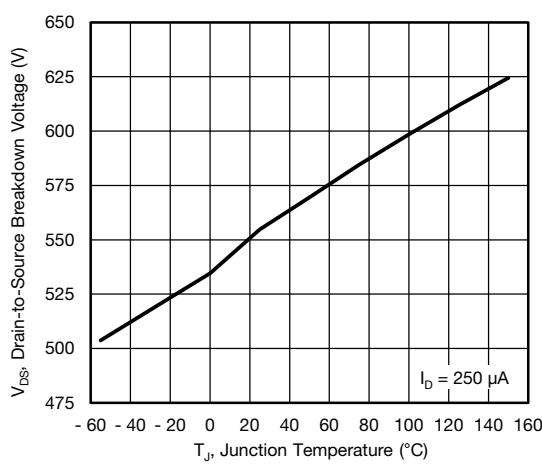


Fig. 11 - Temperature vs. Drain-to-Source Voltage

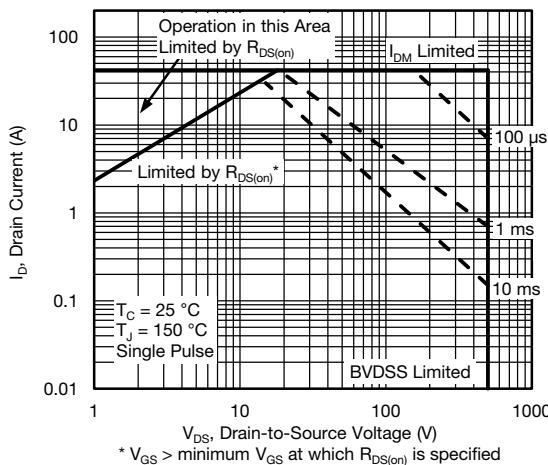
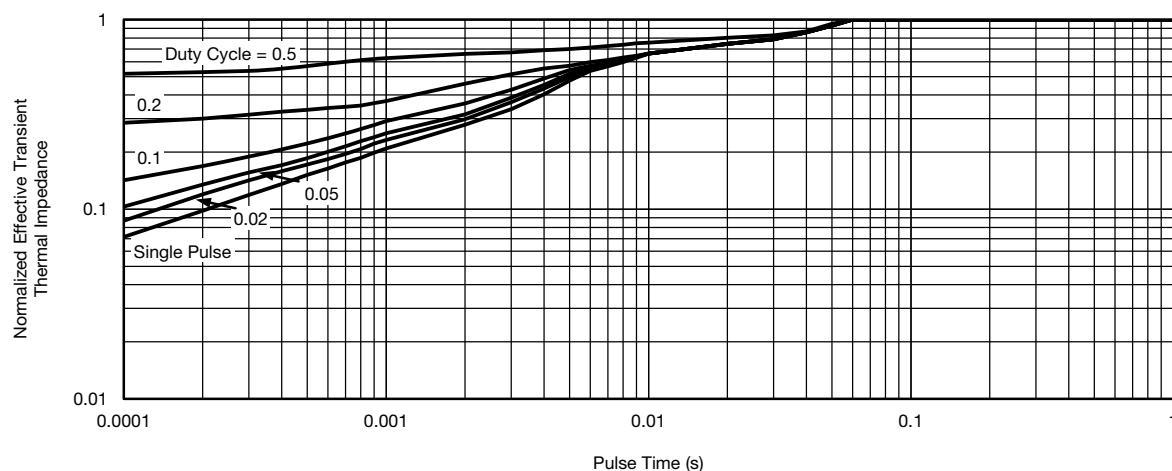
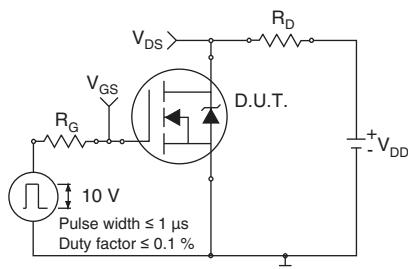


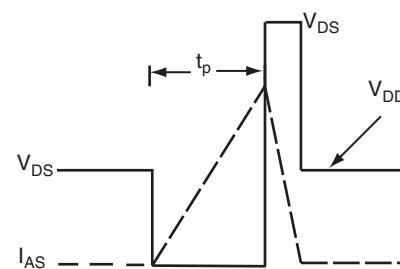
Fig. 9 - Maximum Safe Operating Area



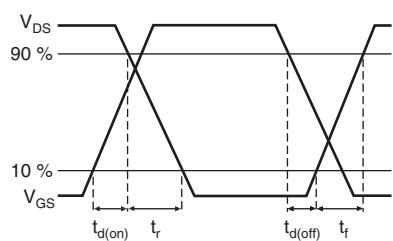
**Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case**



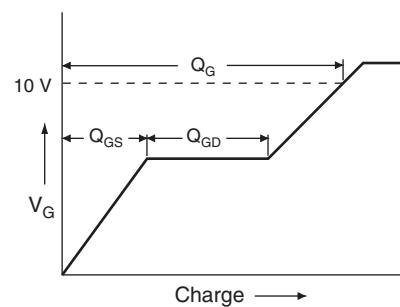
**Fig. 13 - Switching Time Test Circuit**



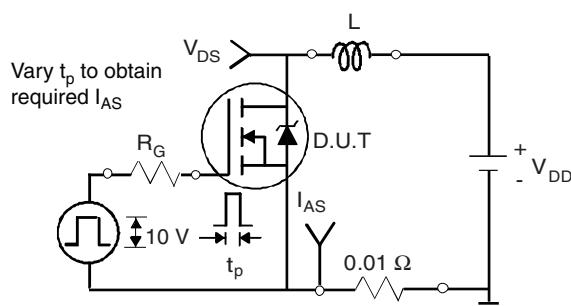
**Fig. 16 - Unclamped Inductive Waveforms**



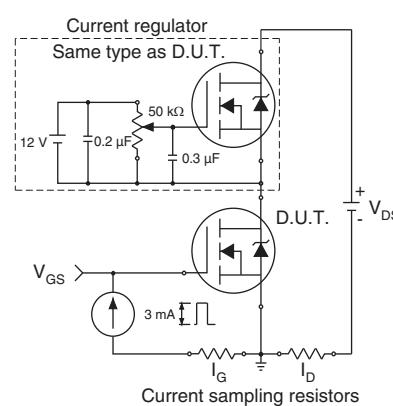
**Fig. 14 - Switching Time Waveforms**



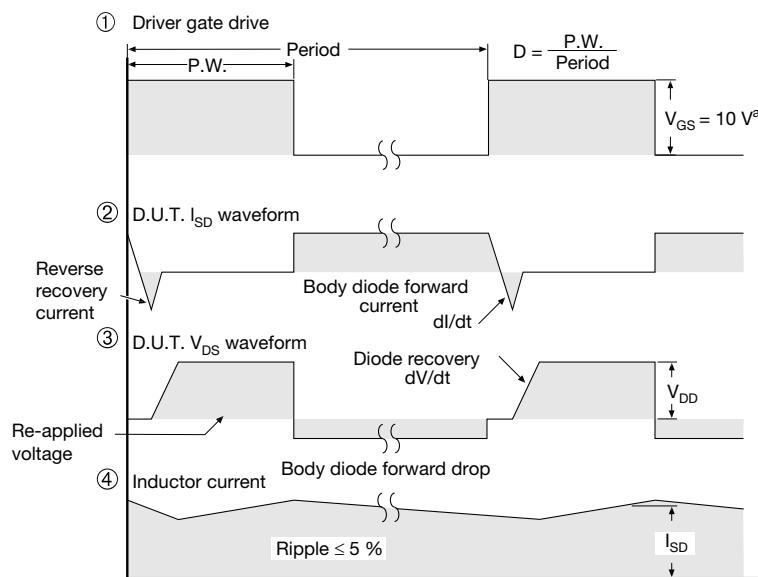
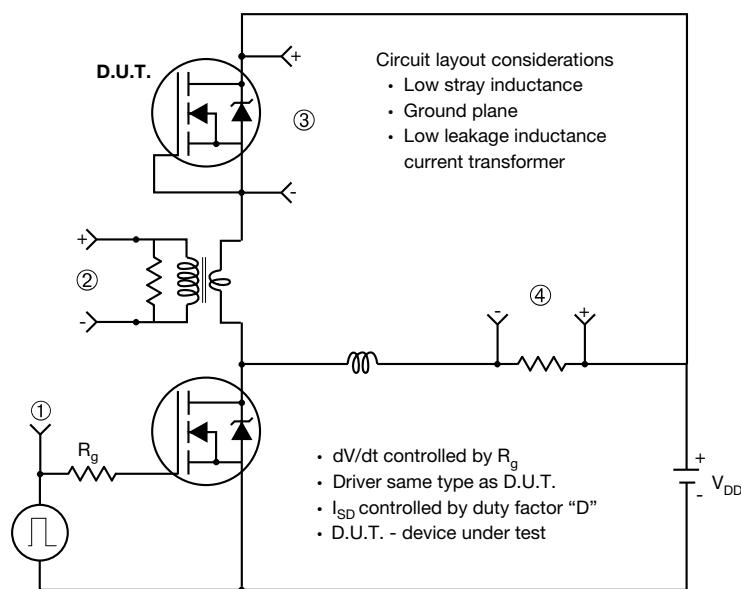
**Fig. 17 - Basic Gate Charge Waveform**



**Fig. 15 - Unclamped Inductive Test Circuit**



**Fig. 18 - Gate Charge Test Circuit**

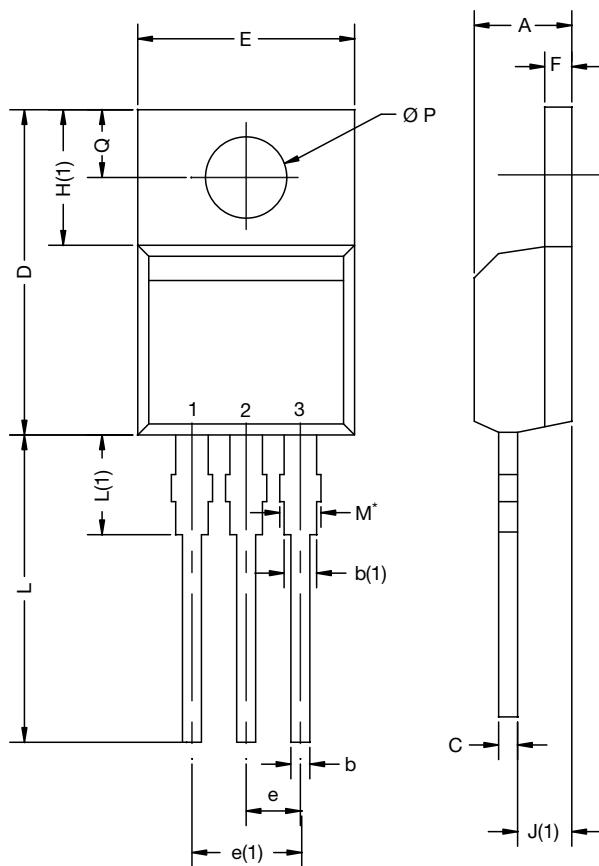
**Peak Diode Recovery dV/dt Test Circuit**

**Note**

a.  $V_{GS} = 5 \text{ V}$  for logic level devices

**Fig. 19 - For N-Channel**

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### TO-220-1



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
$\varnothing P$	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118

ECN: E21-0621-Rev. D, 04-Nov-2021  
DWG: 6031

#### Note

- $M^* = 0.052$  inches to  $0.064$  inches (dimension including protrusion), heatsink hole for HVM

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