

Power-off Protection, 6 Ω , 1.8 V to 5.5 V, SPDT Analog Switch (2:1 Multiplexer)

DESCRIPTION

The DG2002E is a high performance single-pole, double-throw (SPDT) analog switch designed for 1.8 V to 5.5 V operation with a single power rail.

Fabricated with high density CMOS technology, the device achieves low on resistance of 6 Ω and switch off capacitance of 7 pF at a 5 V power supply and low power consumption, and fast switching speeds. Its charge injection is 1 pC.

The DG2002E can handle both analog and digital signals and permits signals with amplitudes of up to V_+ to be transmitted in either direction. Its control logic inputs can go over V_+ up to 5.5 V. It features break before make switching performance.

A powered-off protection circuit is built into the switch to prevent an abnormal current flow from COM pin to V_+ during the power-down condition. Each output pin can withstand greater than 7 kV (human body model).

Operation temperature is specified from -40 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$. The DG2002E is available in the compact SC-70-6L package.

FEATURES

- Low switch on-resistance (6 Ω)
- +1.8 V to +5.5 V single supply operation
- Powered-off protection
- Control logic inputs can go over V_+
- Low parasitic capacitance, 7 pF at switch off
- Low charge injection, 1 pC
- Break before make switching
- Latch-up performance exceeds 200 mA per JESD 78
- High ESD rating
 - 7000 V human body model (JS-001)
 - 1000 V charge device model (JS-002)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Note

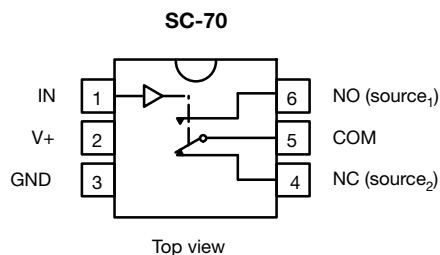
* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details



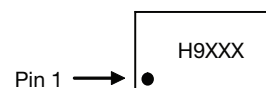
APPLICATIONS

- Battery powered devices
- Instrumentation
- Medical equipment
- Low voltage data acquisition
- Control and automation
- Consumer and computing

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Device marking: H9



Device marking: H9XXX
XXX = Date / lot traceability code

TRUTH TABLE		
LOGIC	NC	NO
0	On	Off
1	Of	On

Notes

- Logic "0" ≤ 0.8 V
- Logic "1" ≥ 2.4 V

ORDERING INFORMATION		
TEMP. RANGE	PACKAGE	PART NUMBER
-40 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$	SC-70-6	DG2002EDL-T1-GE3

**ABSOLUTE MAXIMUM RATINGS**

PARAMETER		LIMIT	UNIT
V+, COM, NC, NO, IN reference to GND		-0.3 to 6	V
Continuous current (any terminal)		± 50	mA
Peak current (pulsed at 1 ms, 10 % duty cycle)		± 200	
Storage temperature		-65 to +150	°C
Power dissipation (packages) ^a	6-pin SC-70 ^b	250	mW
ESD / HBM	JS-001	7000	V
ESD / CDM	JS-002	1000	
Latch up	Per JESD78 with 1.5 x voltage clamp	200	mA

Notes

a. All leads welded or soldered to PC board

b. Derate 3.1 mW/°C above 70 °C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (V+ = 5 V)

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 5 V, ± 10 % VIN = 0.8 V or 2.4 V ^e	TEMP. ^a	LIMITS -40 °C to +85 °C			UNIT
				MIN. ^b	TYP. ^c	MAX. ^b	
Analog Switch							
Analog signal range ^d	VNO, VNC VCOM		Full	0	-	V+	V
Drain-source on-resistance ^d	RDS(on)	V+ = 4.5 V, VCOM = 3 V, INO, INC = 10 mA	Room	-	6	8	Ω
			Full	-	8	10	
RDS(on) flatness ^d	RDS(on) flatness	V+ = 5 V, VCOM = 1.5 V, 3.5 V, INO, INC = 10 mA	Room	-	0.4	-	nA
RDS(on) match ^d	ΔRDS(on)	V+ = 4.5 V, VCOM = 3 V, INO, INC = 10 mA	Room	-	0.04	0.2	
Switch-off leakage current ^f	INO(off), INC(off)	V+ = 5.5 V, VNO, VNC = 1 V / 4.5 V, VCOM = 4.5 V / 1 V	Room	-1.5	-	1.5	
	ICOM(off)		Full	-4	-	4	
			Room	-1	-	1	
			Full	-4	-	4	
Channel-on leakage current ^f	ICOM(on)	V+ = 5.5 V, VNO, VNC = VCOM = 1 V / 4.5 V	Room	-1	-	1	μA
			Full	-4	-	4	
Power-down leakage	IPD	V+ = 0 V, VCOM = 5 V, NO/NC open, VIN = GND	Full	-	-	2	μA
		V+ = 0 V, VNO, VNC = 5 V, COM open, VIN = GND	Full	-	-	2	
Digital Control							
Input high voltage	VINH		Full	2.4	-	-	V
Input low voltage	VINL		Full	-	-	0.8	
Input capacitance ^d	CIN		Full	-	6	-	pF
Input current	IINL or IINH	VIN = 0 V or V+	Full	-1	-	1	μA
Dynamic Characteristics							
Turn-on time ^d	tON	VNO or VNC = 3 V, RL = 300 Ω, CL = 35 pF	Room	-	10	30	ns
			Full	-	-	32	
Turn-off time ^d	tOFF		Room	-	8	24	
			Full	-	-	26	
Break-before-make time ^d	tBBM		Room	1	-	-	
Charge injection ^d	QINJ	CL = 1 nF, VGEN = 0 V, VNO, VNC = 0 V, RGEN = 0 Ω	Room	-	1	-	pC
Off-isolation ^d	OIRR	RL = 50 Ω, CL = 5 pF, f = 1 MHz	Room	-	-78	-	dB
Crosstalk ^d	XTALK		Room	-	-77	-	
NO, NC off capacitance ^d	CNO(off)	VIN = 0 V or V+, f = 1 MHz	Room	-	7	-	pF
	CNC(off)		Room	-	7	-	
Channel-on capacitance ^d	CON		Room	-	13	-	
Power Supply							
Power supply current ^d	I+	VIN = 0 V or V+	Full	-	0.004	1	μA



SPECIFICATIONS (V+ = 3 V)							
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 3 V, ± 10 % VIN = 0.4 V or 2 V ^e	TEMP. ^a	LIMITS -40 °C to +85 °C			UNIT
				MIN. ^b	TYP. ^c	MAX. ^b	
Analog Switch							
Analog signal range ^d	VNO, VNC VCOM		Full	0	-	V+	V
Drain-source on-resistance ^d	RDS(on)	V+ = 2.7 V, VCOM = 1.5 V, INO, INC = 10 mA	Room	-	13	22	Ω
			Full	-	15	24	
RDS(on) flatness ^d	RDS(on) flatness	V+ = 3 V, VCOM = 0 V to V+, INO, INC = 10 mA	Room	-	1.4	-	
RDS(on) match ^d	ΔRDS(on)	V+ = 2.7 V, VCOM = 1.5 V, INO, INC = 10 mA	Room	-	0.03	0.35	
Switch-off leakage current ^f	INO(off), INC(off)	V+ = 3.3 V, VNO, VNC = 1 V / 3 V, VCOM = 3 V / 1 V	Room	-0.4	-	0.4	nA
			Full	-4	-	4	
	ICOM(off)		Room	-0.8	-	0.8	
			Full	-8	-	8	
Channel-on leakage current ^f	ICOM(on)	V+ = 3.3 V, VNO, VNC = VCOM = 1 V / 3 V	Room	-0.8	-	0.8	nA
			Full	-8	-	8	
Digital Control							
Input high voltage	VINH		Full	2	-	-	V
Input low voltage	VINL		Full	-	-	0.4	
Input capacitance ^d	CIN		Full	-	6	-	pF
Input current	IINL or IINH	VIN = 0 V or V+	Full	-1	-	1	μA
Dynamic Characteristics							
Turn-on time ^d	tON	VNO or VNC = 2 V, RL = 300 Ω, CL = 35 pF	Room	-	13	34	ns
			Full	-	-	37	
Turn-off time ^d	tOFF		Room	-	9	20	
			Full	-	-	22	
Break-before-make time ^d	tBBM		Room	1	-	-	
Charge injection ^d	QINJ	CL = 1 nF, VGEN = 0 V, VNO, VNC = 0 V, RGEN = 0 Ω	Room	-	0.9	-	pC
Off-isolation ^d	OIRR	RL = 50 Ω, CL = 5 pF, f = 1 MHz	Room	-	-78	-	dB
Crosstalk ^d	XTALK		Room	-	-77	-	
NO, NC off capacitance ^d	CNO(off)	VIN = 0 V or V+, f = 1 MHz	Room	-	7	-	pF
	CNC(off)		Room	-	7	-	
Channel-on capacitance ^d	CON		Room	-	14	-	
Power Supply							
Power supply current ^d	I+	VIN = 0 V or V+	Full	-	0.002	1	μA



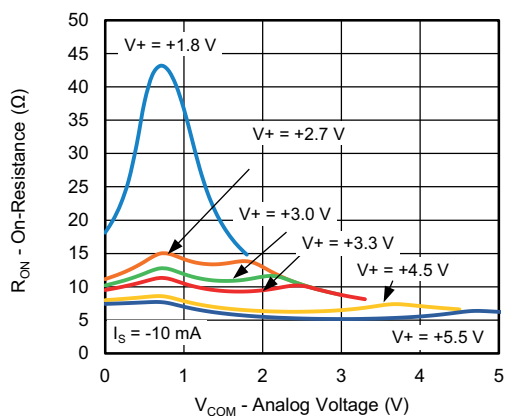
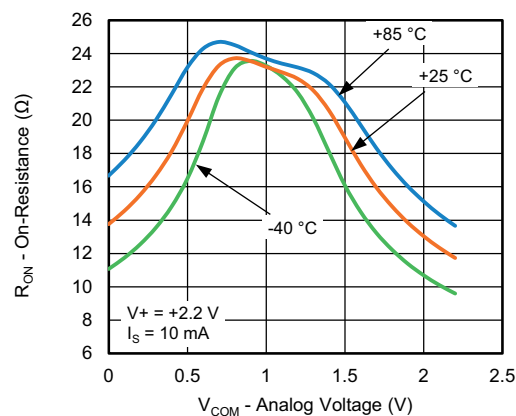
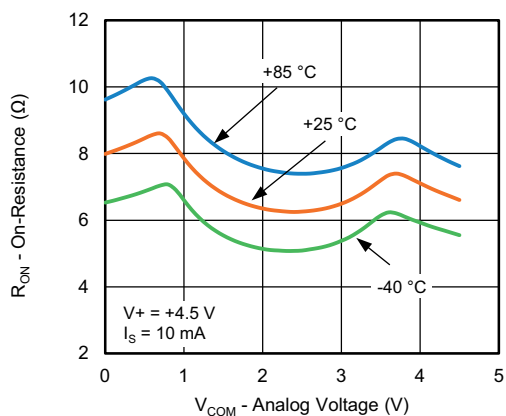
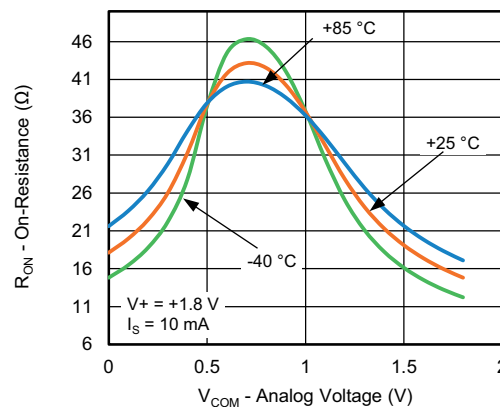
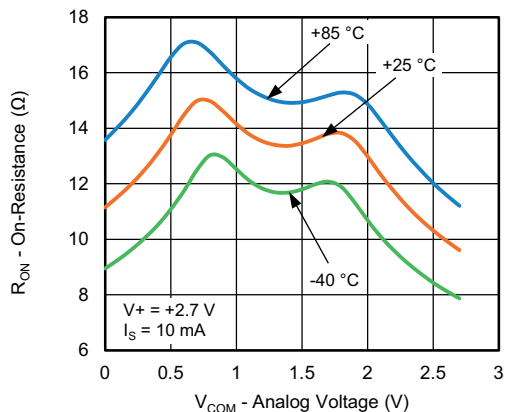
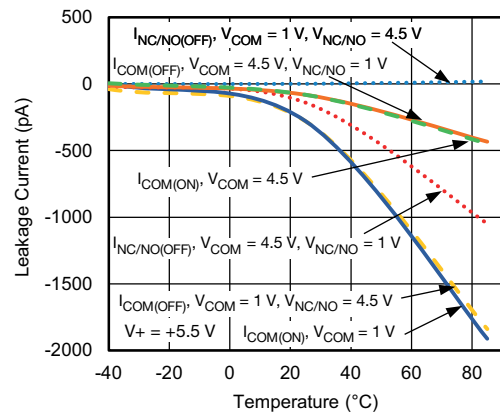
SPECIFICATIONS (V+ = 2.5 V)							
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 2.5 V, ± 10 % VIN = 0.4 V or 2 V ^e	TEMP. ^a	LIMITS -40 °C to +85 °C			UNIT
				MIN. ^b	TYP. ^c	MAX. ^b	
Analog Switch							
Analog signal range ^d	VNO, VNC VCOM		Full	0	-	V+	V
Drain-source on-resistance ^d	RDS(on)	V+ = 2.2 V, VCOM = 1 V, INO, INC = 10 mA	Room	-	23	27	Ω
			Full ^d	-	24	28	
RDS(on) flatness ^d	RDS(on) flatness	V+ = 2.5 V, VCOM = 0 V to V+, INO, INC = 10 mA	Room	-	1.7	-	
RDS(on) match ^d	ΔRDS(on)	V+ = 2.2 V, VCOM = 1.2 V, INO, INC = 10 mA	Room	-	0.1	0.5	
Switch-off leakage current ^f	INO(off), INC(off)	V+ = 2.7 V, VNO, VNC = 0.5 V / 1.5 V, VCOM = 1.5 V / 0.5 V	Room	-0.2	-	0.2	nA
			Full ^d	-3	-	3	
	ICOM(off)		Room	-0.2	-	0.2	
			Full ^d	-3	-	3	
Channel-on leakage current ^f	ICOM(on)	V+ = 2.7 V, VNO, VNC = VCOM = 0.5 V / 1.5 V	Room	-0.2	-	0.2	nA
			Full ^d	-3	-	3	
Digital Control							
Input high voltage	VINH		Full	2	-	-	V
Input low voltage	VINL		Full	-	-	0.4	
Input capacitance ^d	CIN		Full	-	6	-	pF
Input current	IINL or IINH	VIN = 0 V or V+	Full	-1	-	1	μA
Dynamic Characteristics							
Turn-on time ^d	tON	VNO or VNC = 1.5 V, RL = 300 Ω, CL = 35 pF	Room	-	16	36	ns
			Full ^d	-	-	38	
Turn-off time ^d	tOFF		Room	-	10	19	
			Full	-	-	21	
Break-before-make time ^d	tBBM		Room ^d	1	-	-	
Charge injection ^d	QINJ	CL = 1 nF, VGEN = 0 V, VNO, VNC = 0 V, RGEN = 0 Ω	Room	-	0.9	-	pC
Off-isolation ^d	OIRR	RL = 50 Ω, CL = 5 pF, f = 1 MHz	Room	-	-78	-	dB
Crosstalk ^d	XTALK		Room	-	-77	-	
NO, NC off capacitance ^d	CNO(off)	VIN = 0 V or V+, f = 1 MHz	Room	-	7	-	pF
	CNC(off)		Room	-	7	-	
Channel-on capacitance ^d	CON		Room	-	14	-	
Power Supply							
Power supply current ^d	I+	VIN = 0 V or V+	Full	-	-	1	μA

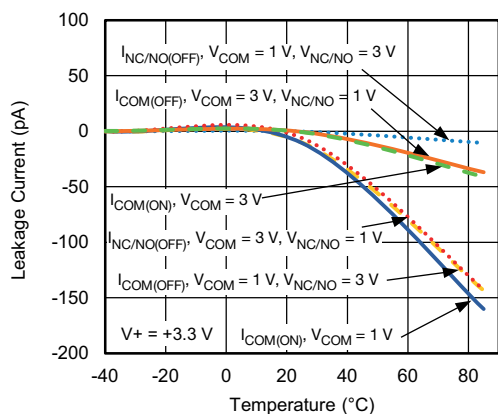
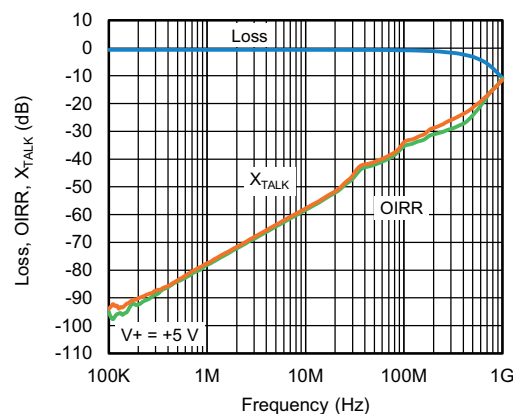
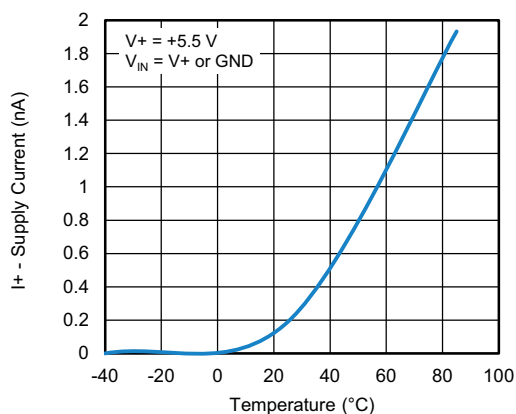
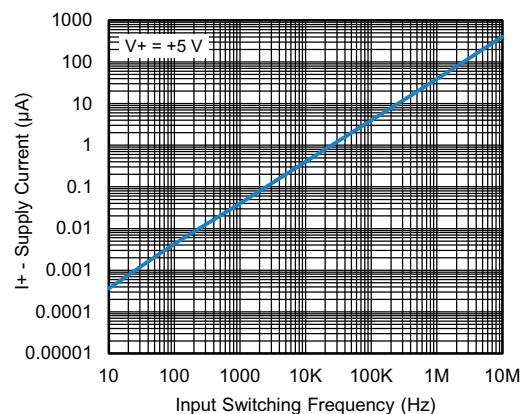
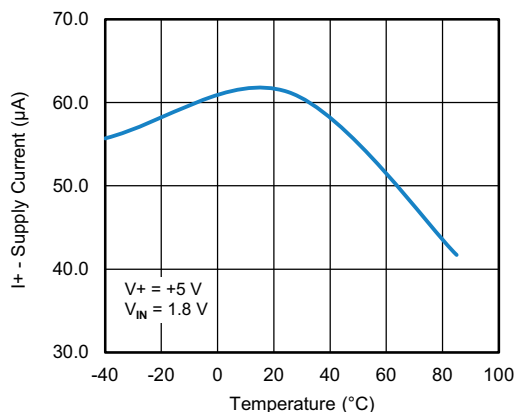
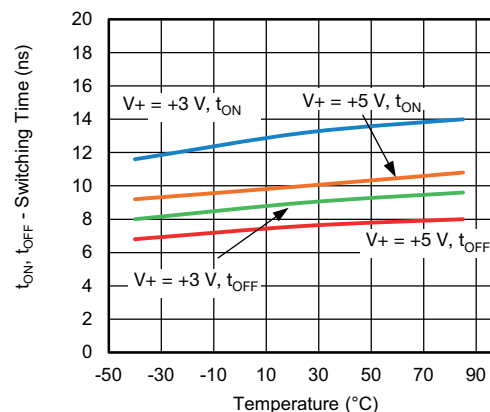


SPECIFICATIONS (V+ = 2 V)							
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 2 V, ± 10 % VIN = 0.4 V or 1.6 V ^e	TEMP. ^a	LIMITS -40 °C to +85 °C			UNIT
				MIN. ^b	TYP. ^c	MAX. ^b	
Analog Switch							
Analog signal range ^d	VNO, VNC VCOM		Full	0	-	V+	V
Drain-source on-resistance ^d	RDS(on)	V+ = 1.8 V, VCOM = 1 V, INO, INC = 10 mA	Room Full ^d	- -	37 36	42 44	Ω
RDS(on) flatness ^d	RDS(on) flatness	V+ = 2 V, VCOM = 0 V to V+, INO, INC = 10 mA	Room	-	3	-	
RDS(on) match ^d	ΔRDS(on)	V+ = 1.8 V, VCOM = 1 V, INO, INC = 10 mA	Room	-	0.04	0.5	
Switch-off leakage current ^f	INO(off), INC(off)	V+ = 2.2 V, VNO, VNC = 0.5 V / 1.5 V, VCOM = 1.5 V / 0.5 V	Room	-0.2	-	0.2	nA
			Full ^d	-3	-	3	
	ICOM(off)		Room	-0.2	-	0.2	
			Full ^d	-3	-	3	
Channel-on leakage current ^f	ICOM(on)	V+ = 2.2 V, VNO, VNC = VCOM = 0.5 V / 1.5 V	Room	-0.2	-	0.2	nA
			Full ^d	-3	-	3	
Digital Control							
Input high voltage	VINH		Full	1.6	-	-	V
Input low voltage	VINL		Full	-	-	0.4	
Input capacitance ^d	CIN		Full	-	6	-	pF
Input current	IINL or IINH	VIN = 0 V or V+	Full	-1	-	1	μA
Dynamic Characteristics							
Turn-on time ^d	tON	VNO or VNC = 1.5 V, RL = 300 Ω, CL = 35 pF	Room	-	21	40	ns
			Full ^d	-	-	42	
Turn-off time ^d	tOFF		Room	-	13	20	
			Full ^d	-	-	21	
Break-before-make time ^d	tBBM		Room	1	-	-	
Charge injection ^d	QINJ		CL = 1 nF, VGEN = 0 V, VNO, VNC = 0 V, RGEN = 0 Ω	Room	-	0.8	
Off-isolation ^d	OIRR	RL = 50 Ω, CL = 5 pF, f = 1 MHz	Room	-	-78	-	dB
Crosstalk ^d	XTALK		Room	-	-77	-	
NO, NC off capacitance ^d	CNO(off)	VIN = 0 V or V+, f = 1 MHz	Room	-	7	-	pF
	CNC(off)		Room	-	7	-	
Channel-on capacitance ^d	CON		Room	-	14	-	
Power Supply							
Power supply current ^d	I+	VIN = 0 V or V+	Full	-	-	1	μA

Notes

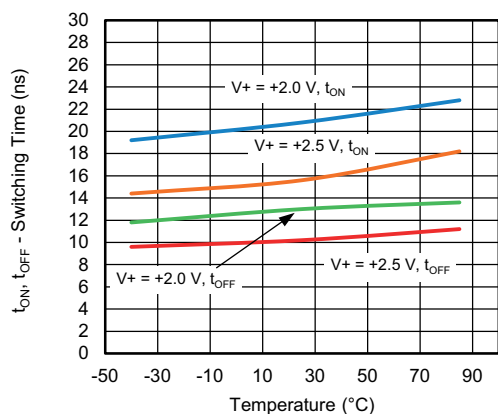
- a. Room = 25 °C, full = as determined by the operating suffix
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet
c. Typical values are for design aid only, not guaranteed nor subject to production testing
d. Guarantee by design, nor subjected to production test
e. V_{IN} = input voltage to perform proper function
f. Guaranteed by 5 V leakage testing, not production tested

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

 $R_{DS(on)}$ vs. V_{COM} and Supply Voltage

 $R_{DS(on)}$ vs. Analog Voltage and Temperature

 $R_{DS(on)}$ vs. Analog Voltage and Temperature

 $R_{DS(on)}$ vs. Analog Voltage and Temperature

 $R_{DS(on)}$ vs. Analog Voltage and Temperature

Leakage Current vs. Temperature

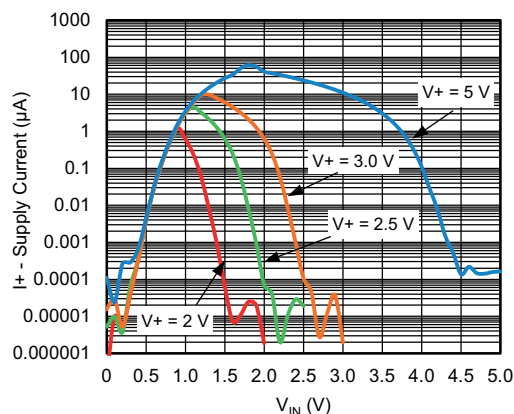
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Leakage Current vs. Temperature

Insertion Loss, Off-Isolation Crosstalk vs. Frequency

Supply Current vs. Temperature

Supply Current vs. Input Switching Frequency

Supply Current vs. Temperature

Switching Time vs. Temperature



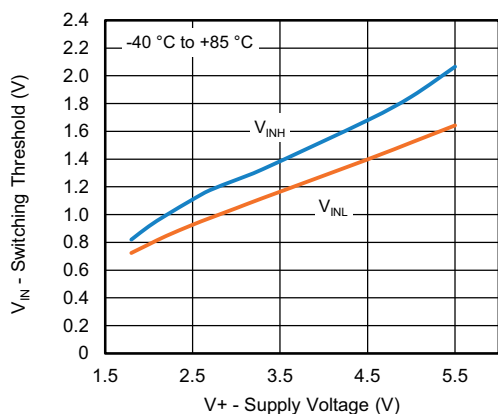
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



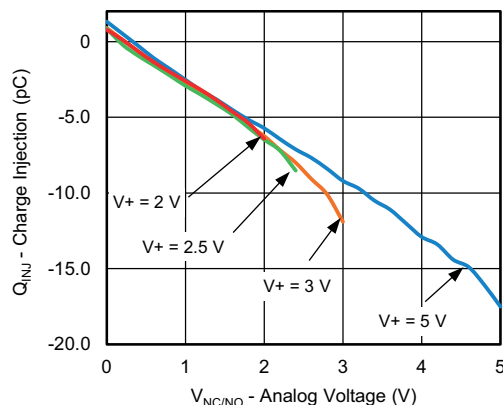
Switching Time vs. Temperature



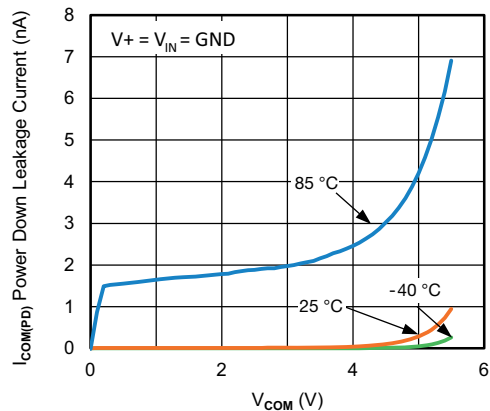
Supply Current vs. Enable Input Voltage



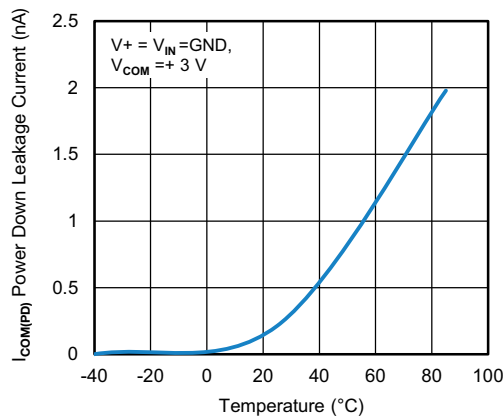
Switching Threshold vs. Supply Voltage



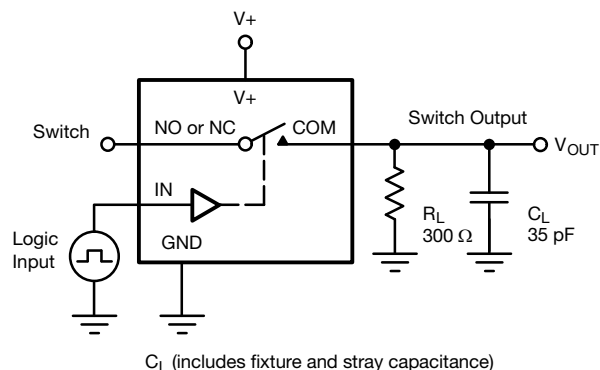
Charge Injection vs. Analog Voltage



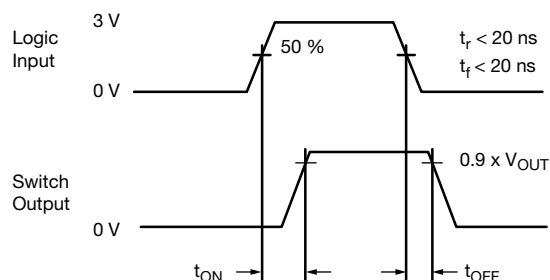
Power Down Leakage Current vs. V_{COM}



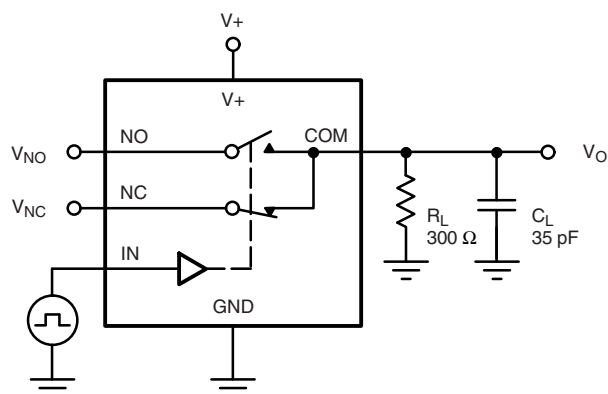
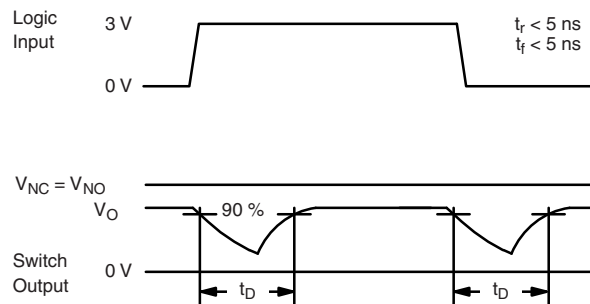
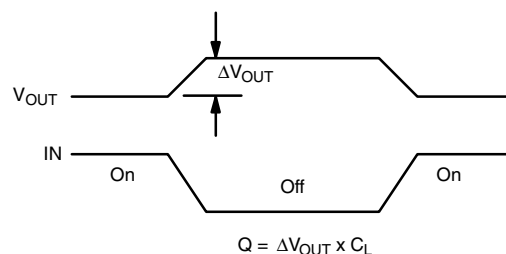
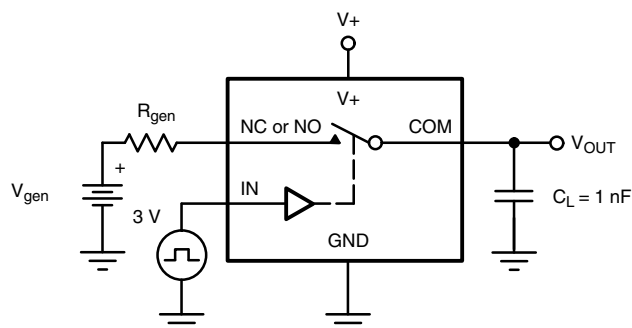
Power Down Leakage Current vs. Temperature

TEST CIRCUITS

 C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$

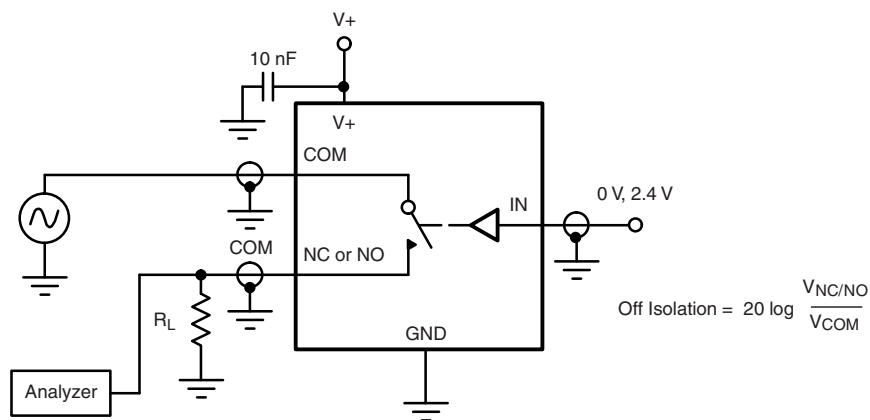
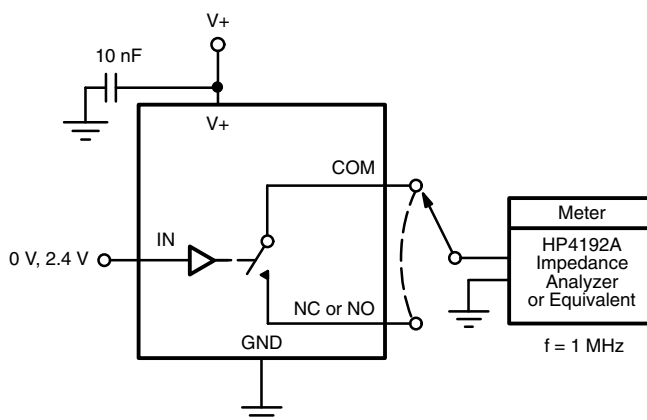


Logic "1" = switch on
Logic input waveforms inverted for switches that have the opposite logic sense.

Fig. 1 - Switching Time

 C_L (includes fixture and stray capacitance)

Fig. 2 - Break-Before-Make Interval


IN depends on switch configuration: input polarity determined by sense of switch.

Fig. 3 - Charge Injection

TEST CIRCUITS

Fig. 4 - Off-Isolation

Fig. 5 - Channel Off / On Capacitance

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