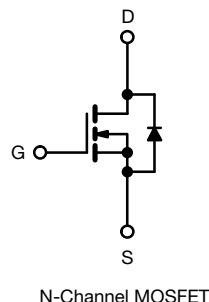
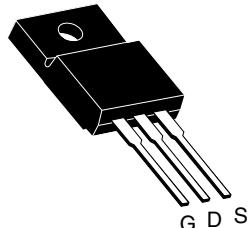


## EF Series Power MOSFET With Fast Body Diode

**TO-220 FULLPAK**

**FEATURES**

- A specific on resistance ( $m\Omega \cdot cm^2$ ) reduction of 25 %
- Low figure-of-merit (FOM)  $R_{on} \times Q_g$
- Low input capacitance ( $C_{iss}$ )
- Reduced switching and conduction losses
- Ultra low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
COMPLIANT  
HALOGEN  
FREE

**PRODUCT SUMMARY**

$V_{DS}$ (V) at $T_J$ max.	650	
$R_{DS(on)}$ typ. ( $\Omega$ ) at 25 °C	$V_{GS} = 10$ V	0.084
$Q_g$ max. (nC)	134	
$Q_{gs}$ (nC)	16	
$Q_{gd}$ (nC)	48	
Configuration	Single	

**APPLICATIONS**

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Renewable energy
  - Solar (PV inverters)

**ORDERING INFORMATION**

Package	TO-220 FULLPAK	
Lead (Pb)-free and halogen-free	SiHF35N60EF-GE3	

**ABSOLUTE MAXIMUM RATINGS** ( $T_C = 25$  °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	600	V
Gate-source voltage		$\pm 30$	
Continuous drain current ( $T_J = 150$ °C) <sup>e</sup>	$I_D$	32	A
$V_{GS}$ at 10 V		20	
Pulsed drain current <sup>a</sup>	$I_{DM}$	80	
Linear derating factor		2.0	W/°C
Single pulse avalanche energy <sup>b</sup>	$E_{AS}$	298	mJ
Maximum power dissipation	$P_D$	39	W
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C
Drain-source voltage slope	$dv/dt$	100	V/ns
Reverse diode $dv/dt$ <sup>d</sup>		50	
Soldering recommendations (peak temperature) <sup>c</sup>	For 10 s	260	°C
Mounting torque	M3 screw	0.6	Nm

**Notes**

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 140$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$  Ω,  $I_{AS} = 4.6$  A
- 1.6 mm from case
- $I_{SD} = 17$  A,  $di/dt = 300$  A/μs, starting  $T_J = 25$  °C
- Limited by maximum junction temperature

**THERMAL RESISTANCE RATINGS**

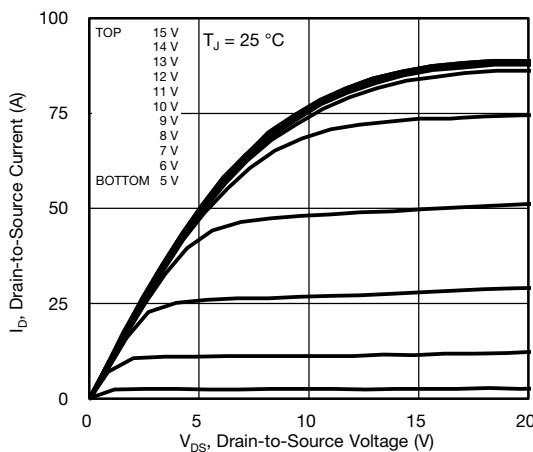
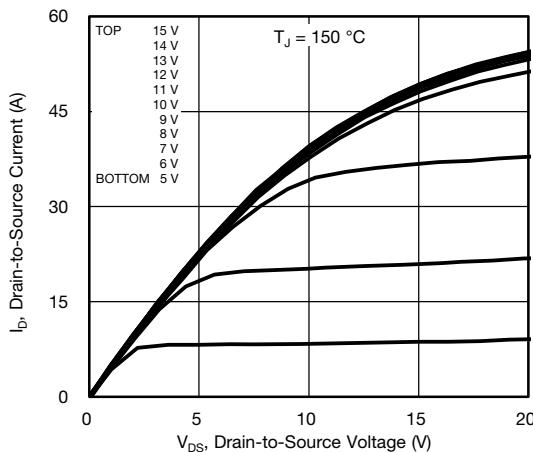
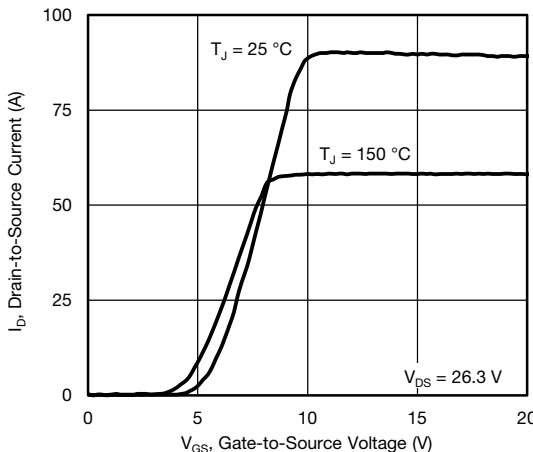
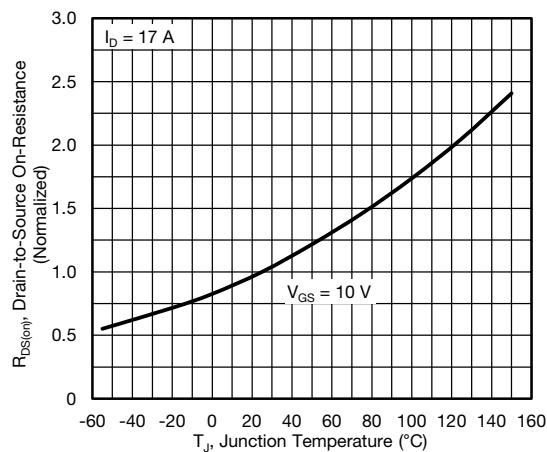
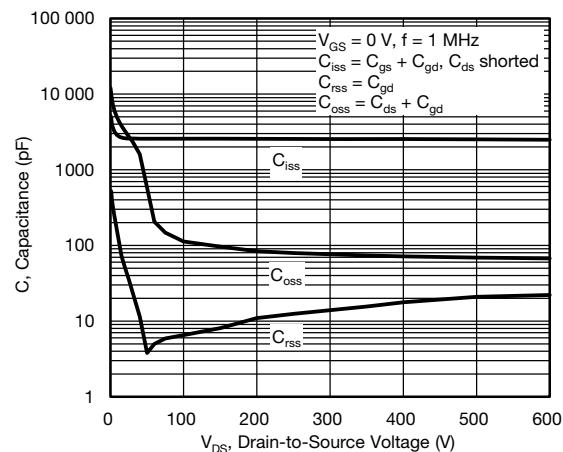
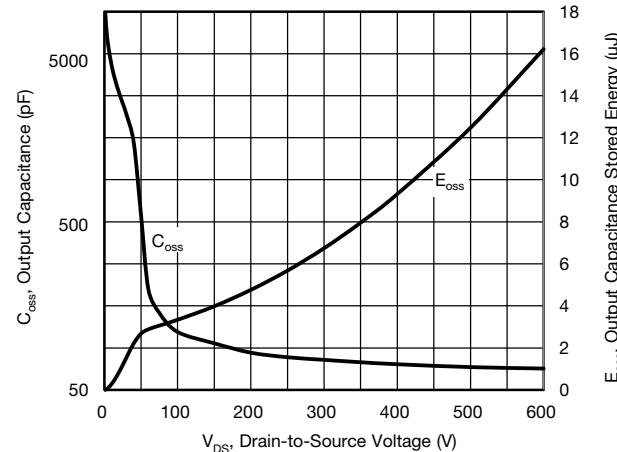
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	-	65	
Maximum junction-to-case (drain)	$R_{thJC}$	-	3.2	°C/W

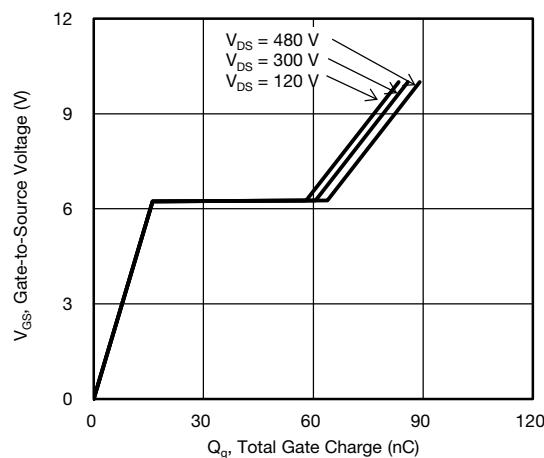
**SPECIFICATIONS (T<sub>J</sub> = 25 °C, unless otherwise noted)**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}$ , $I_D = 250 \mu\text{A}$		600	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, $I_D = 10 \text{ mA}$		-	0.66	-	V/°C
Gate-source threshold voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250 \mu\text{A}$		2.0	-	4.0	V
Gate-source leakage	$I_{GSS}$	$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
		$V_{GS} = \pm 30 \text{ V}$		-	-	± 1	μA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 480 \text{ V}$ , $V_{GS} = 0 \text{ V}$		-	-	1	
		$V_{DS} = 480 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $T_J = 125 \text{ °C}$		-	-	500	μA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$	$I_D = 17 \text{ A}$	-	0.084	0.097	Ω
Forward transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 30 \text{ V}$ , $I_D = 17 \text{ A}$		-	8	-	S
<b>Dynamic</b>							
Input capacitance	$C_{iss}$	$V_{GS} = 0 \text{ V}$ , $V_{DS} = 100 \text{ V}$ , $f = 1 \text{ MHz}$		-	2568	-	pF
Output capacitance	$C_{oss}$			-	113	-	
Reverse transfer capacitance	$C_{rss}$			-	7	-	
Effective output capacitance, energy related <sup>a</sup>	$C_{o(er)}$	$V_{DS} = 0 \text{ V}$ to 480 V, $V_{GS} = 0 \text{ V}$		-	81	-	pF
Effective output capacitance, time related <sup>b</sup>	$C_{o(tr)}$			-	421	-	
Total gate charge	$Q_g$			-	89	134	nC
Gate-source charge	$Q_{gs}$	$V_{GS} = 10 \text{ V}$	$I_D = 17 \text{ A}$ , $V_{DS} = 480 \text{ V}$	-	16	-	
Gate-drain charge	$Q_{gd}$			-	48	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 480 \text{ V}$ , $I_D = 17 \text{ A}$ , $V_{GS} = 10 \text{ V}$ , $R_g = 9.1 \Omega$		-	28	56	ns
Rise time	$t_r$			-	85	170	
Turn-off delay time	$t_{d(off)}$			-	96	192	
Fall time	$t_f$			-	61	122	
Gate input resistance	$R_g$	$f = 1 \text{ MHz}$ , open drain		0.2	0.5	1.0	Ω
<b>Drain-Source Body Diode Characteristics</b>							
Continuous source-drain diode current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	32	A
Pulsed diode forward current	$I_{SM}$			-	-	80	
Diode forward voltage	$V_{SD}$	$T_J = 25 \text{ °C}$ , $I_S = 17 \text{ A}$ , $V_{GS} = 0 \text{ V}$		-	-	1.2	V
Reverse recovery time	$t_{rr}$	$T_J = 25 \text{ °C}$ , $I_F = I_S = 17 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_R = 400 \text{ V}$		-	150	300	ns
Reverse recovery charge	$Q_{rr}$			-	1.1	2.2	μC
Reverse recovery current	$I_{RRM}$			-	14	-	A

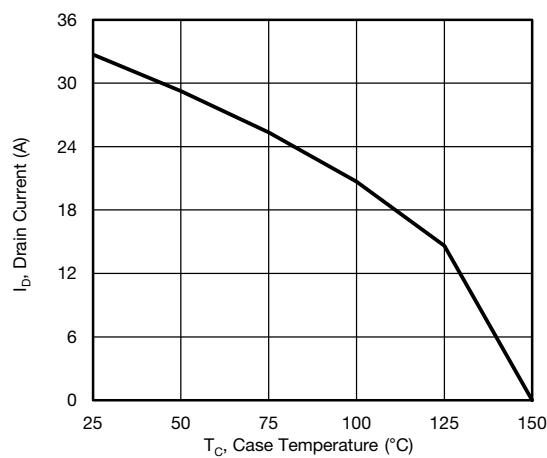
**Notes**

a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$   
b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$

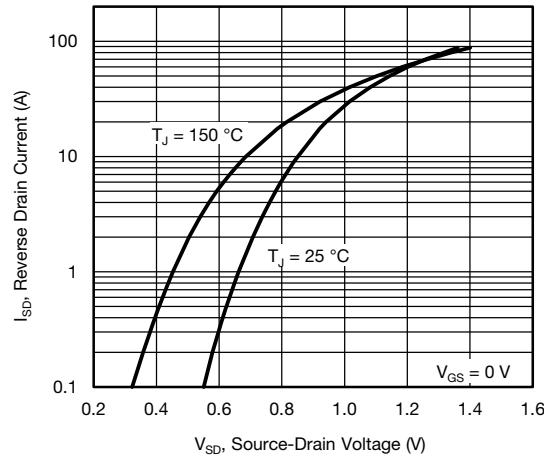
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics**

**Fig. 2 - Typical Output Characteristics**

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 4 - Normalized On-Resistance vs. Temperature**

**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 6 -  $C_{oss}$  and  $E_{oss}$  vs.  $V_{DS}$**



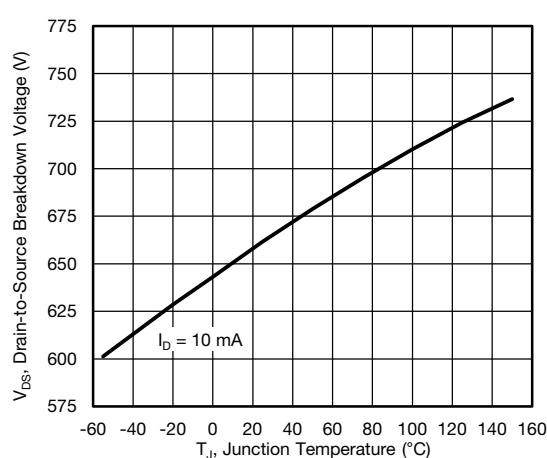
**Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage**



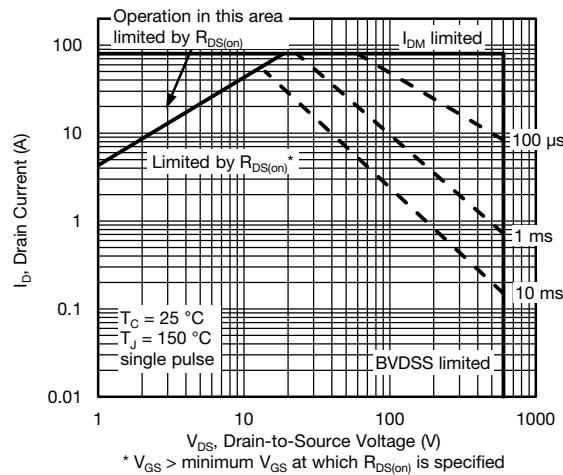
**Fig. 10 - Maximum Drain Current vs. Case Temperature**



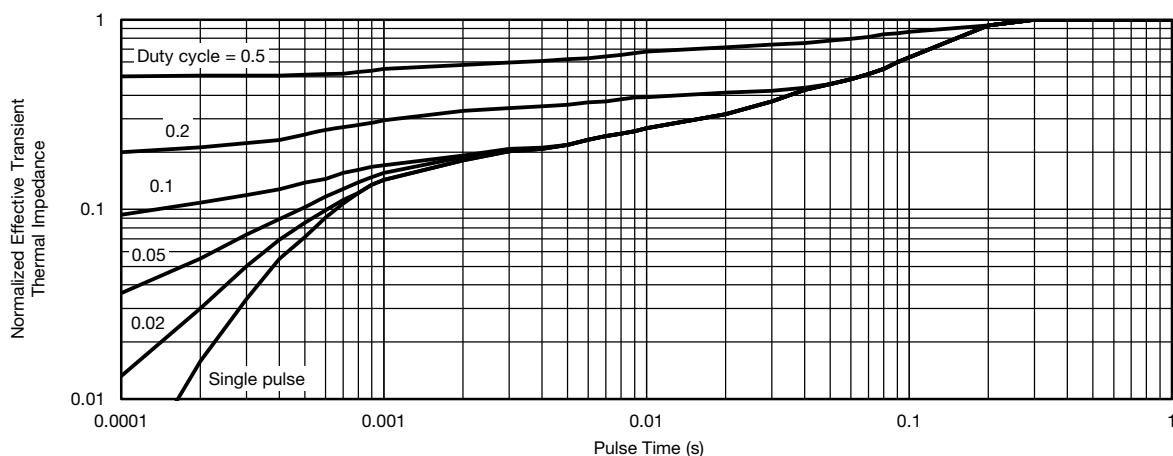
**Fig. 8 - Typical Source-Drain Diode Forward Voltage**



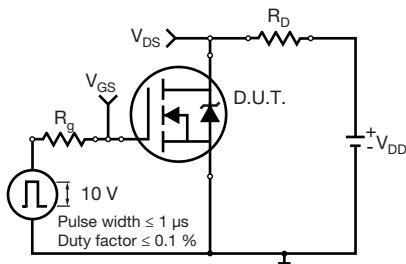
**Fig. 11 - Temperature vs. Drain-to-Source Voltage**



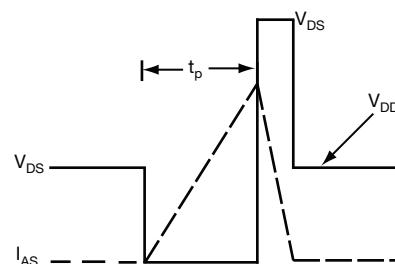
**Fig. 9 - Maximum Safe Operating Area**



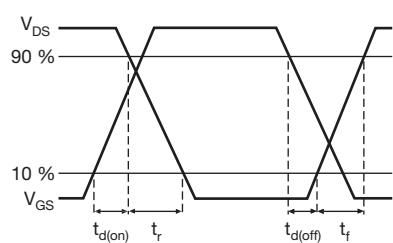
**Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case**



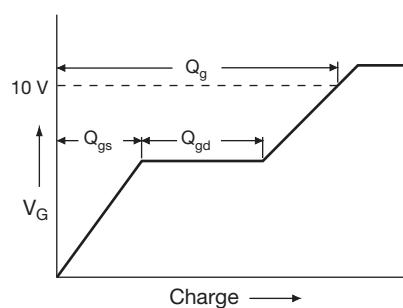
**Fig. 13 - Switching Time Test Circuit**



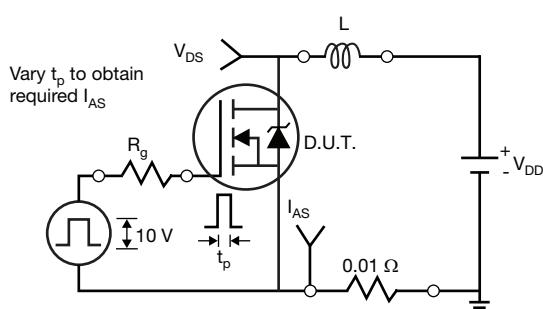
**Fig. 16 - Unclamped Inductive Waveforms**



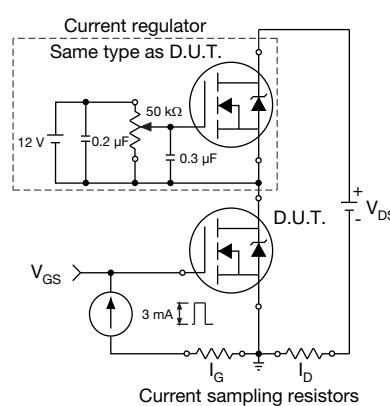
**Fig. 14 - Switching Time Waveforms**



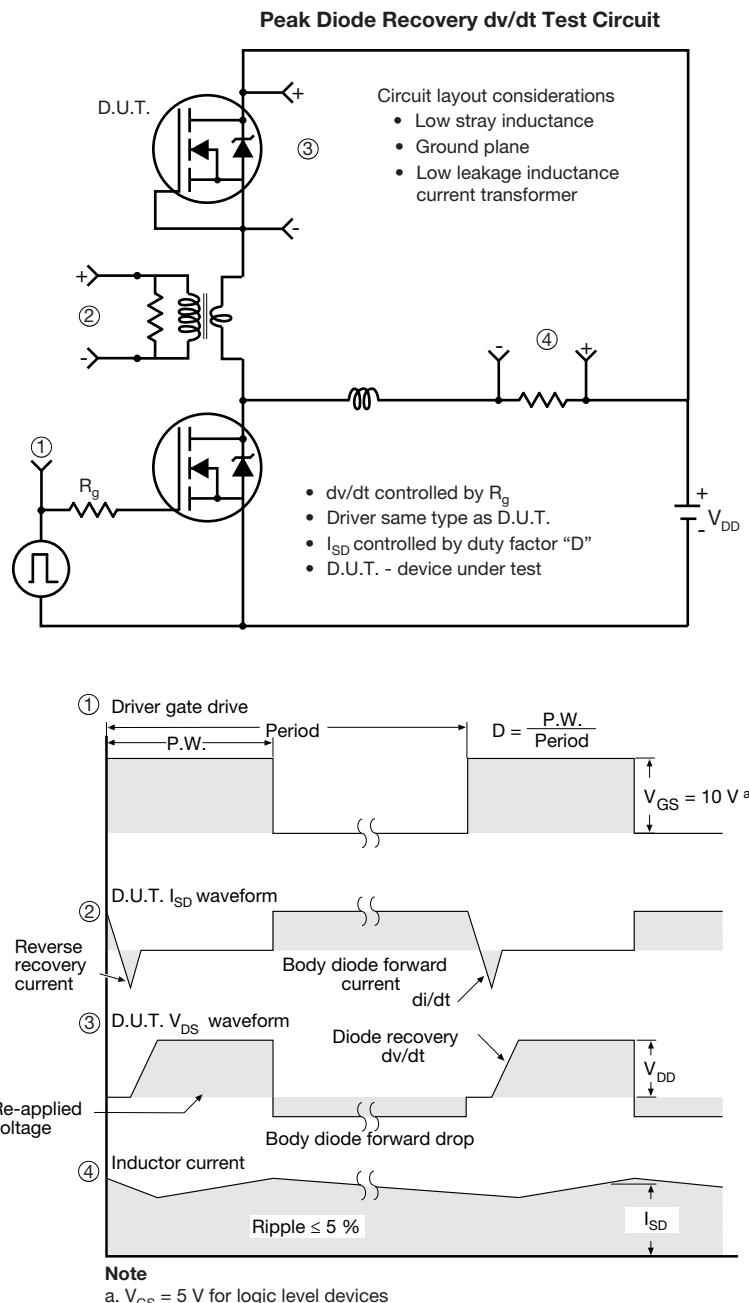
**Fig. 17 - Basic Gate Charge Waveform**



**Fig. 15 - Unclamped Inductive Test Circuit**



**Fig. 18 - Gate Charge Test Circuit**



**Fig. 19 - For N-Channel**



[www.vishay.com](http://www.vishay.com)

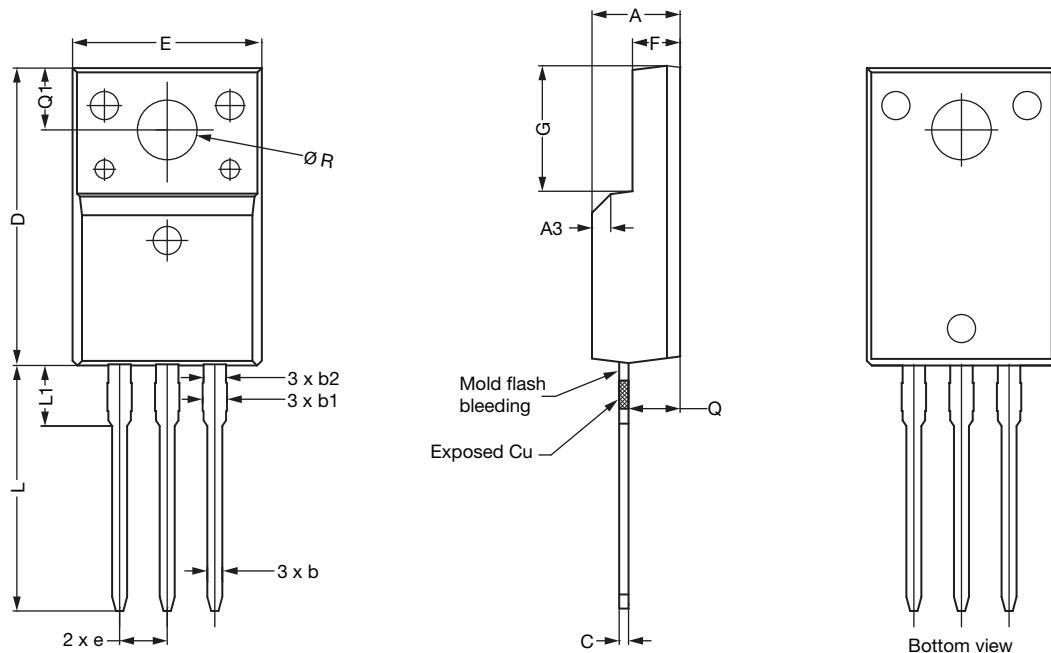
**SiHF35N60EF**

Vishay Siliconix

*Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?92110](http://www.vishay.com/ppg?92110).*

## TO-220 FULLPAK (High Voltage)

### OPTION 1: FACILITY CODE = 9

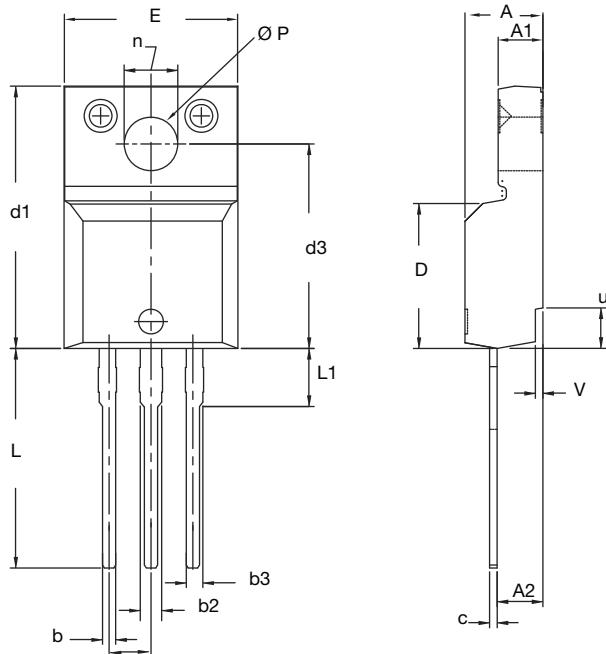


MILLIMETERS			
DIM.	MIN.	NOM.	MAX.
A	4.60	4.70	4.80
b	0.70	0.80	0.91
b1	1.20	1.30	1.47
b2	1.10	1.20	1.30
C	0.45	0.50	0.63
D	15.80	15.87	15.97
e	2.54 BSC		
E	10.00	10.10	10.30
F	2.44	2.54	2.64
G	6.50	6.70	6.90
L	12.90	13.10	13.30
L1	3.13	3.23	3.33
Q	2.65	2.75	2.85
Q1	3.20	3.30	3.40
Ø R	3.08	3.18	3.28

#### Notes

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet  $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1<sup>st</sup> character located at the 2<sup>nd</sup> row of the unit marking

### OPTION 2: FACILITY CODE = Y



	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
$\varnothing P$	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
V	0.400	0.500	0.016	0.020

ECN: E19-0180-Rev. D, 08-Apr-2019  
 DWG: 5972

#### Notes

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2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet  $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1<sup>st</sup> character located at the 2<sup>nd</sup> row of the unit marking

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