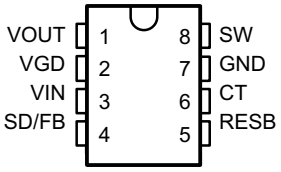
LOW-POWER SYNCHRONOUS BOOST CONVERTER

FEATURES

- **1 V Input Voltage Operation Start-Up Ensured Under Full Load on Main Output, and Operation Down to 0.5 V**
- **200 mW Output Power at Battery Voltages as Low as 0.8 V**
- **Secondary 7 V Supply from a Single Inductor**
- **Output Fully Disconnected in Shutdown**
- **Adaptive Current Mode Control for Optimum Efficiency**
- **High Efficiency Over Wide Operating Range**
- **6 µA Shutdown Supply Current**
- **Output Reset Function with Programmable Reset Period**

PW PACKAGE
(TOP VIEW)

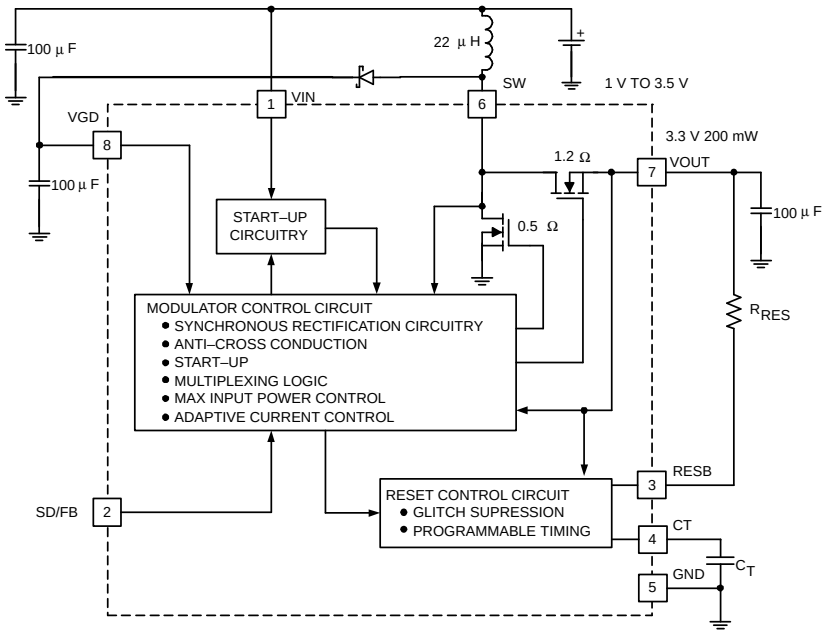
D PACKAGE
(TOP VIEW)



DESCRIPTION

The UCCx9411 family of low-input voltage, single-inductor-boost converters is optimized to operate from a single or dual alkaline cell, and steps up to a 3.3 V, 5 V, or adjustable output at 200 mW. The UCCx9411 family also provides an auxiliary 7 V output, primarily for the gate-drive supply, which can be used for applications requiring an auxiliary output, such as 5 V, by linear regulating. The primary output starts up under full load at input voltages typically as low as 0.8 V with a ensured max of 1 V, and operates down to 0.5 V once the converter is operating, thereby maximizing battery usage.

SIMPLIFIED BLOCK DIAGRAM AND APPLICATION CIRCUIT



A. Pinout shown is for the TSSOP Package. Consult Package Descriptions for the SOIC configurations.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The UCCx9411 family is designed to accommodate demanding applications such as pagers and cell phones that require high efficiency over a wide operating range of several milliwatts to a couple of hundred milli-watts. High efficiency at low output current is achieved by optimizing switching and conduction losses with a low total quiescent current. At higher output current, the 0.5 Ω switch and 1.2 Ω synchronous rectifier along with continuous mode conduction provide high power efficiency. The wide input voltage range of the UCCx9411 family can accommodate other power sources such as NiCd and NiMH.

The UCCx9411 family also provides shutdown control. Packages available are the 8-pin SOIC (D) and 8-pin TSSOP (PW) to optimize board space.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)(2)

		VALUE/UNIT
VIN	Input voltage	–0.3 V to 10 V
SD	Input voltage	–0.3 V to V_{IN}
VGD	Input voltage	–0.3 V to 14 V
SW	Input voltage	–0.3 V to 15 V
V_{OUT}	Output voltage	–0.3 V to 10 V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Currents are positive into, negative out of the specific terminal. Consult Packaging Section of the *Portable Products Data Book* (SLUD001) for thermal limitations and considerations of packages.

available options

T_J	PACKAGE PW(1)			PACKAGE D(1)		
	OUTPUT VOLTAGE			OUTPUT VOLTAGE		
	ADJ	3.3 V	5 V	ADJ	3.3 V	5 V
–40°C to 85°C	29411PW	29412PW	29413PW	29411D	29412D	29413D
0°C to 70°C	39411PW	39412PW	39413PW	39411D	39412D	39413D

(1) The UCC39411, UCC39412 and UCC39413 is avilable in tape and reel. Add TR suffix to device type (e.g. UCC39411PWTR or UCC39411DTR) to order quantities of 2000 devices per reel (PW package) or 2500 devices per reel (D package).

ELECTRICAL CHARACTERISTICS

T_J = 0°C to 70°C for the UCC3941x, T_J = –40°C to 85°C for the UCC2941x, V_{IN} = 1.25 V for UCC39411, UCC39412, V_{IN} = 2.5 V for the UCC39413, $T_A = T_J$

PARAMETER	TEST CONDITIONS	UCC3941x			UCC2941x			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT VOLTAGE SECTION								
Minimum start-up voltage	No external VGD load, T_J = 25°C, I_{OUT} = 60 mA(1)		0.8	1		0.8	1	V
	No external VGD load, I_{OUT} = 60 mA(1)		0.9	1.1		1.2	1.4	V
Minimum dropout voltage	No external VGD load, I_{OUT} = 10 mA(1)			0.5			0.7	V
Input voltage range		1.1		3.2	1.3		3.2	V
Quiescent supply current	See (2)		6	12		8	16	µA

(1) Ensured by design. Not production tested.
(2) For the UCC39411 FB = 1.306 V, VGD = 7.7 V, For the UCC39412 V_{OUT} = 3.5 V and VGD = 7.7 V, For the UCC39413 V_{OUT} = 5.3 V, VGD=9.3 V.

ELECTRICAL CHARACTERISTICS (continued)

T_J = 0°C to 70°C for the UCC3941x, T_J = –40°C to 85°C for the UCC2941x, V_{IN} = 1.25 V for UCC39411, UCC39412, V_{IN} = 2.5 V for the UCC39413, $T_A = T_J$

PARAMETER	TEST CONDITIONS	UCC3941x			UCC2941x			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply current at shutdown	SD = GND		6	12		8	16	µA
OUTPUT SECTION								
Quiescent supply current	See (2)		15	28		20	37	µA
Supply current at shutdown	SD = GND		3	6		5	10	µA
Regulation voltage (UCC39412)	1 V < V_{IN} < 3 V	3.2	3.3	3.39	3.15	3.3	3.45	V
	1 V < V_{IN} < 3 V, 0 mA < I_{OUT} < 60 mA(1)	3.17	3.3	3.43	3.11	3.3	3.5	V
Regulation voltage (UCC39413)	1 V < V_{IN} < 5 V	4.85	5	5.15	4.78	5	5.23	V
	1 V < V_{IN} < 5 V, 0 mA < I_{OUT} < 60 mA(1)	4.8	5	5.2	4.71	5	5.3	V
ADJ voltage (UCC39411)	1 V < V_{IN} < 3 V	1.212	1.25	1.288	1.194	1.25	1.306	V
Maximum output voltage (UCCx9411)				5.5			5.5	V
VGD OUTPUT SECTION								
Quiescent supply current	See (2)		20	40		27	55	µA
Supply current at shutdown	SD = GND		20	40		27	55	µA
Regulation voltage (UCC39411/2)	1 V < V_{IN} < 3 V	6.3	7	7.7	6.3	7	7.7	V
	1 V < V_{IN} < 3 V, 0 mA < I_{OUT} < 10 mA(1)	6.3	7	7.7	6.3	7	7.7	V
Regulation voltage (UCC39413)	1 V < V_{IN} < 5 V	7.7	8.5	9.3	7.7	8.5	9.3	V
	1 V < V_{IN} < 5 V, 0 mA < I_{OUT} < 10 mA(3)	7.7	8.5	9.3	7.7	8.5	9.3	V
INDUCTOR CHARGING SECTION (L = 22 µH)								
Peak discontinuous current	Operating range, L = 22 µH	180	250	300	180	250	300	mA
Peak continuous current		385	550	715	385	550	715	mA
Charge switch $R_{DS(on)}$	D package		0.5	0.75		0.6	0.85	Ω
Current limit delay	See (3)		50			50		ns
SYNCHRONOUS RECTIFIER SECTION								
Rectifier $R_{DS(on)}$	D package		1.2	1.8		1.4	2.16	Ω
SHUTDOWN SECTION								
Threshold		0.4	0.6	0.8	0.2	0.6	0.9	V
Input bias current	SD = GND	2	5	15	2	5	15	µA
	SD = 1.25 V		5	20		20	100	nA
RESET SECTION								
Threshold (UCC39411)		1.08	1.125	1.17	1.07	1.125	1.18	V
Threshold (UCC39412)		2.85	2.97	3.09	2.83	2.97	3.11	V
Threshold (UCC39413)		4.32	4.5	4.68	4.3	4.5	4.7	V
Reset period	C_T = 0.15 µF	113	188	300	94	188	300	ms
V_{OUT} to reset delay	V_{OUT} falling at -1 mV/µs(3)		60			60		µs
Sink current		1	20		1	20		mA
Output low voltage	I_{OUT} = 500 µA			0.1			0.1	V
Output leakage				0.5			0.5	µA

(3) Ensured by design. Not production tested.

PIN ASSIGNMENTS

VIN: Input voltage to supply the IC during start-up. After the output is running the IC draws power from VOUT or VGD.

SW: An inductor is connected between this pin and VIN. The VGD (gate drive supply) flyback diode is also connected to this pin. When servicing the main output supply this pin pulls low, charging the inductor, then shuts off dumping the energy through the synchronous rectifier to the output. When servicing the VGD supply, the internal synchronous rectifier stays off and the energy is diverted to VGD through the flyback diode. During discontinuous portions of the inductor current, a MOSFET resistively connects VIN to SW damping excess circulating energy to eliminate undesired high-frequency ringing.

VGD: The VGD pin, which is coarsely regulated around 7 V (8.5 V for the UCC39413), is primarily used for the gate drive supply for the power switches in the IC. This pin can be loaded with up to 10 mA as long as it does not present a load at voltages below 2 V (this ensures proper start-up of the IC). The VGD supply can go as low as 6.3 V without interfering with the servicing of the main output. When below 6.3 V, VGD has the highest priority.

VOUT: Main output voltage (3.3 V, 5 V, or adjustable), has highest priority in the multiplexing scheme, as long as VGD is above the critical level of 6.3 V. Startup at full load is achievable at input voltages down to 1 V.

CT: This pin provides the timer for determining the reset period. The period is controlled by placing a capacitor to ground of value $C = (0.81e^{-6}) \times t$ where t is the desired reset period.

RESB: This pin provides an active low signal to alert the user when the main output voltage falls below 10% of its targeted value. The open-drain output can be used to reset a microcontroller that may be powered off of the main output voltage.

SD/FB: For the UCC39411, this pin is used to adjust the output voltage via a resistive divider from VOUT. It also serves as the shutdown pin for all three versions. Pulling this pin low provides a shutdown signal to the IC.

GND: Ground of the IC.

APPLICATION INFORMATION

OPERATION

A detailed block diagram of the UCC39411 is shown in Figure 1. Unique control circuitry provides high-efficiency power conversion for both light and heavy loads by transitioning between discontinuous and continuous conduction based on load conditions. Figure 2 depicts converter waveforms for the application circuit shown in Figure 3. A single 22µH inductor provides the energy pulses required for a highly efficient 3.3 V converter at up to 200 mW output power.

At time t1, the 3.3 V output voltage has dropped below its lower threshold, and the inductor is charged with an on time determined by: t_{ON} = 5.5 µs/VIN. For a 1.25 V input and a 22 µH inductor, the resulting peak current is approximately 250 mA. At time t2, the inductor begins to discharge with a minimum off time of approximately 1 ms. Under lightly loaded conditions, the amount of energy delivered in this single pulse satisfies the voltage-control loop, and the converter does not command any more energy pulses until the output again drops below the lower-voltage threshold.

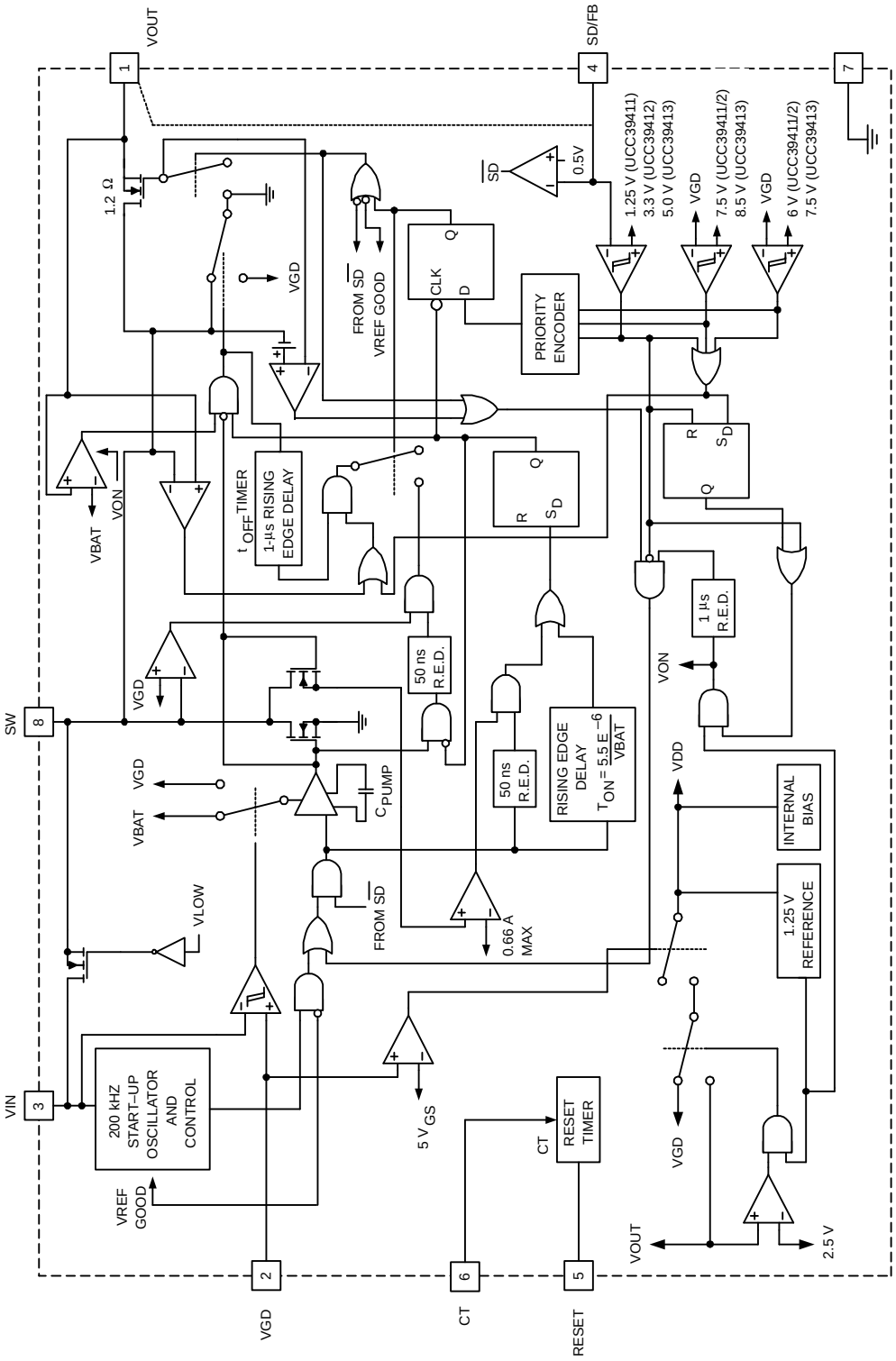
At time t3, the VGD supply drops below its lower threshold, but the output voltage is still above its threshold point. This results in an energy pulse to the gate-drive supply at t4. In some cases, a single pulse supplied to VGD is insufficient to raise the VGD voltage level enough to satisfy the voltage loop. Under this condition, multiple pulses are supplied to VGD. Note that when the UCC3941x is servicing VGD only, the IC maintains a discontinuous mode of operation. After time t4, the 3.3 V output drops below its threshold and requests to be serviced once the VGD cycle has completed, which occurs at time t5.

Time t6 represents a transition between light load and heavy load. A single energy pulse is not sufficient to force the output voltage above its upper threshold before the minimum off time has expired and a second charge cycle is commanded. Since the inductor current does not reach zero in this case, the peak current is greater than 250 mA at the end of the next charge on time. The result is a ratcheting of inductor current until either the output voltage is satisfied, or the converter reaches its set current limit. At time t7, the gate drive voltage has dropped below its 7 V threshold but the converter continues to service the output because it has higher priority unless VGD drops below about 6.3 V.

Between time t7 and t8, the converter reaches its peak current limit.

Once the peak current is reached, the converter operates in continuous mode with approximately 60 mA of inductor current ripple. At time t8, the 3.3 V output is satisfied and the converter can service the gate drive voltage, VGD, which occurs at time t9.

APPLICATION INFORMATION (continued)



A. Switches are shown in the low state. Pinouts as shown is for the 8-pin D package (SOIC). See package description for 8-pin PW (TSSOP).

Figure 1. Low Power Synchronous Boost

APPLICATION INFORMATION (continued)

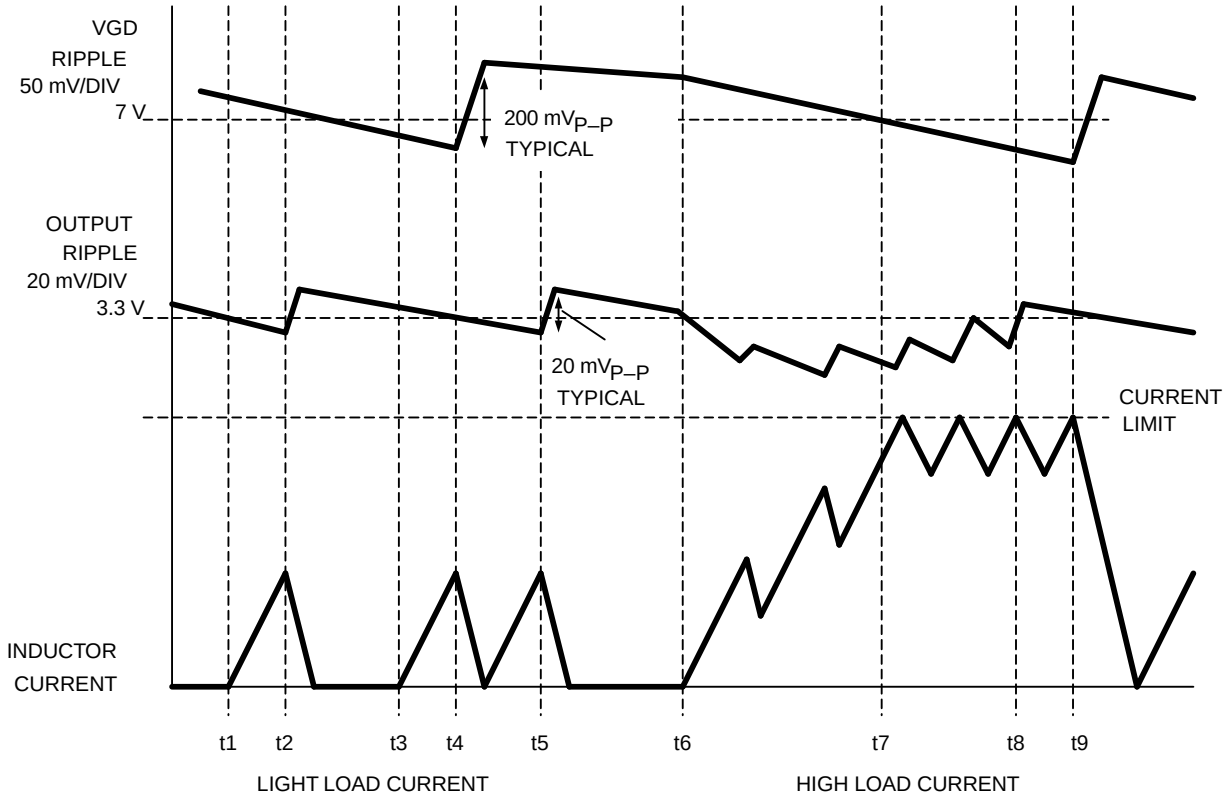
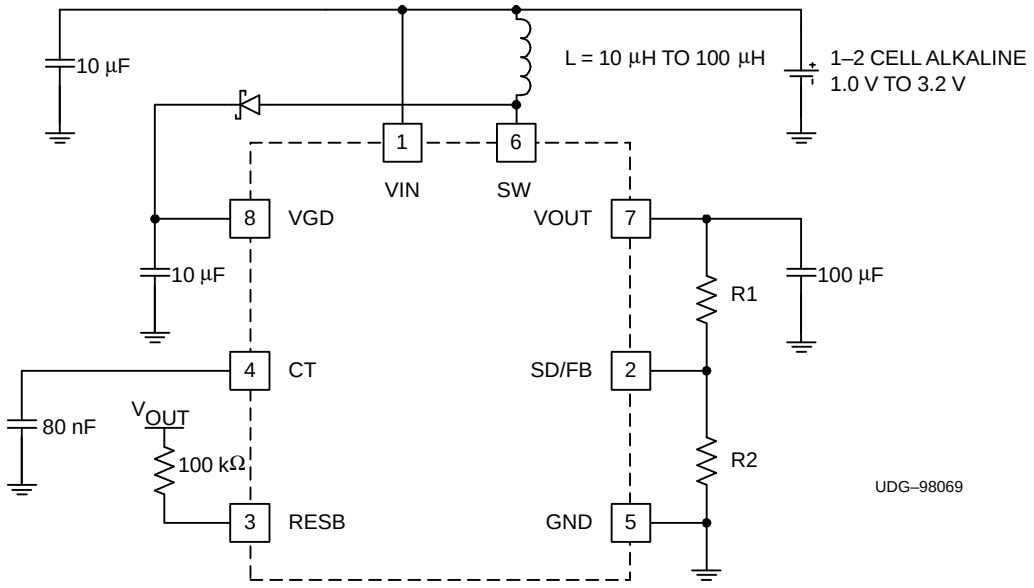


Figure 2. Inductor Current and Output Ripple Waveforms



A. Pinout shown is for the TSSOP package. Consult Package Description for the SOIC configuration.

Figure 3. Low Power Synchronous Boost Converter ADJ Version -200 mW

SHUTDOWN CONTROL

Shutdown of the UCC3941x is controlled via the interface with the SD/FB pin. Pulling the SD/FB pin low, for all

APPLICATION INFORMATION (continued)

versions, causes the IC to go into shutdown. In the UCC39412 and UCC39413, the SD/FB pin is used solely as a shutdown function. Therefore, the SD/FB pin for the UCC39412 and UCC39413 can be directly controlled using conventional CMOS or transistor to transistor logic (TTL) technology. For the UCC39411, interface into the SD/FB is slightly more complicated due to the added feedback function. When feeding back the output voltage to the SD/FB pin on the UCC39411, the IC requires a Thevenin impedance of at least 200 kΩ (500 kΩ for industrial/military applications) to ground. Then, to accomplish shutdown of the IC, an open-drain device may be used.

COMPONENT SELECTION INDUCTOR SELECTION

An inductor value of 22 µH works well in most applications, but values between 10 µH to 100 µH are also acceptable. Lower value inductors typically offer lower ESR and smaller physical size. Due to the nature of the *bang-bang* controllers, larger inductor values typically result in larger overall voltage ripple, because once the output voltage level is satisfied the converter goes discontinuous, resulting in the residual energy of the inductor causing overshoot.

It is recommended to keep the ESR of the inductor below 0.15 Ω for 200 mW applications.

OUTPUT CAPACITOR SELECTION

Once the inductor value is selected, the capacitor value determines the ripple of the converter. The worst case peak-to-peak ripple of a cycle is determined by two components, one is due to the charge storage characteristic, and the other is the ESR of the capacitor. The worst case ripple occurs when the inductor is operating at max current and is expressed as follows:

$$\Delta V = \frac{\left(I_{CL}\right)^2 L}{2C\left(V_O - V_I\right)} + I_{CL} C_{ESR} \quad (1)$$

- I_{CL} = the peak inductor current = 550 mA
- ΔV = Output ripple
- V_O = Output voltage
- V_I = Input voltage
- C_{ESR} = ESR of the output capacitor

INPUT CAPACITOR SELECTION

Since the UCCx9411 family does not require a large decoupling capacitor on the input voltage to operate properly, a 10 µF cap is sufficient for most applications. Optimum efficiency occurs when the capacitor value is large enough to decouple the source impedance, this usually occurs for capacitor values in excess of 100 µF.

RESET OPERATION

A reset function is provided to prevent the microprocessor from executing code during undervoltage conditions, typically during power up or power down. The reset voltage threshold is fixed at 90% of the output voltage for all versions of the UCCx941x. To prevent erratic operation in noisy environments, a glitch filter is provided.

To allow sufficient time for the microprocessor clock to stabilize, a user-programmable reset period is provided. The reset period, the time from the output voltage rising above 90% of nominal to RESB going high, is programmed via an external capacitor connected to the CT pin.

The reset period is defined as:

$t_{RP} = C \times 1.25$

where C is in µF, and t_{RP} is in seconds.

A typical reset profile during power up is shown in Figure 4 and power down in Figure 5.

TYPICAL CHARACTERISTICS

POWER-UP SEQUENCE

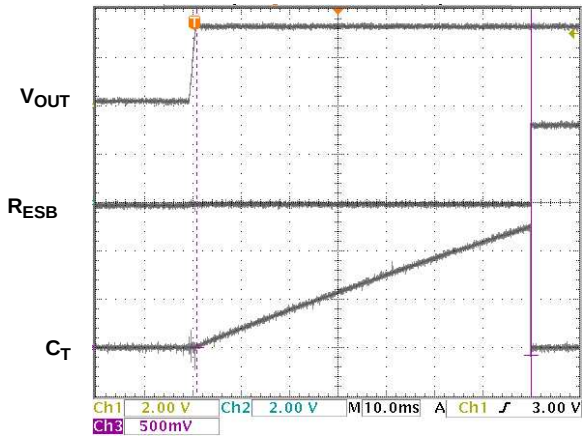


Figure 4.

POWER-DOWN SEQUENCE

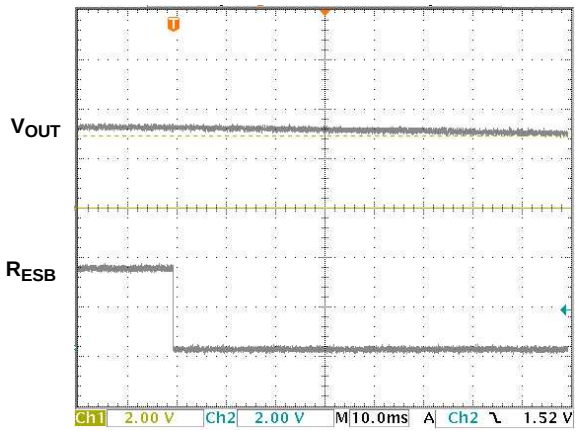


Figure 5.

TYPICAL EFFICIENCY vs LOAD CURRENT

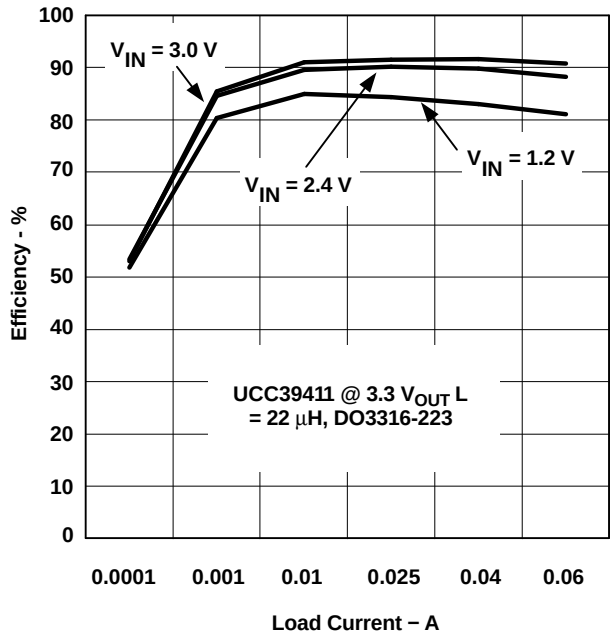


Figure 6.

TYPICAL EFFICIENCY vs LOAD CURRENT

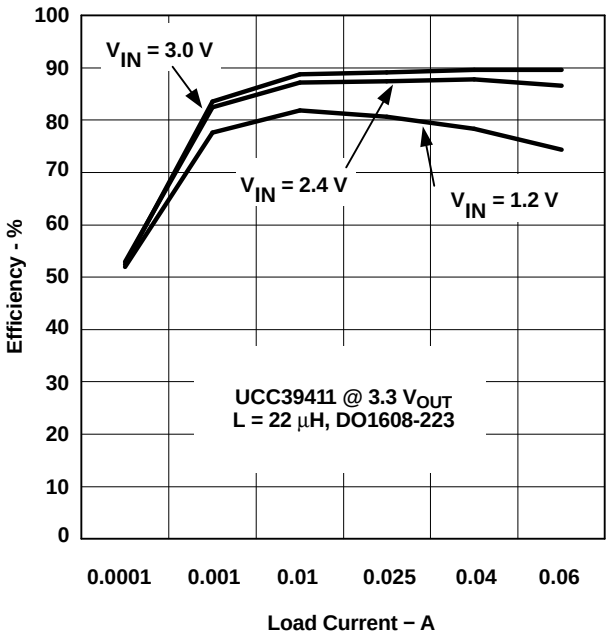


Figure 7.

TYPICAL CHARACTERISTICS (continued)

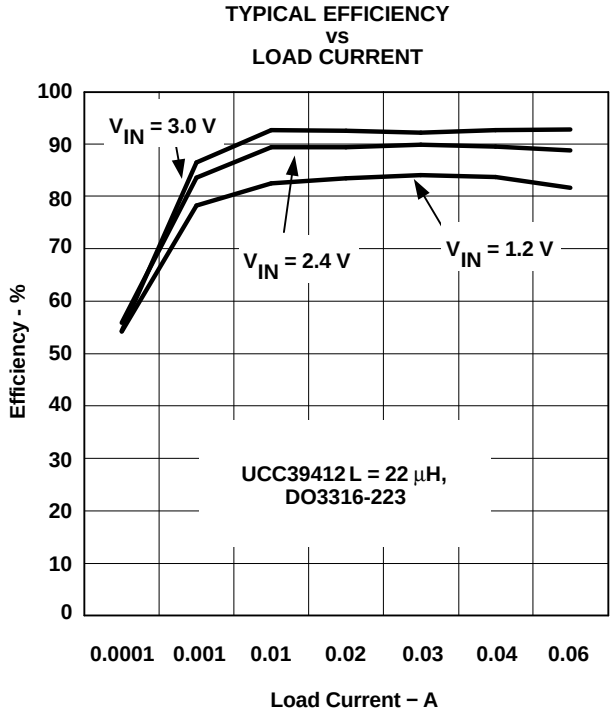


Figure 8.

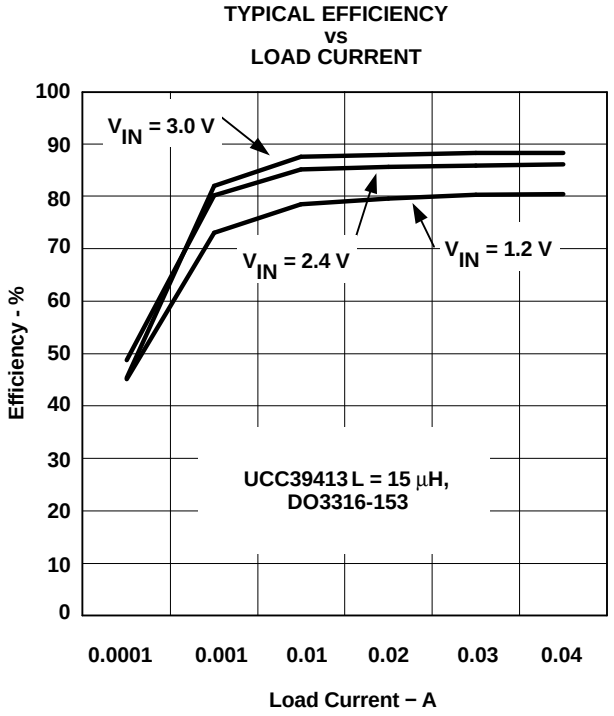


Figure 9.

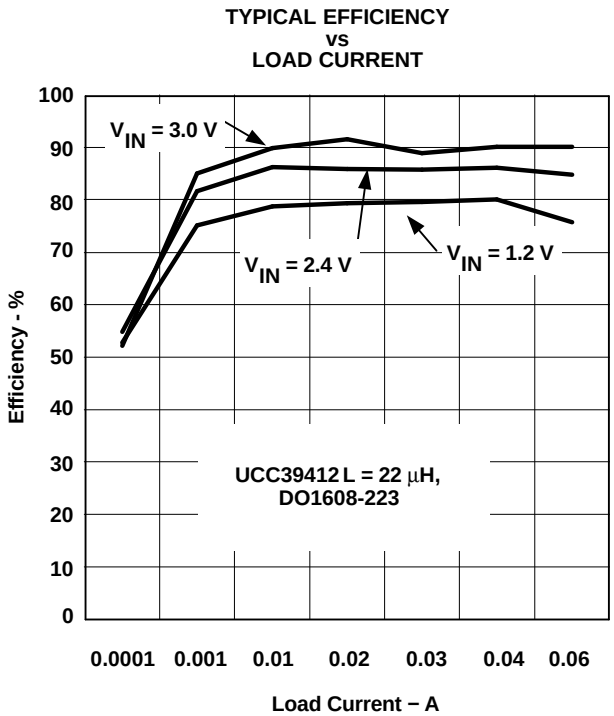


Figure 10.

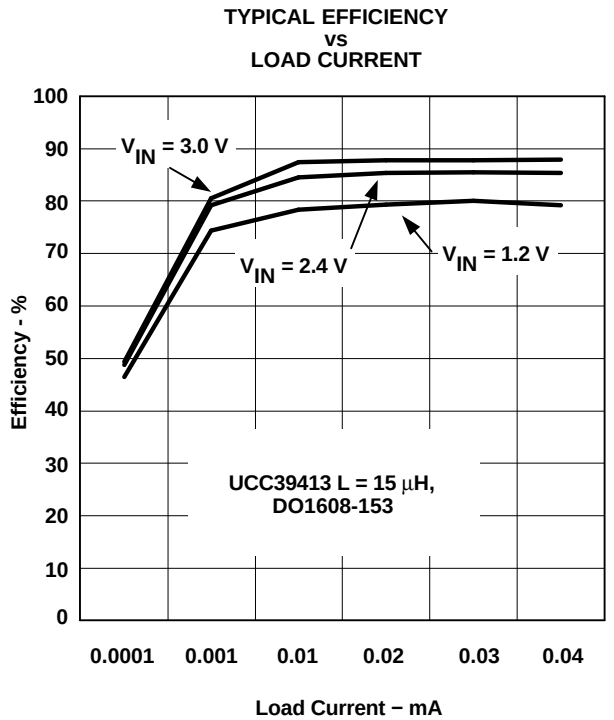


Figure 11.

TYPICAL CHARACTERISTICS (continued)

TYPICAL EFFICIENCY vs LOAD CURRENT (2 CELL APPLICATION)

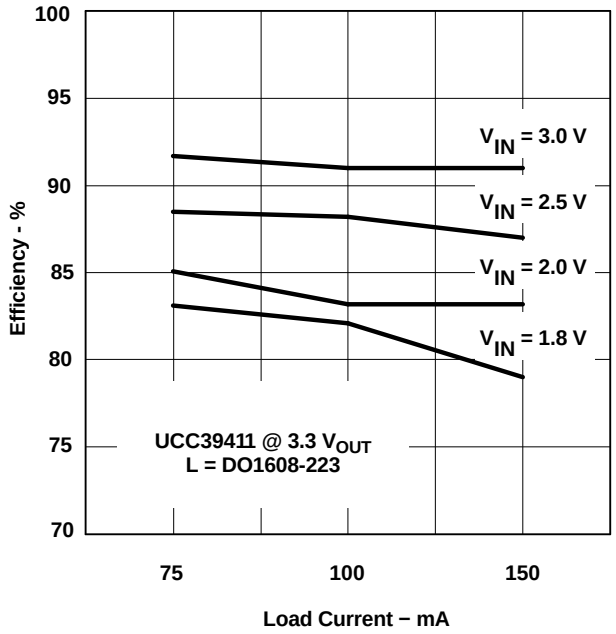


Figure 12.

MAXIMUM LOAD CURRENT, 2 CELL APPLICATION vs INPUT CURRENT

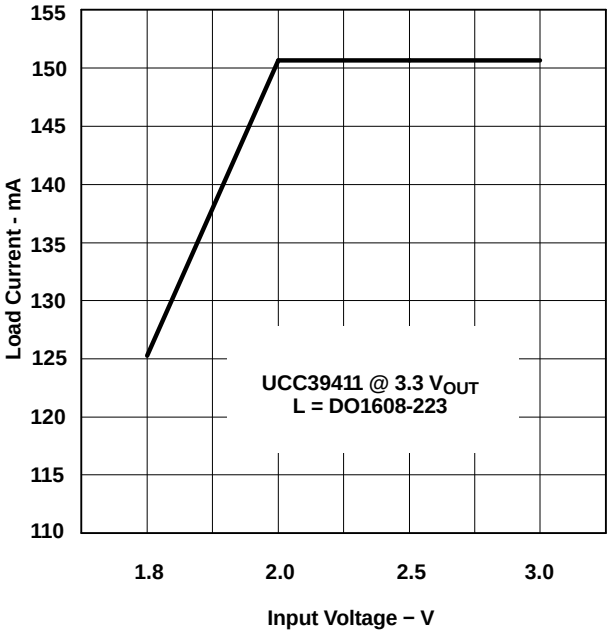


Figure 13.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC39411D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC 39411	Samples
UCC39411DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC 39411	Samples
UCC39411PW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	39411	Samples
UCC39412PW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	39412	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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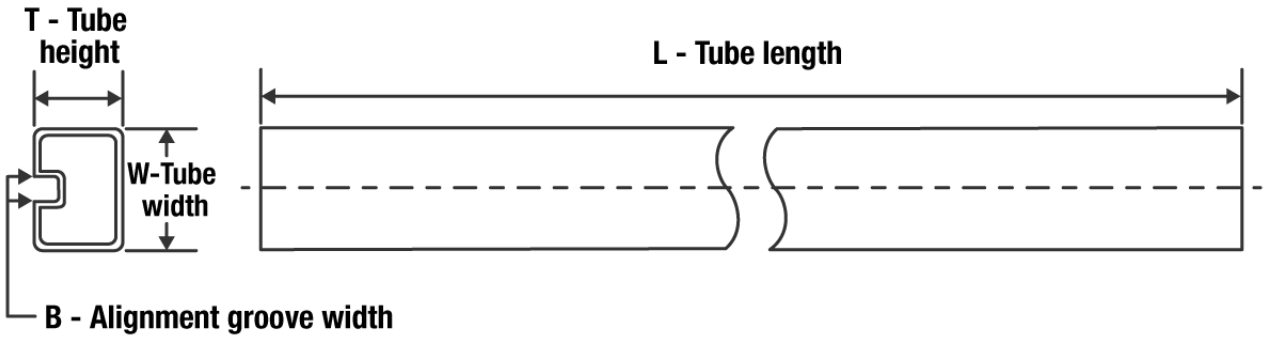
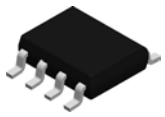
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC39411D	D	SOIC	8	75	506.6	8	3940	4.32
UCC39411DG4	D	SOIC	8	75	506.6	8	3940	4.32
UCC39411PW	PW	TSSOP	8	150	530	10.2	3600	3.5
UCC39412PW	PW	TSSOP	8	150	508	8.5	3250	2.8

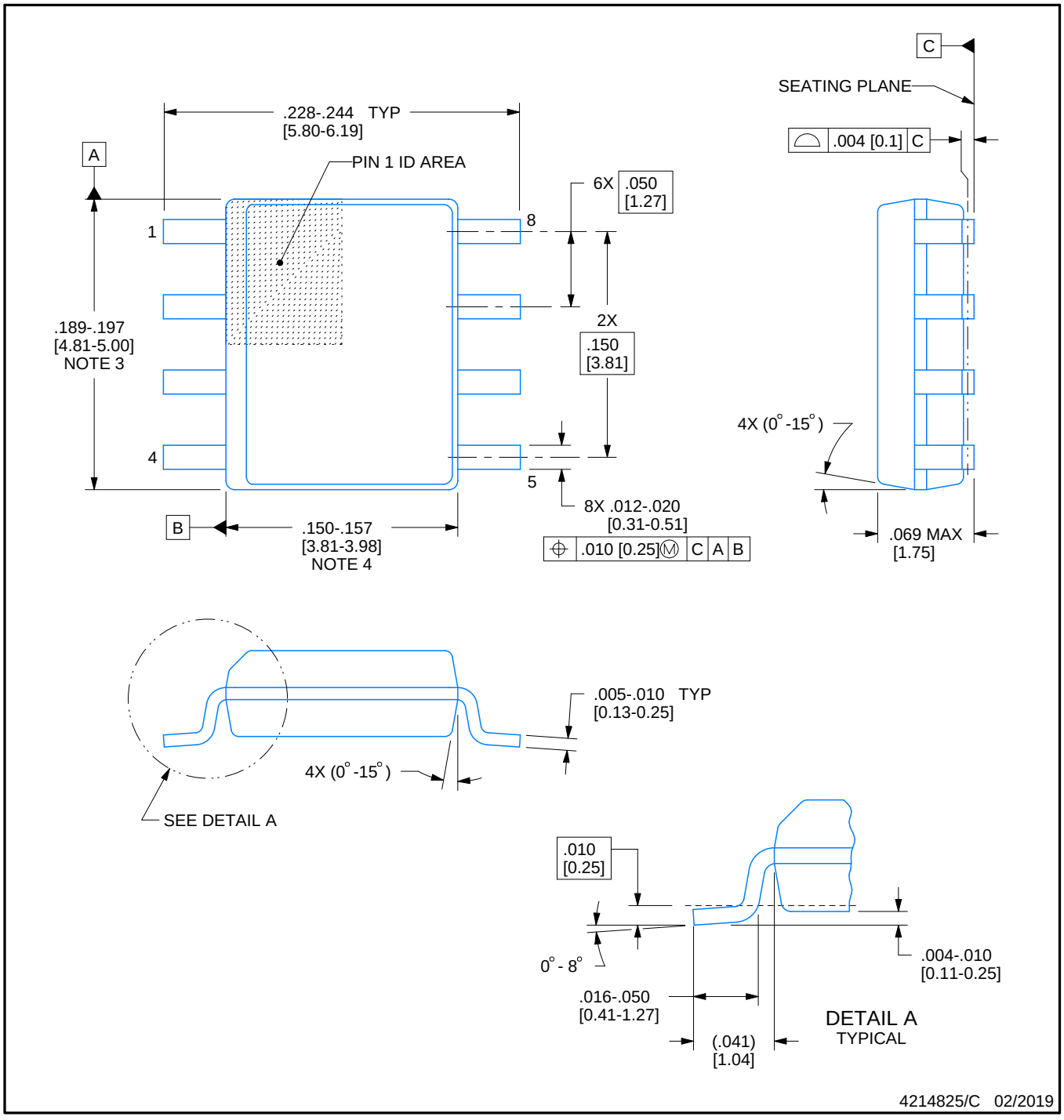


PACKAGE OUTLINE

D0008A

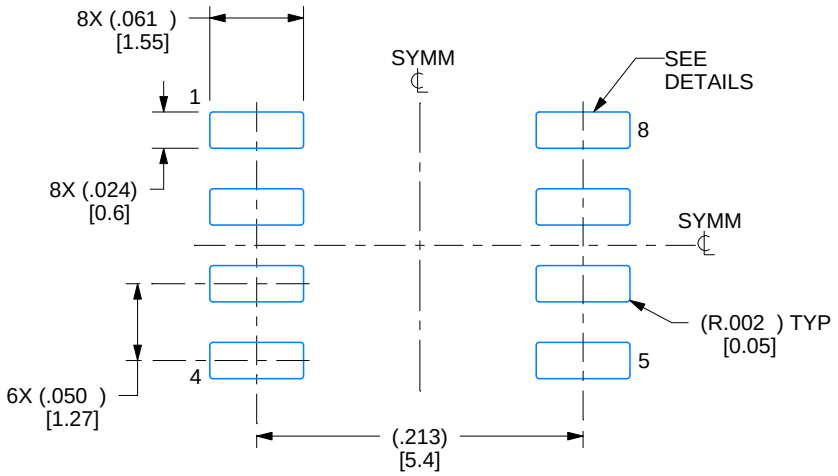
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

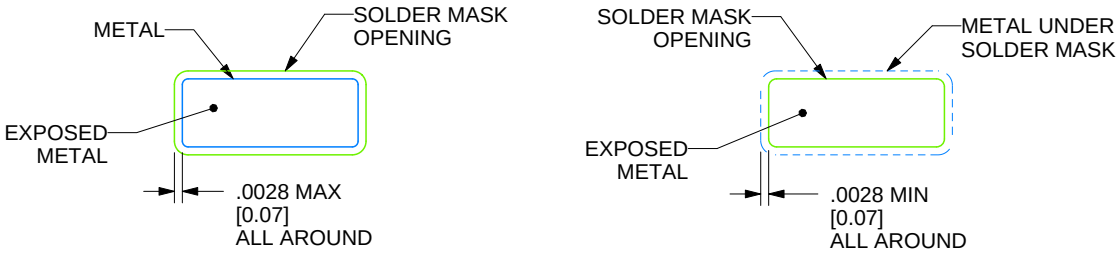


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

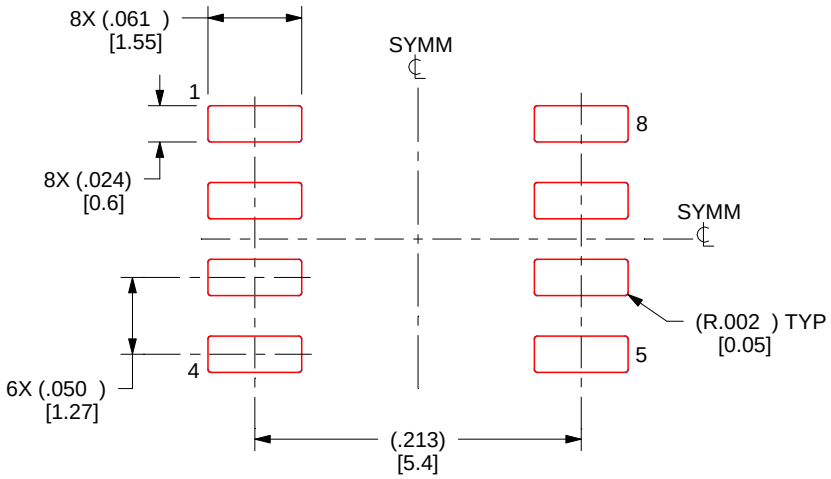
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

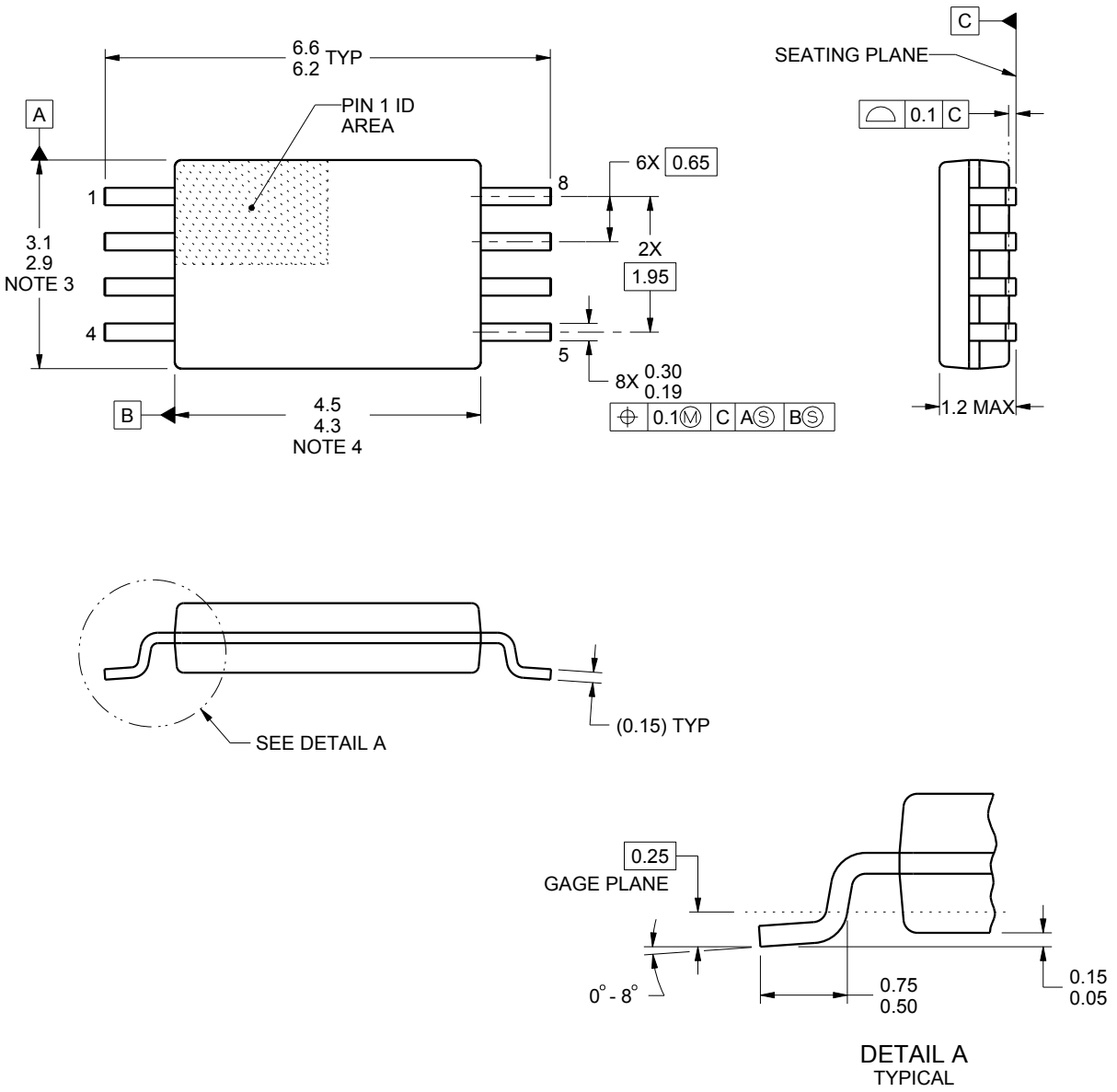
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

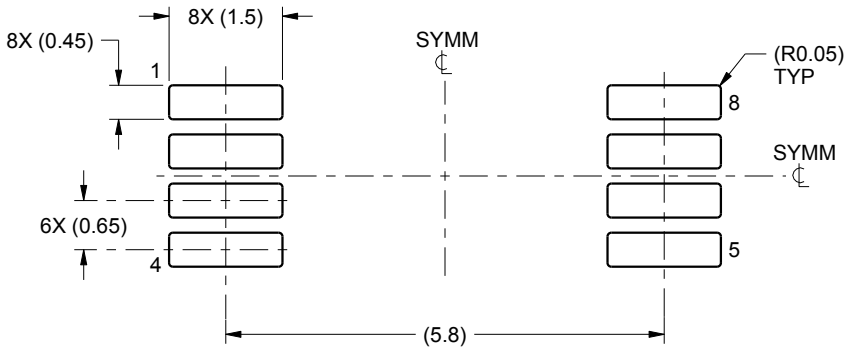
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

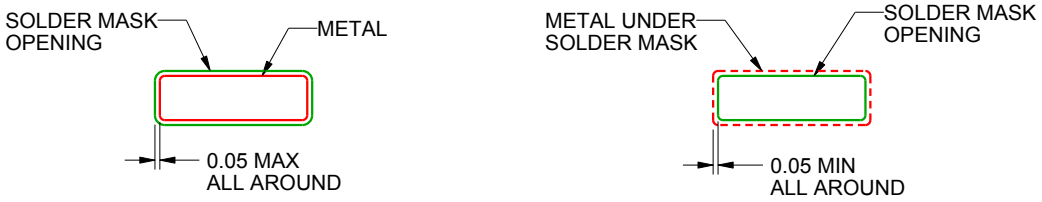


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

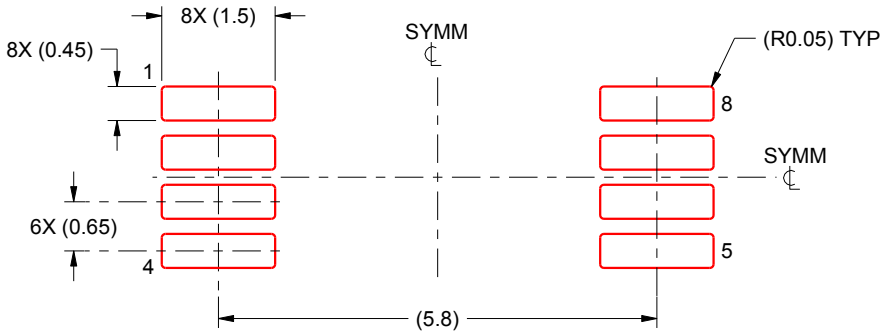


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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