# SPST CMOS ANALOG SWITCHES

## FEATURES

- **2-V to 12-V Single-Supply Operation**
- **Specified ON-State Resistance:**
  - **15 Ω Max With 12-V Supply**
  - **20 Ω Max With 5-V Supply**
  - **50 Ω Max With 3.3-V Supply**
- **Specified Low OFF-Leakage Currents:**
  - **1 nA at 25°C**
  - **10 nA at 85°C**

- **Specified Low ON-Leakage Currents:**
  - **1 nA at 25°C**
  - **10 nA at 85°C**
- **Low Charge Injection: 11.5 pC (12-V Supply)**
- **Fast Switching Speed:**
  $t_{ON}$ = 80 ns, $t_{OFF}$ = 50 ns (12-V Supply)
- **Break-Before-Make Operation ($t_{ON} > t_{OFF}$)**
- **TTL/CMOS-Logic Compatible With 5-V Supply**

## DESCRIPTION/ORDERING INFORMATION

The TS12A4514/TS12A4515 are single pole/single throw (SPST), low-voltage, single-supply CMOS analog switches, with very low switch ON-state resistance. The TS12A4514 is normally open (NO). The TS12A4515 is normally closed (NC).

These CMOS switches can operate continuously with a single supply between 2 V and 12 V. Each switch can handle rail-to-rail analog signals. The OFF-leakage current maximum is only 1 nA at 25°C or 10 nA at 85°C.

All digital inputs have 0.8-V to 2.4-V logic thresholds, ensuring TTL/CMOS-logic compatibility when using a 5-V supply.

For pin-compatible parts for use with dual supplies, see the TS12A4516/TS12A4517.

### ORDERING INFORMATION

| $T_A$ | PACKAGE[1][2] | | ORDERABLE PART NUMBER | TOP-SIDE MARKING[3] |
|---|---|---|---|---|
| –40°C to 85°C | PDIP – P | Reel of 1000 | TS12A4514P | TS12A4514P |
| | SOIC – D | Reel of 1500 | TS12A4514D | YD514 |
| | | Reel of 2500 | TS12A4514DR | |
| | SOP (SOT-23) – DBV | Reel of 3000 | TS12A4514DBVR | 9CJ_ |
| | PDIP – P | Reel of 1000 | TS12A4515P | TS12A4515P |
| | SOIC – D | Reel of 1500 | TS12A4515D | YD515 |
| | | Reel of 2500 | TS12A4515DR | |
| | SOP (SOT-23) – DBV | Reel of 3000 | TS12A4515DBVR | 9CK_ |

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(3) DBV: The last character designates assembly/test Site

# TS12A4514, TS12A4515

## PIN CONFIGURATIONS



**TS12A4514**
**D OR P PACKAGE**
**(TOP VIEW)**

**TS12A4515**
**D OR P PACKAGE**
**(TOP VIEW)**

**TS12A4514**
**SOT-23 PACKAGE**
**(TOP VIEW)**

**TS12A4515**
**SOT-23 PACKAGE**
**(TOP VIEW)**
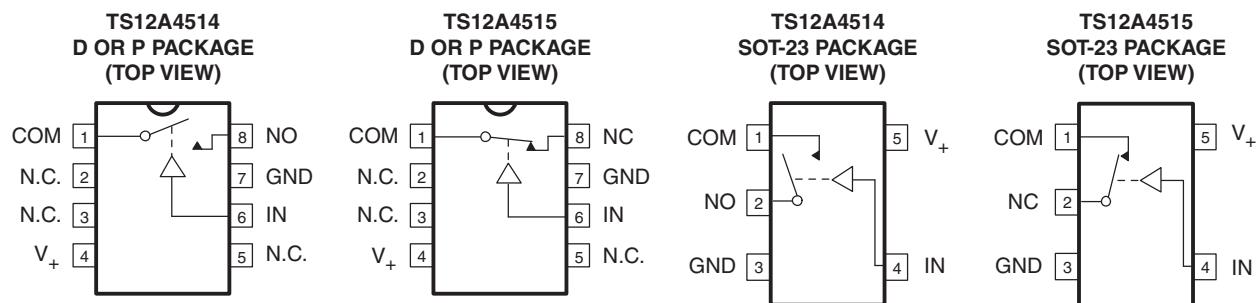
| INPUT | SWITCH STATE | |
|---|---|---|
| | TS12A4514 | TS12A4515 |
| LOW | OFF | ON |
| HIGH | ON | OFF |

MARKNG INFORMATION (SOTs onl y)

LOT SPECIFIC CODE
XX LXX
AE = TS12A4514
AF = TS12A4515

N.C. – Not internally connected

NO – Normally open

NC – Normally closed

## Absolute Minimum and Maximum Ratings[(1)(2)]

voltages referenced to GND

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_+$ | Supply voltage range[(3)] | −0.3 | 13 | V |
| $V_{NC}$ $V_{NO}$ $V_{COM}$ | Analog voltage range[(4)] | −0.3 | $V_+ + 0.3$ or ±20 mA | V |
| | Continuous current into any terminal | | ±20 | mA |
| | Peak current, NO or COM (pulsed at 1 ms, 10% duty cycle) | | ±30 | mA |
| | ESD per method 3015.7 | | >2000 | V |
| | Continuous power dissipation ($T_A$ = 70°C) | 8-pin plastic DIP (derate 9.09 mW/°C above 70°C) | 727 | mW |
| | | 8-pin SOIC (derate 5.88 mW/°C above 70°C) | 471 | |
| | | 5-pin SOT-23 (derate 7.1 mW/°C above 70°C) | 571 | |
| $T_A$ | Operating temperature range | −40 | 85 | °C |
| $T_{stg}$ | Storage temperature range | −65 | 150 | °C |
| | Lead temperature (soldering, 10 s) | | 300 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) Voltages exceeding $V_+$ or GND on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

## Electrical Characteristics for 5-V Supply[1]

$V_+$ = 4.5 V to 5.5 V, $V_{INH}$ = 2.4 V, $V_{INL}$ = 0.8 V, $T_A$ = −40°C to 85°C (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | $T_A$ | MIN | TYP[2] | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | |
| Analog signal range | $V_{COM}$, $V_{NO}$, $V_{NC}$ | | | 0 | | $V_+$ | V |
| ON-state resistance | $r_{on}$ | $V_+$ = 4.5 V, $V_{COM}$ = 3.5 V, $I_{COM}$ = 1 mA | 25°C | | 9.5 | 15 | Ω |
| | | | Full | | | 20 | |
| ON-state resistance flatness | $r_{on(flat)}$ | $V_{COM}$ = 1 V, 2 V, 3 V, $I_{COM}$ = 1 mA | 25°C | | 1 | 3 | Ω |
| | | | Full | | | 4 | |
| NO, NC OFF leakage current[3] | $I_{NO(OFF)}$, $I_{NC(OFF)}$ | $V_+$ = 5.5 V, $V_{COM}$ = 1 V, $V_{NO}$ or $V_{NC}$ = 4.5 V | 25°C | | | 1 | nA |
| | | | Full | | | 10 | |
| COM OFF leakage current[3] | $I_{COM(OFF)}$ | $V_+$ = 5.5 V, $V_{COM}$ = 1 V, $V_{NO}$ or $V_{NC}$ = 4.5 V | 25°C | | | 1 | nA |
| | | | Full | | | 10 | |
| COM ON leakage current[3] | $I_{COM(ON)}$ | $V_+$ = 5.5 V, $V_{COM}$ = 4.5 V, $V_{NO}$ or $V_{NC}$ = 4.5 V | 25°C | | | 1 | nA |
| | | | Full | | | 10 | |
| **Digital Control Input (IN)** | | | | | | | |
| Input logic high | $V_{IH}$ | | Full | 2.4 | | $V_+$ | V |
| Input logic low | $V_{IL}$ | | Full | 0 | | 0.8 | V |
| Input leakage current | $I_{IH}$, $I_{IL}$ | $V_{IN}$ = $V_+$, 0 V | Full | | | 0.01 | μA |
| **Dynamic** | | | | | | | |
| Turn-on time | $t_{ON}$ | see Figure 2 | 25°C | | 32 | 100 | ns |
| | | | Full | | | 125 | |
| Turn-off time | $t_{OFF}$ | see Figure 2 | 25°C | | 25 | 50 | ns |
| | | | Full | | | 60 | |
| Charge injection[4] | $Q_C$ | $C_L$ = 1 nF, $V_{NO}$ = 0 V, $R_S$ = 0 Ω, See Figure 1 | 25°C | | −3 | | pC |
| NO, NC OFF capacitance | $C_{NO(OFF)}$, $C_{NC(OFF)}$ | f = 1 MHz, See Figure 4 | 25°C | | 7.5 | | pF |
| COM OFF capacitance | $C_{COM(OFF)}$ | f = 1 MHz, See Figure 4 | 25°C | | 7.5 | | pF |
| COM ON capacitance | $C_{COM(ON)}$ | f = 1 MHz, See Figure 4 | 25°C | | 19 | | pF |
| Digital input capacitance | $C_I$ | $V_{IN}$ = $V_+$, 0 V | 25°C | | 1.5 | | pF |
| Bandwidth | BW | $R_L$ = 50 Ω, $C_L$ = 15 pF, $V_{NO}$ = 1 $V_{RMS}$, f = 100 kHz | 25°C | | 475 | | MHz |
| OFF isolation | $O_{ISO}$ | $R_L$ = 50 Ω, $C_L$ = 15 pF, $V_{NO}$ = 1 $V_{RMS}$, f = 100 kHz | 25°C | | −94 | | dB |
| Total harmonic distortion | THD | $R_L$ = 50 Ω, $C_L$ = 15 pF, $V_{NO}$ = 1 $V_{RMS}$, f = 100 kHz | 25°C | | 0.08 | | % |
| **Supply** | | | | | | | |
| $V_+$ supply current | $I_+$ | $V_{IN}$ = 0 V or $V_+$ | 25°C | | | 0.05 | μA |
| | | | Full | | | 0.1 | |

(1)   The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2)   Typical values are at $T_A$ = 25°C.
(3)   Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are ensured by correlation at 25°C.
(4)   Specified by design, not production tested

# TS12A4514, TS12A4515

## Electrical Characteristics for 12-V Supply[1]

$V_+$ = 11.4 V to 12.6 V, $V_{INH}$ = 5 V, $V_{INL}$ = 0.8 V, $T_A$ = –40°C to 85°C (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | $T_A$ | MIN | TYP[2] | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | |
| Analog signal range | $V_{COM}$, $V_{NO}$, $V_{NC}$ | | | 0 | | $V_+$ | V |
| ON-state resistance | $r_{on}$ | $V_+$ = 11.4 V, $V_{COM}$ = 10 V, $I_{COM}$ = 1 mA | 25°C | | 6.5 | 10 | Ω |
| | | | Full | | | 15 | |
| ON-state resistance flatness | $r_{on(flat)}$ | $V_+$ = 11.4 V, $V_{COM}$ = 2 V, 5 V, 10 V, $I_{COM}$ = 1 mA | 25°C | | 1.5 | 3 | Ω |
| | | | Full | | | 4 | |
| NO, NC OFF leakage current[3] | $I_{NO(OFF)}$, $I_{NC(OFF)}$ | $V_+$ = 12.6 V, $V_{COM}$ = 1 V, $V_{NO}$ or $V_{NC}$ = 10 V | 25°C | | | 1 | nA |
| | | | Full | | | 10 | |
| COM OFF leakage current[3] | $I_{COM(OFF)}$ | $V_+$ = 12.6 V, $V_{COM}$ = 1 V, $V_{NO}$ or $V_{NC}$ = 10 V | 25°C | | | 1 | nA |
| | | | Full | | | 10 | |
| COM ON leakage current[3] | $I_{COM(ON)}$ | $V_+$ = 12.6 V, $V_{COM}$ = 10 V, $V_{NO}$ or $V_{NC}$ = 10 V | 25°C | | | 1 | nA |
| | | | Full | | | 10 | |
| **Digital Control Input (IN)** | | | | | | | |
| Input logic high | $V_{IH}$ | | Full | 5 | | $V_+$ | V |
| Input logic low | $V_{IL}$ | | Full | 0 | | 0.8 | V |
| Input leakage current | $I_{IH}$, $I_{IL}$ | $V_{IN}$ = $V_+$, 0 V | Full | | | 0.01 | µA |
| **Dynamic** | | | | | | | |
| Turn-on time | $t_{ON}$ | See Figure 2 | 25°C | | 22 | 75 | ns |
| | | | Full | | | 80 | |
| Turn-off time | $t_{OFF}$ | See Figure 2 | 25°C | | 20 | 45 | ns |
| | | | Full | | | 50 | |
| Charge injection[4] | $Q_C$ | $C_L$ = 1 nF, $V_{NO}$ = 0 V, $R_S$ = 0 Ω, See Figure 1 | 25°C | | –11.5 | | pC |
| NO, NC OFF capacitance | $C_{NO(OFF)}$ $C_{NC(OFF)}$ | f = 1 MHz, See Figure 4 | 25°C | | 7.5 | | pF |
| COM OFF capacitance | $C_{COM(OFF)}$ | f = 1 MHz, See Figure 4 | 25°C | | 7.5 | | pF |
| COM ON capacitance | $C_{COM(ON)}$ | f = 1 MHz, See Figure 4 | 25°C | | 21.5 | | pF |
| Digital input capacitance | $C_I$ | $V_{IN}$ = $V_+$, 0 V | 25°C | | 1.5 | | pF |
| Bandwidth | BW | $R_L$ = 50 Ω, $C_L$ = 15 pF, $V_{NO}$ = 1 $V_{RMS}$, f = 100 kHz | 25°C | | 520 | | MHz |
| OFF isolation | $O_{ISO}$ | $R_L$ = 50 Ω, $C_L$ = 15 pF, $V_{NO}$ = 1 $V_{RMS}$, f = 100 kHz | 25°C | | –95 | | dB |
| Total harmonic distortion | THD | $R_L$ = 50 Ω, $C_L$ = 15 pF, $V_{NO}$ = 1 $V_{RMS}$, f = 100 kHz | 25°C | | 0.07 | | % |
| **Supply** | | | | | | | |
| $V_+$ supply current | $I_+$ | $V_{IN}$ = 0 V or $V_+$ | 25°C | | | 0.05 | µA |
| | | | Full | | | 0.2 | |

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) Typical values are at $T_A$ = 25°C.
(3) Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are ensured by correlation at 25°C.
(4) Specified by design, not production tested

Product Folder Link(s): *TS12A4514 TS12A4515*

## Electrical Characteristics for 3-V Supply[1]

$V_+$ = 3 V to 3.6 V, $T_A$ = –40°C to 85°C (unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | $T_A$ | MIN | TYP[2] | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | |
| Analog signal range | $V_{COM}$, $V_{NO}$, $V_{NC}$ | | | 0 | | $V_+$ | V |
| ON-state resistance | $r_{on}$ | $V_+$ = 3 V, $V_{COM}$ = 1.5 V, $I_{NO}$ = 1 mA, | 25°C | | 18.5 | 40 | Ω |
| | | | Full | | | 50 | |
| ON-state resistance flatness | $r_{on(flat)}$ | $V_+$ = 3 V, $V_{COM}$ = 1 V, 1.5 V, 2 V, $I_{COM}$ = 1 mA | 25°C | | 1 | 3 | Ω |
| | | | Full | | | 4 | |
| NO, NC OFF leakage current[3] | $I_{NO(OFF)}$, $I_{NC(OFF)}$ | $V_+$ = 3.6 V, $V_{COM}$ = 1 V, $V_{NO}$ or $V_{NC}$ = 3 V | 25°C | | | 1 | nA |
| | | | Full | | | 10 | |
| COM OFF leakage current[3] | $I_{COM(OFF)}$ | $V_+$ = 3.6 V, $V_{COM}$ = 1 V, $V_{NO}$ or $V_{NC}$ = 3 V | 25°C | | | 1 | nA |
| | | | Full | | | 10 | |
| COM ON leakage current[3] | $I_{COM(ON)}$ | $V_+$ = 3.6 V, $V_{COM}$ = 3 V, $V_{NO}$ or $V_{NC}$ = 3 V | 25°C | | | 1 | nA |
| | | | Full | | | 10 | |
| **Digital Control Input (IN)** | | | | | | | |
| Input logic high | $V_{IH}$ | | Full | 2.4 | | $V_+$ | V |
| Input logic low | $V_{IL}$ | | Full | 0 | | 0.8 | V |
| Input leakage current | $I_{IH}$, $I_{IL}$ | $V_{IN}$ = $V_+$, 0 V | Full | | | 0.01 | µA |
| **Dynamic** | | | | | | | |
| Turn-on time[4] | $t_{ON}$ | See Figure 2 | 25°C | | 63 | 120 | ns |
| | | | Full | | | 175 | |
| Turn-off time[4] | $t_{OFF}$ | See Figure 2 | 25°C | | 33 | 80 | ns |
| | | | Full | | | 120 | |
| Charge injection[4] | $Q_C$ | $C_L$ = 1 nF, See Figure 1 | 25°C | | −1.5 | | pC |
| NO, NC OFF capacitance | $C_{NO(OFF)}$, $C_{NC(OFF)}$ | f = 1 MHz, See Figure 4 | 25°C | | 7.5 | | pF |
| COM OFF capacitance | $C_{COM(OFF)}$ | f = 1 MHz, See Figure 4 | 25°C | | 7.5 | | pF |
| COM ON capacitance | $C_{COM(ON)}$ | f = 1 MHz, See Figure 4 | 25°C | | 17 | | pF |
| Digital input capacitance | $C_I$ | $V_{IN}$ = $V_+$, 0 V | 25°C | | 1.5 | | pF |
| Bandwidth | BW | $R_L$ = 50 Ω, $C_L$ = 15 pF, $V_{NO}$ = 1 $V_{RMS}$, f = 100 kHz | 25°C | | 460 | | MHz |
| OFF isolation | $O_{ISO}$ | $R_L$ = 50 Ω, $C_L$ = 15 pF, $V_{NO}$ = 1 $V_{RMS}$, f = 100 kHz | 25°C | | −94 | | dB |
| Total harmonic distortion | THD | $R_L$ = 50 Ω, $C_L$ = 15 pF, $V_{NO}$ = 1 $V_{RMS}$, f = 100 kHz | 25°C | | 0.15 | | % |
| **Supply** | | | | | | | |
| $V_+$ supply current | $I_+$ | $V_{IN}$ = 0 V or $V_+$ | 25°C | | | 0.03 | µA |
| | | | Full | | | 0.05 | |

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) Typical values are at $T_A$ = 25°C.
(3) Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are ensured by correlation at 25°C.
(4) Specified by design, not production tested

# TS12A4514, TS12A4515

## PIN DESCRIPTION[1]

| PIN NO. | | | | NAME | DESCRIPTION |
|---|---|---|---|---|---|
| TS12A4514 | | TS12A4515 | | | |
| D, P | SOT-23 | D, P | SOT-23 | | |
| 1 | 1 | 1 | 1 | COM | Common |
| 2, 3, 5 | – | 2, 3, 5 | – | N.C. | No connect (not internally connected) |
| 4 | 5 | 4 | 5 | $V_+$ | Power supply |
| 6 | 4 | 6 | 4 | IN | Digital control to connect COM to NO or NC |
| 7 | 3 | 7 | 3 | GND | Digital ground |
| 8 | 2 | – | – | NO | Normally open |
| – | – | 8 | 2 | NC | Normally closed |

(1) NO, NC, and COM pins are identical and interchangeable. Any may be considered as an input or an output; signals pass in both directions.

*Submit Documentation Feedback*                    Copyright © 2006–2009, Texas Instruments Incorporated

Product Folder Link(s): *TS12A4514 TS12A4515*

**Figure 2. Switching Times**
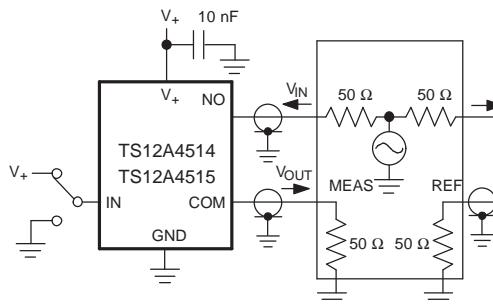


Measurements are standardized against short at socket terminals. OFF isolation is measured between COM and OFF terminals on each switch. ON loss is measured between COM and ON terminals on each switch. Signal direction through switch is reversed; worst values are recorded.

$$\text{OFF Isolation} = 20\log \frac{V_{OUT}}{V_{IN}}$$

$$\text{ON Loss} = 20\log \frac{V_{OUT}}{V_{IN}}$$

**Figure 3. OFF Isolation and ON Loss**
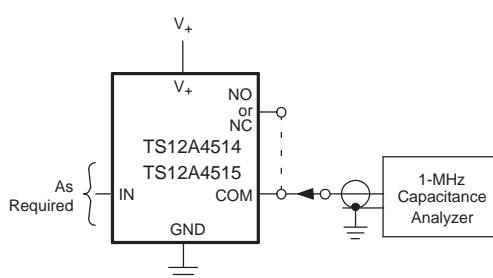


**Figure 4. NO, NC, and COM Capacitance**

Product Folder Link(s): *TS12A4514 TS12A4515*

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TS12A4514D | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | YD514 | Samples |
| TS12A4514DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 9CJE | Samples |
| TS12A4514DR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | YD514 | Samples |
| TS12A4514P | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | TS12A4514P | Samples |
| TS12A4515D | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | YD515 | Samples |
| TS12A4515DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 9CKE | Samples |
| TS12A4515DR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | YD515 | Samples |
| TS12A4515DRG4 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | YD515 | Samples |
| TS12A4515P | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | TS12A4515P | Samples |
| TS12A4515PE4 | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | TS12A4515P | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2) RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**
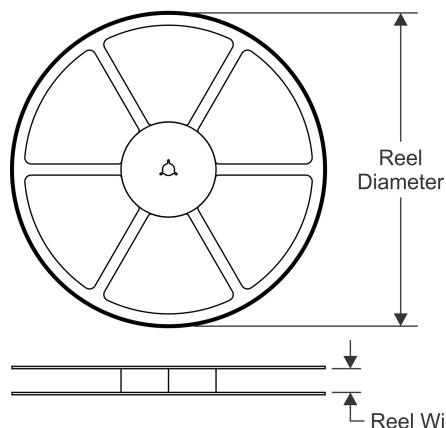
**TAPE DIMENSIONS**
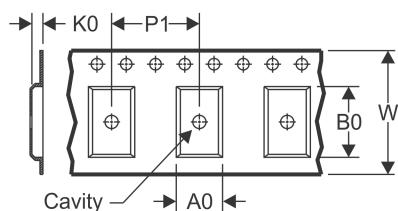
| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**
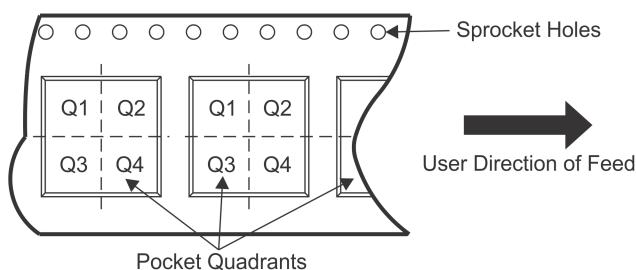
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TS12A4514DBVR | SOT-23 | DBV | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TS12A4514DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TS12A4515DBVR | SOT-23 | DBV | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TS12A4515DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**
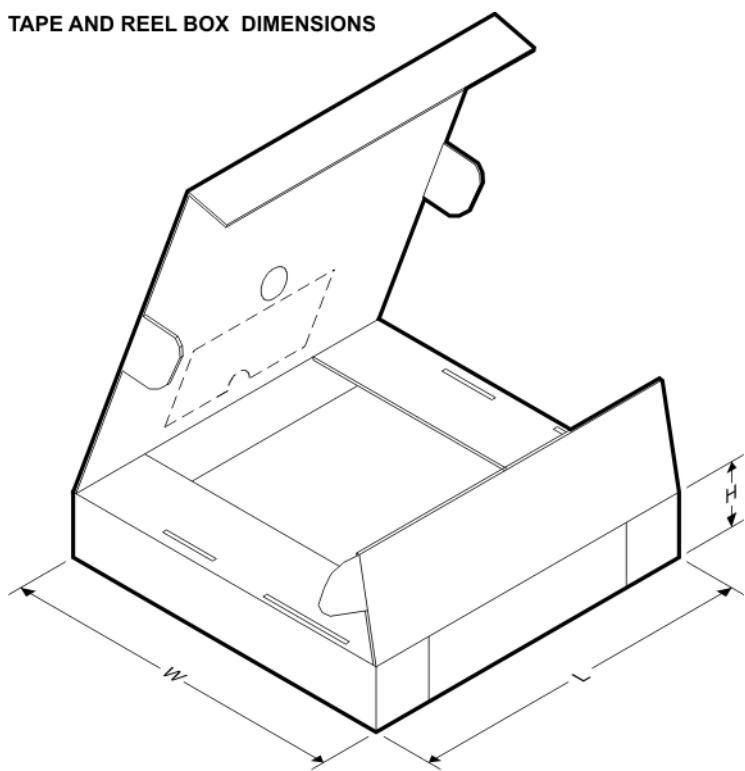


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TS12A4514DBVR | SOT-23 | DBV | 5 | 3000 | 200.0 | 183.0 | 25.0 |
| TS12A4514DR | SOIC | D | 8 | 2500 | 853.0 | 449.0 | 35.0 |
| TS12A4515DBVR | SOT-23 | DBV | 5 | 3000 | 200.0 | 183.0 | 25.0 |
| TS12A4515DR | SOIC | D | 8 | 2500 | 853.0 | 449.0 | 35.0 |

# PACKAGE MATERIALS INFORMATION

**TUBE**
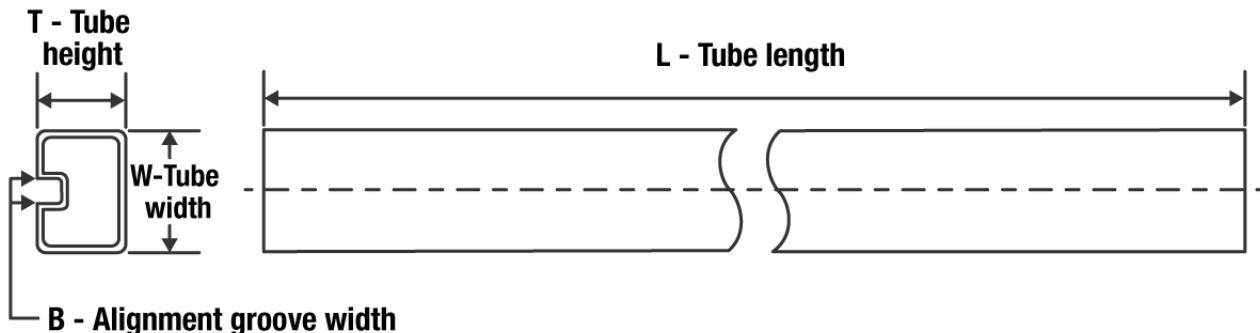


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| TS12A4514D | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| TS12A4514P | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TS12A4515D | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| TS12A4515P | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TS12A4515PE4 | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |

4214839/F   06/2021
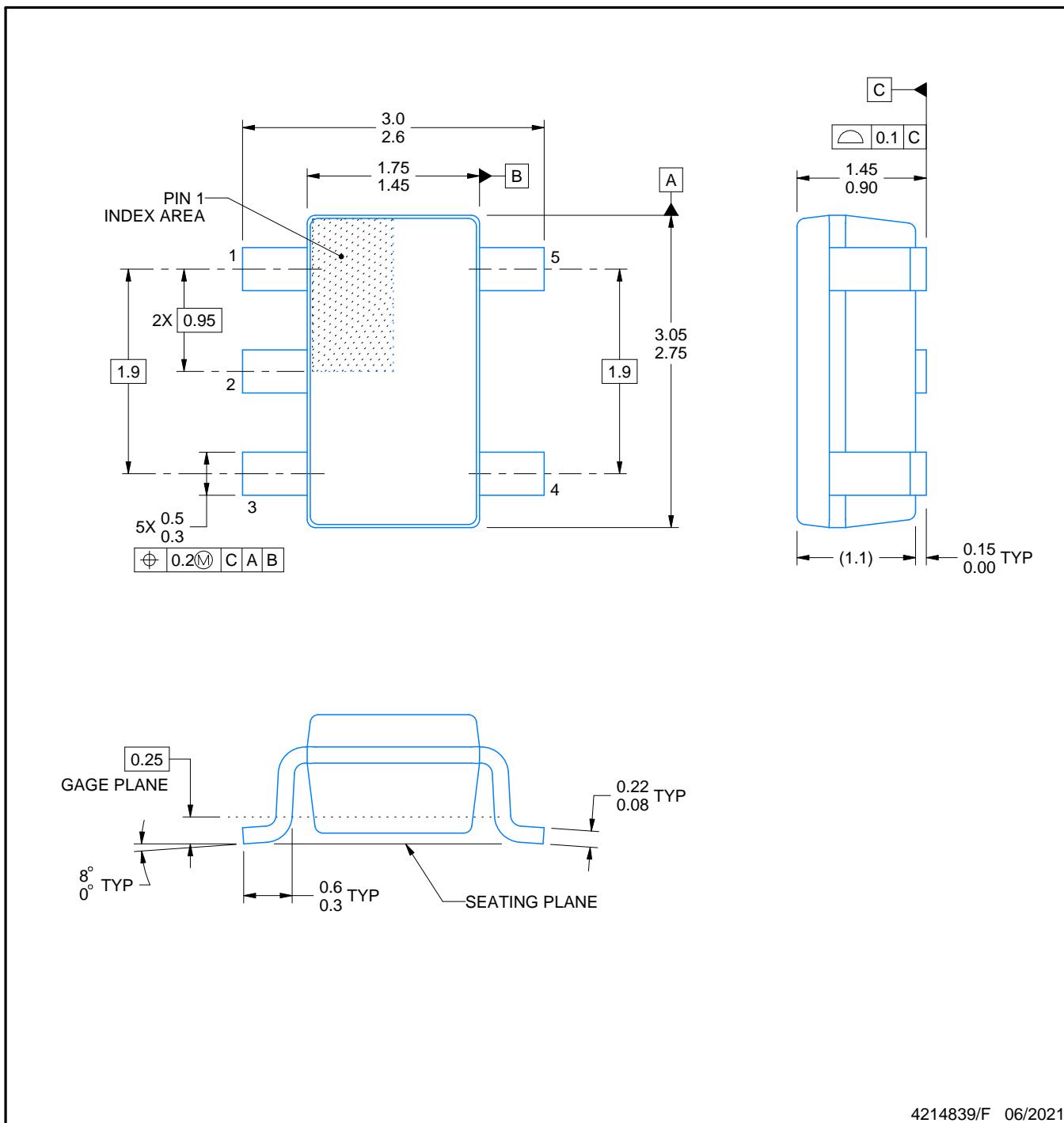
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.

PKG ℄

5X (1.1)

1

5X (0.6)

5

SYMM ℄

2

(1.9)

2X (0.95)

3

4

(R0.05) TYP

(2.6)
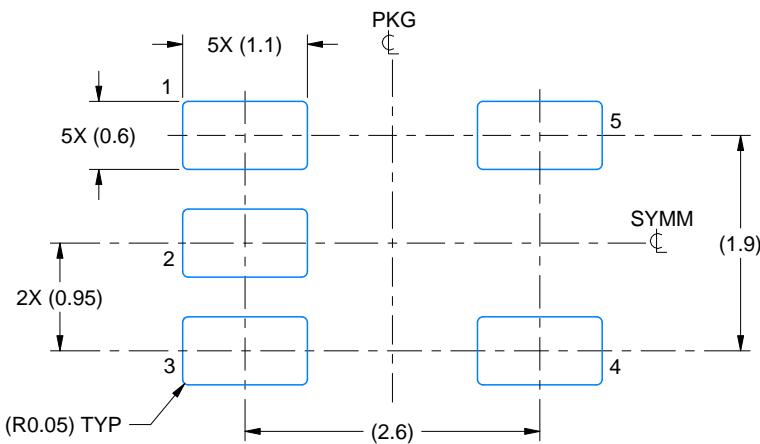
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

SOLDER MASK OPENING

METAL

METAL UNDER SOLDER MASK

SOLDER MASK OPENING

EXPOSED METAL

EXPOSED METAL

0.07 MAX ARROUND

0.07 MIN ARROUND

NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED
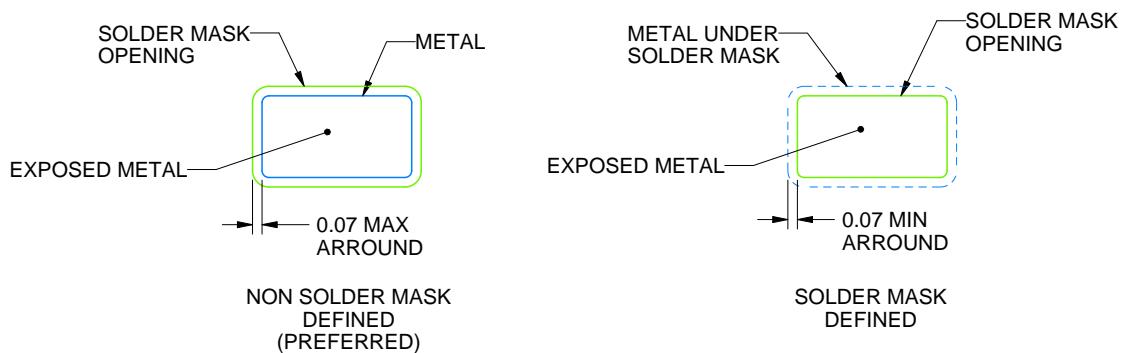
SOLDER MASK DETAILS

4214839/F   06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
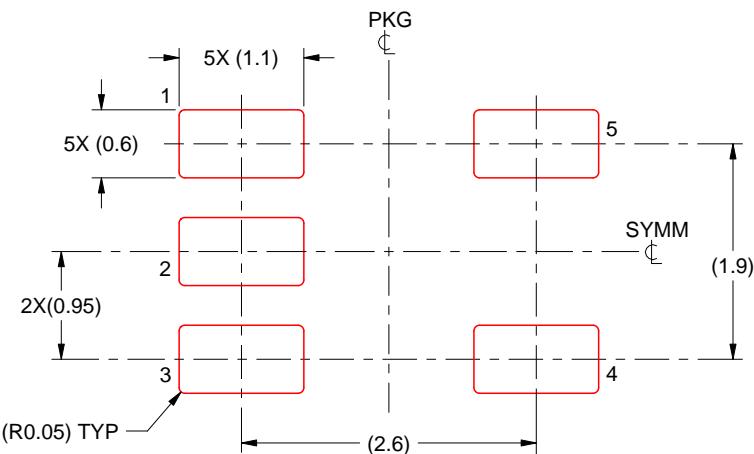
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F   06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

P (R−PDIP−T8)                                    PLASTIC DUAL−IN−LINE PACKAGE



0.400 (10,16)
0.355 (9,02)

8          5

0.260 (6,60)
0.240 (6,10)

1          4

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92)
MAX
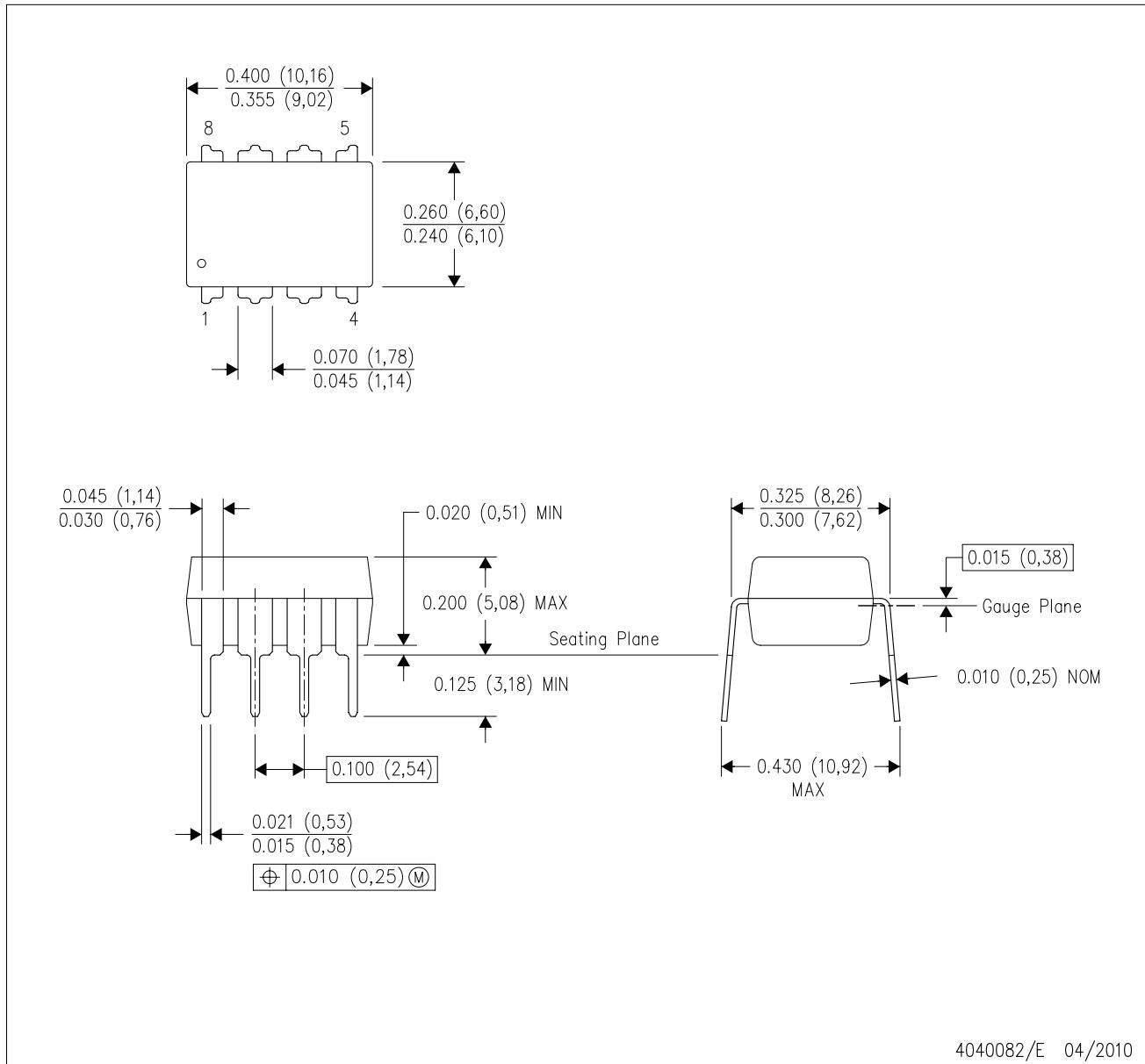
4040082/E  04/2010

NOTES:   A.  All linear dimensions are in inches (millimeters).
         B.  This drawing is subject to change without notice.
         C.  Falls within JEDEC MS−001 variation BA.

4214825/C   02/2019
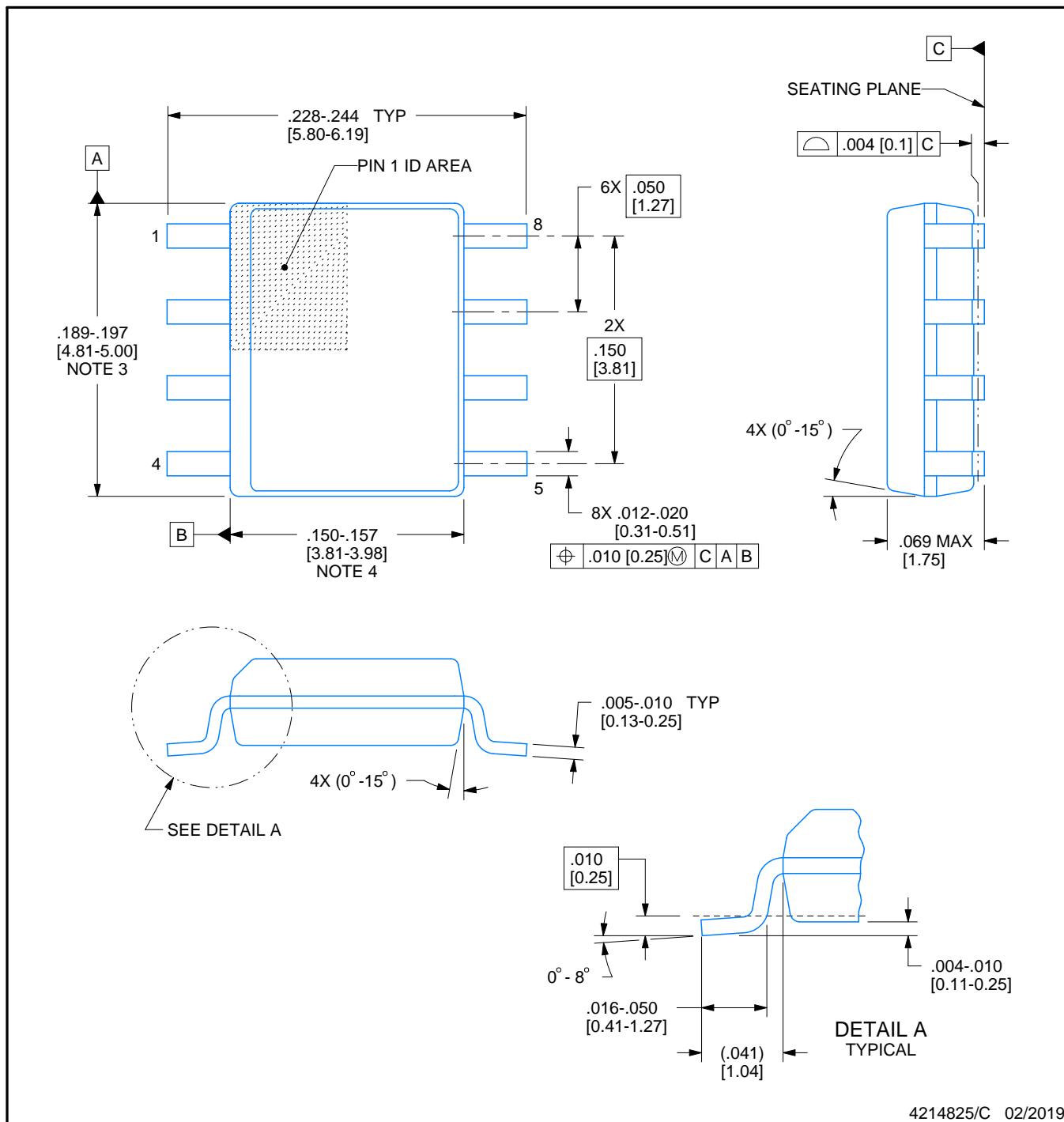
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

8X (.061 )
[1.55]

SYMM
₵

SEE
DETAILS

1

8

8X (.024)
[0.6]

SYMM
₵

(R.002 ) TYP
[0.05]

4

5

6X (.050 )
[1.27]

(.213)
[5.4]

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

METAL

SOLDER MASK
OPENING

SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

EXPOSED
METAL

EXPOSED
METAL

.0028 MAX
[0.07]
ALL AROUND

.0028 MIN
[0.07]
ALL AROUND
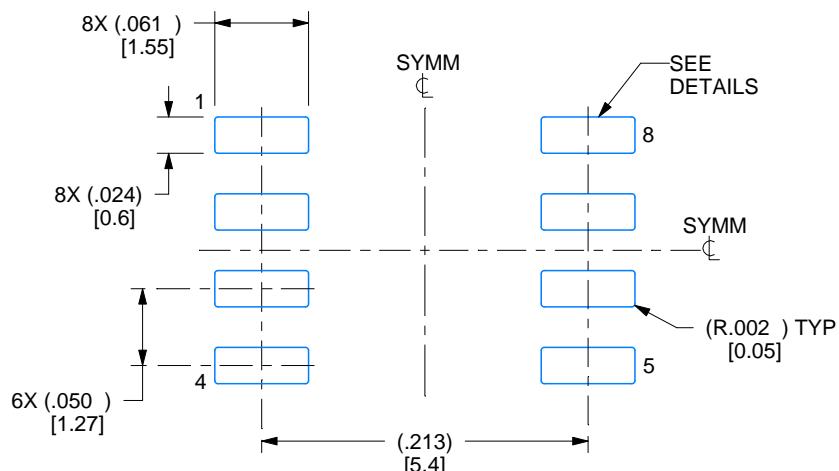
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED
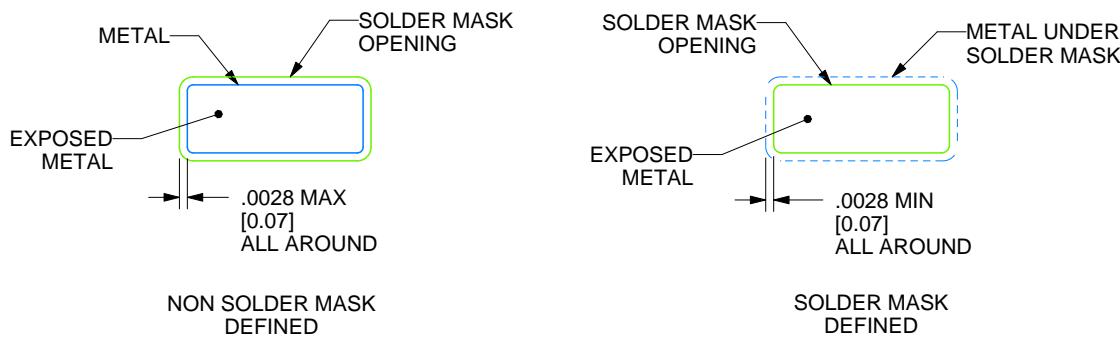
SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

8X (.061 )
[1.55]

SYMM
℄

1

8X (.024)
[0.6]

8

SYMM
℄

(R.002 ) TYP
[0.05]

6X (.050 )
[1.27]

4

5

(.213)
[5.4]
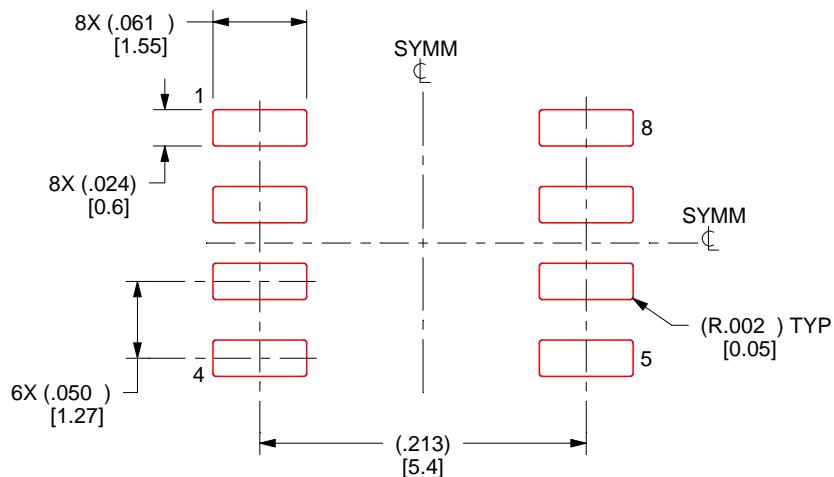
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C  02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# IMPORTANT NOTICE AND DISCLAIMER