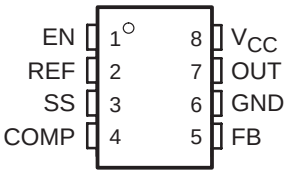
- **Negative 5-V 200-mA Output ($V_{CC} \geq 4.5$ V)**
- **4-V to 6.2-V Input Operating Range**
- **78% Typical Efficiency**
- **160-kHz Fixed-Frequency Current-Mode PWM Controller**
- **EN Input Inhibits Operation and Reduces Supply Current to 1 μA**
- **Soft Start**
- **8-Pin SOIC and DIP Packages**
- **−40°C to 85°C Free-Air Temperature Range**
- **Pin-for-Pin Compatible with MAX735**

D OR P PACKAGE
(TOP VIEW)



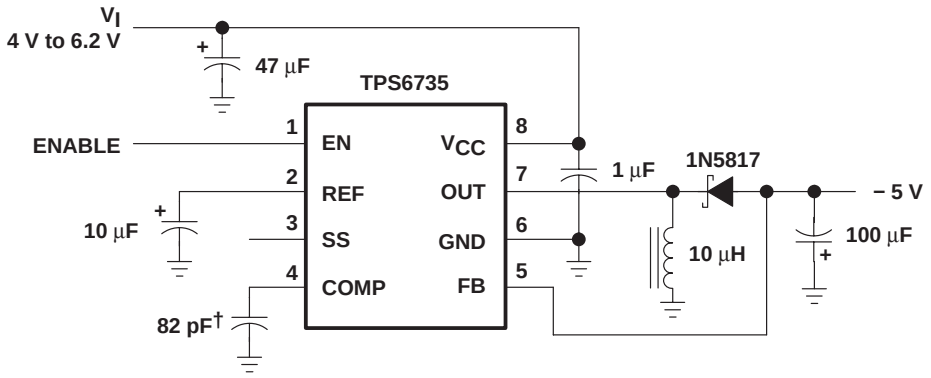
description

The TPS6735 is a fixed negative 5-V output inverting dc/dc converter capable of delivering 200 mA from inputs as low as 4.5 V. The only external components required are an inductor, an output filter capacitor, an input filter capacitor, a reference filter capacitor, and a Schottky rectifier. An enable input is provided to shut down the inverter when a −5-V output is not needed. The typical supply current is 1.9 mA at no-load and is further reduced to 1-μA when the enable input is low.

The TPS6735 is a 160-kHz current-mode pulse-width-modulation (PWM) controller with a p-channel MOSFET power switch. The gate drive uses the −5-V output to reduce the die area needed to realize the 0.4-Ω MOSFET. Soft start is accomplished with the addition of one small capacitor at SS. A 1.22-V reference is available for external loads up to 125 μA.

The TPS6735 is attractive for board-level dc/dc conversion in computer peripherals and in battery-powered equipment requiring high efficiency and low supply current.

The TPS6735 is available in 8-pin DIP and SOIC packages and operates over a free-air temperature range of −40°C to 85°C.



† Not required for loads of 100 mA or less

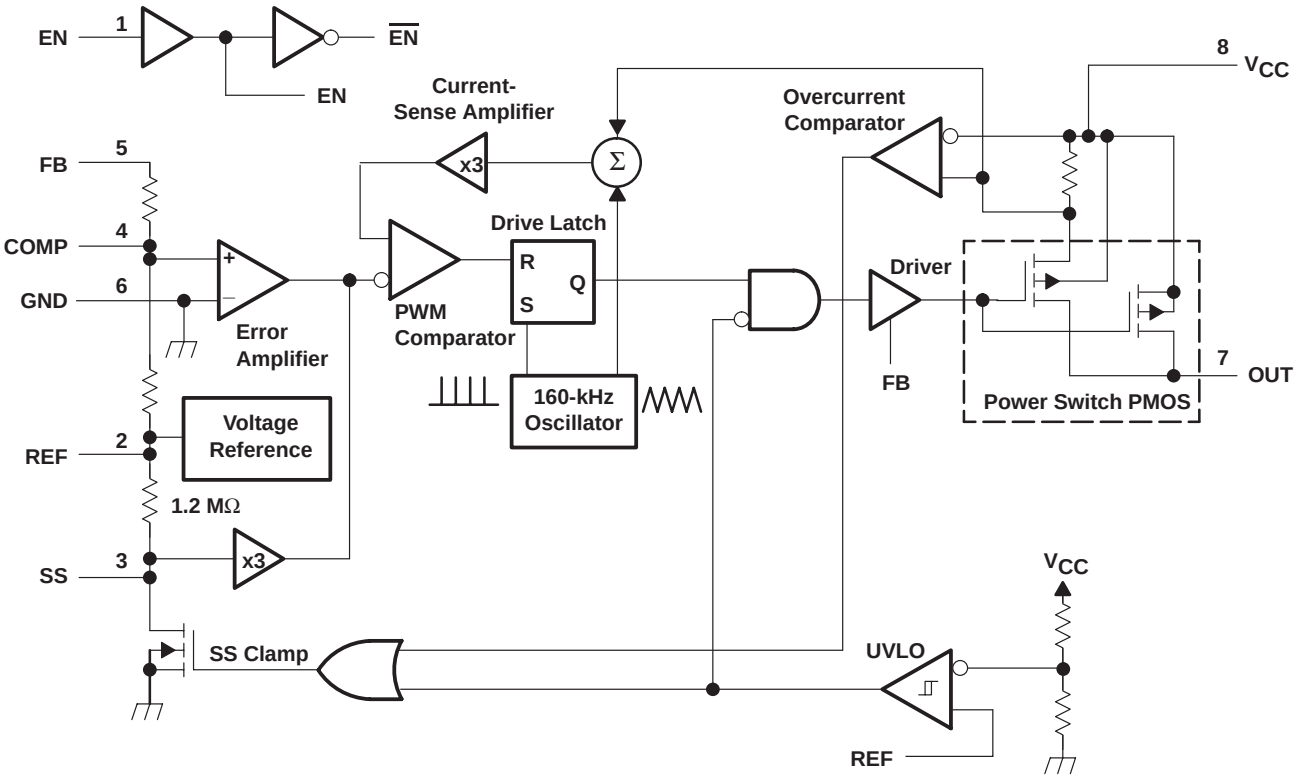
Figure 1. Typical Circuit

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		CHIP FORM (Y)
	SMALL OUTLINE (D)	PLASTIC DIP (P)	
−40°C to 85°C	TPS6735ID	TPS6735IP	TPS6735Y

The D package is also available taped and reeled (TPS6735IDR).

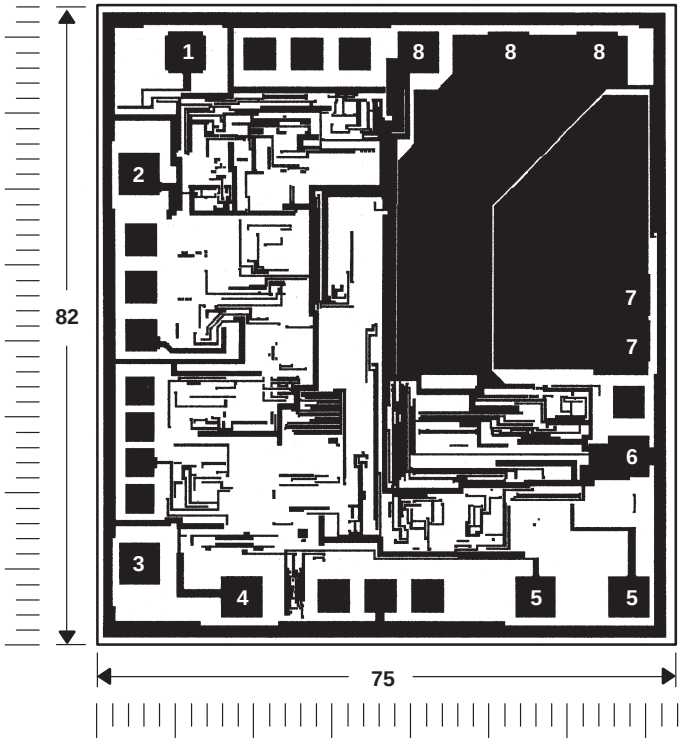
functional block diagram

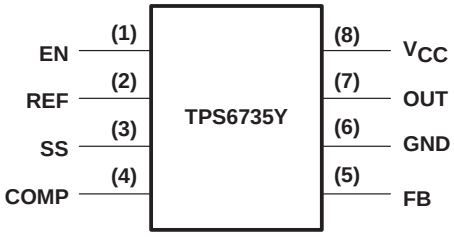


chip information

These chips, when properly assembled, display characteristics similar to the TPS6735. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
EN	1	Enable. EN > 2 V turns on the TPS6735. EN ≤ 0.4 V turns it off.
REF	2	1.22-V reference voltage output. REF can source 125 μA for external loads.
SS	3	Soft start. A capacitor between SS and GND brings the output voltage up slowly.
COMP	4	Compensation. A capacitor to ground stabilizes the feedback loop.
FB	5	Feedback. FB connects to the dc/dc converter output.
GND	6	Ground
OUT	7	Power MOSFET drain connection
V_{CC}	8	Supply-voltage input

detailed description

The following descriptions refer to the functional block diagram.

current-sense amplifier

The current-sense amplifier, which has a fixed gain of 3, amplifies the slope-compensated current-sense voltage (a summation of the voltage on the current-sense resistor and the oscillator ramp) and feeds it to the PWM comparator.

driver latch

The latch, which consists of a set/reset flip-flop and associated logic, controls the state of the power switch by turning the driver on and off. A high output from the latch turns the switch on; a low output turns it off. In normal operation the flip-flop is set high during the clock pulse, but gating keeps the latch output low until the clock pulse is over. The latch is reset when the PWM comparator output goes high.

enable (EN)

A logic low on EN puts the TPS6735 in shutdown mode. In shutdown, the output power switch, voltage reference, and other functions shut off and the supply current is reduced to 1-µA maximum. The soft-start capacitor is discharged through a 1.2-MΩ resistance and the output falls to zero volts.

error amplifier

The error amplifier is a high-gain differential amplifier used to regulate the converter output voltage. The amplifier generates an error signal, which is fed to the PWM comparator, by comparing a sample of the output voltage to the reference and amplifying the difference. The output sample is obtained from a resistive divider connected between FB and REF. FB is connected externally to the converter output, and the divider output is connected to the error-amplifier input. An 82-pF capacitor connected between COMP and GND is required to stabilize the control loop for loads greater than 100 mA.

oscillator and ramp generator

The oscillator circuit provides a 160-kHz clock to set the converter operating frequency, and a timing ramp for slope compensation. The clock waveform is a pulse, a few hundred nanoseconds in duration, that is used to limit the maximum power switch duty cycle to 95%. The timing ramp is summed with the current-sense signal at the input to the current-sense amplifier.

overcurrent comparator

The overcurrent comparator monitors the current in the power switch. The comparator trips and initiates a soft-start cycle if the power-switch current exceeds 2 A peak.

power switch

The power switch is a 0.4-Ω p-channel MOSFET with current sensing. The drain is connected to OUT and the current sense is connected to a resistor. The voltage across the resistor is proportional to current in the power switch and is tied to the overcurrent comparator and the current-sense amplifier. In normal operation, the power switch is turned on at the start of each clock cycle and turned off when the PWM comparator resets the drive latch.

PWM comparator

The comparator resets the drive latch and turns off the power switch whenever the slope-compensated current-sense signal from the current-sense amplifier exceeds the error signal.

reference

The 1.22-V reference is brought out on REF and can source 125-µA maximum to external loads. A 10-µF capacitor connected between REF and GND is recommended to minimize noise pickup.

SS clamp

The SS clamp circuit limits the signal level on error-amplifier output during start-up. The voltage on SS is amplified and used to override the error-amplifier output until it rises above that output, at which point the error amplifier takes over. This prevents the input to the PWM comparator from exceeding its common-mode range (i.e., error amplifier output too high to be reached by the current ramp) by limiting the maximum voltage on the error-amplifier output during start-up.

Soft start causes the output voltage to increase to the regulation point at the controlled rate. The voltage on the charging soft-start capacitor gradually raises the clamp on the error amplifier output voltage, limiting surge currents at power up by increasing the current limit threshold on a cycle-by-cycle basis. A soft-start cycle is initiated when either the enable (EN) signal is switched high or an overcurrent fault condition triggers the discharge of the soft-start capacitor.

undervoltage lockout (UVLO)

The supply voltage is fed through a voltage divider to the input of the UVLO and compared to a reference. The undervoltage-lockout logic prevents the MOSFET from turning on while the supply voltage is below the undervoltage-lockout voltage threshold, and once the supply voltage on V_{CC} is above the threshold, an SS cycle is initiated.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1175 mW	9.4 mW/°C	752 mW	611 mW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Pin voltages: V_{CC} (see Note 1) . . . . . −0.3 V to 7 V
OUT to V_{CC} . . . . . 12.5 V
FB (see Note 1) . . . . . 25 V
SS, COMP, EN voltage range (see Note 1) . . . . . −0.3 V to V_{CC} +0.3 V
Peak switch current . . . . . 2 A
Reference current . . . . . 2.5 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . −40°C to 85°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6mm (1/16 inch) from case for 10 s . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network terminal ground.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage	4		6.2	V
Decoupling capacitor		1		µF
Input capacitor		47		µF
Reference capacitor		10		µF
Output capacitor		100		µF
Compensation capacitor		82		pF
Inductor		10		µH

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5 V, I_O = 0, EN = 5 V, typical values are at T_A = 25°C (unless otherwise noted) (refer to Figure 15)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Supply current			1.9		mA
Standby current	EN = 0.4 V		1	10	μA
High-level input threshold voltage, EN				2	V
Low-level input threshold voltage, EN		0.4			V
Input current, EN		−1		1	μA
Compensation pin impedance			7.5		kΩ
Oscillator frequency			160		kHz
Reference voltage	$I_{O(ref)} \leq$ 125 μA		1.22		V
Reference drift			50		ppm/°C
Undervoltage lockout			3.7		V
On resistance, OUT			0.4		Ω
Leakage current, OUT			20		nA

performance characteristics over recommended operating free-air temperature range, typical values at T_A = 25°C (unless otherwise noted) (refer to Figure 15)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Output voltage	V_{CC} = 4.5 V to 6.2 V I_O = 0 mA to 200 mA	−4.75	−5	−5.25	V
Load current	V_{CC} = 4.5 V to 6.2 V	200	270		mA
Line regulation	V_{CC} = 4.5 V to 6.2 V		0.2%		
Load regulation	I_O = 25 mA to 200 mA		0.2%		
Efficiency	I_O =100 mA		78%		

APPLICATION INFORMATION

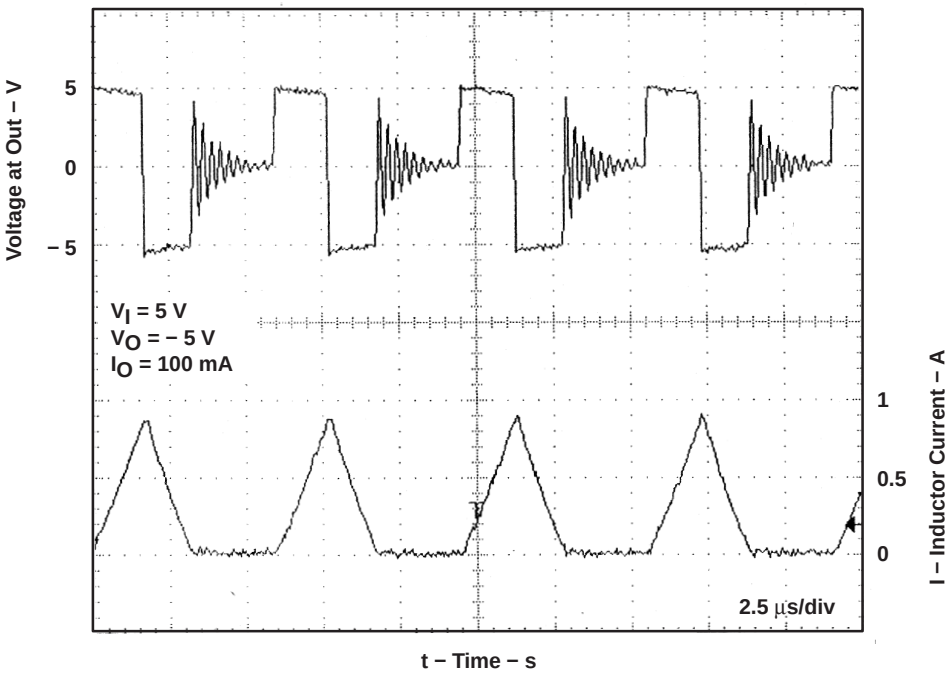


Figure 2. Switching Waveforms

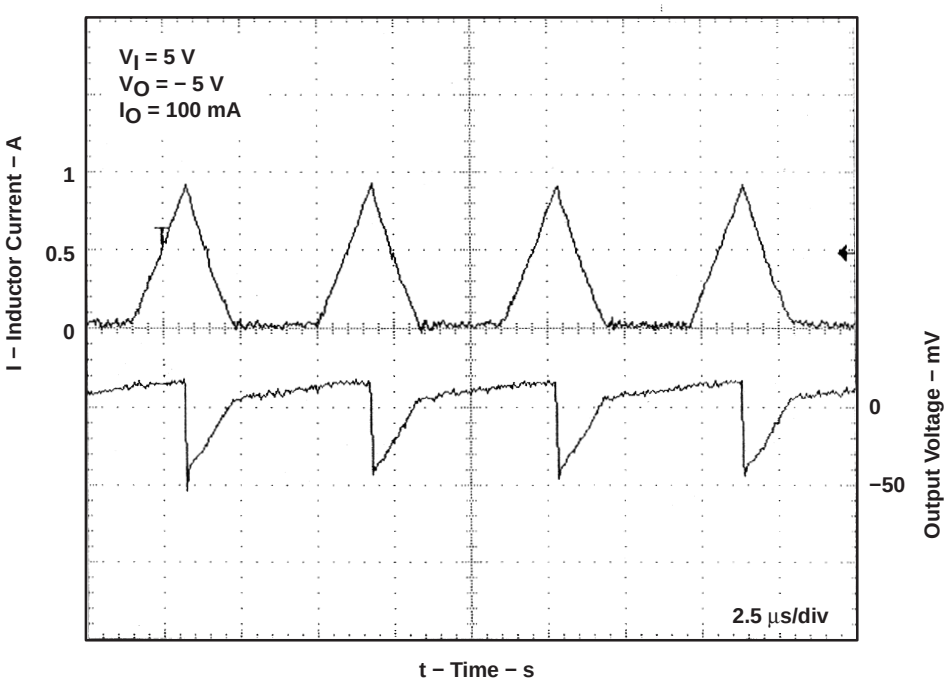


Figure 3. Output Voltage Ripple

APPLICATION INFORMATION

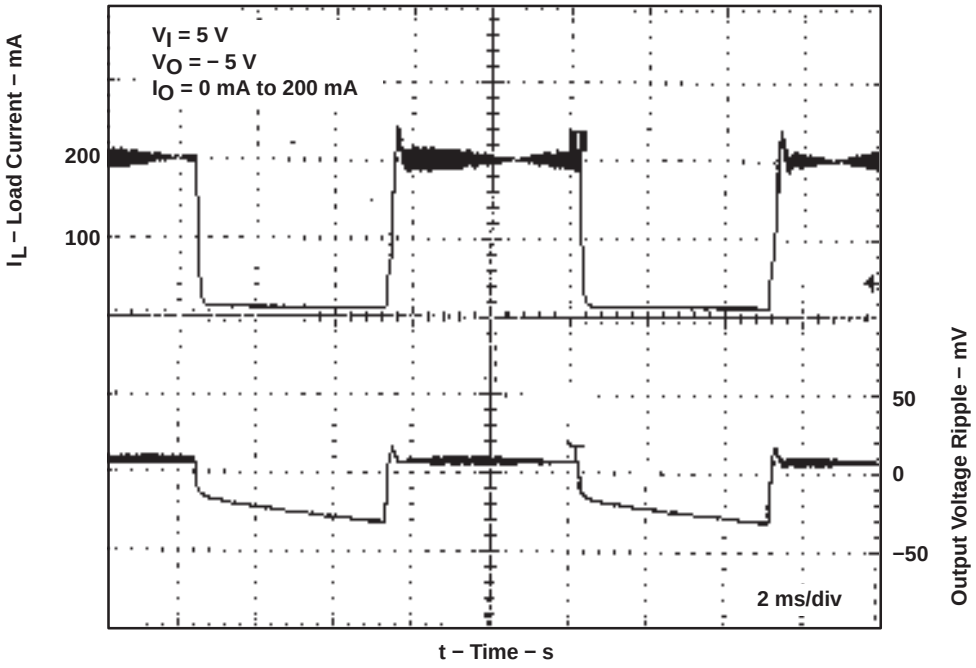


Figure 4. Load Transient Response

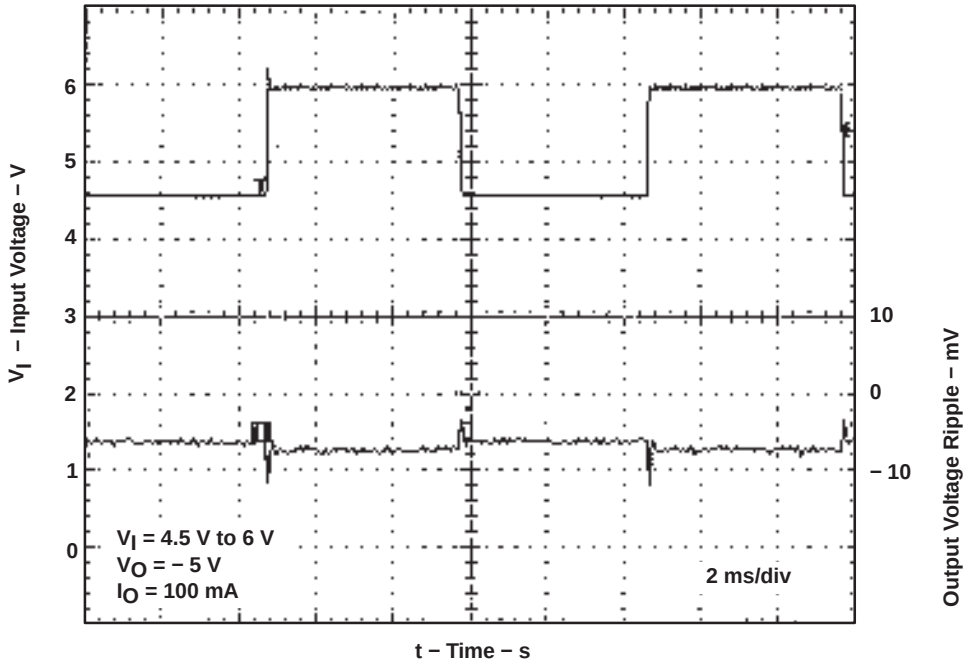


Figure 5. Line Transient Response

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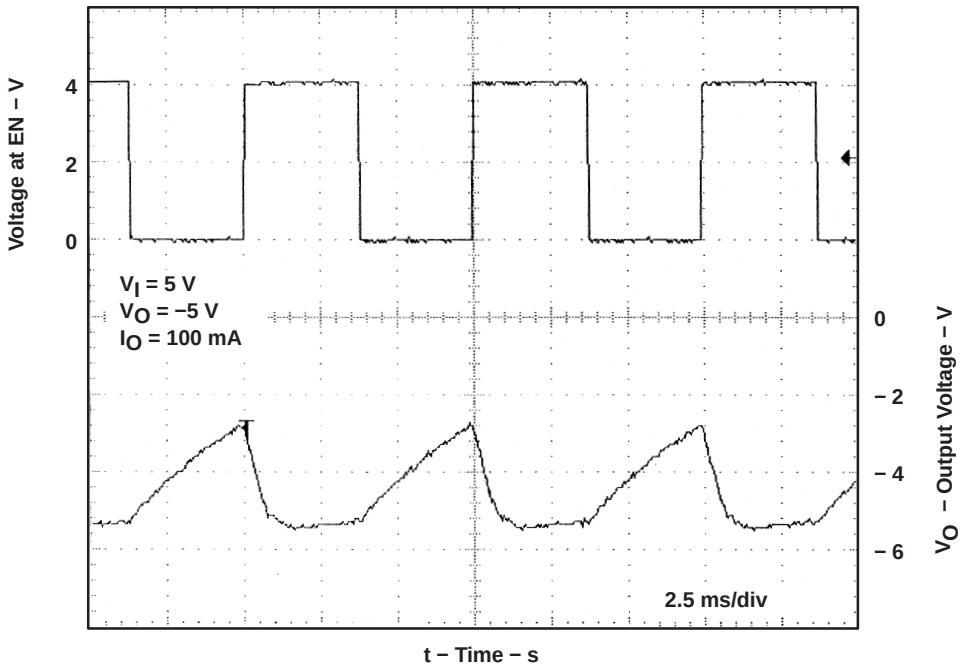

Figure 6. Enable Response Time

system typical characteristics

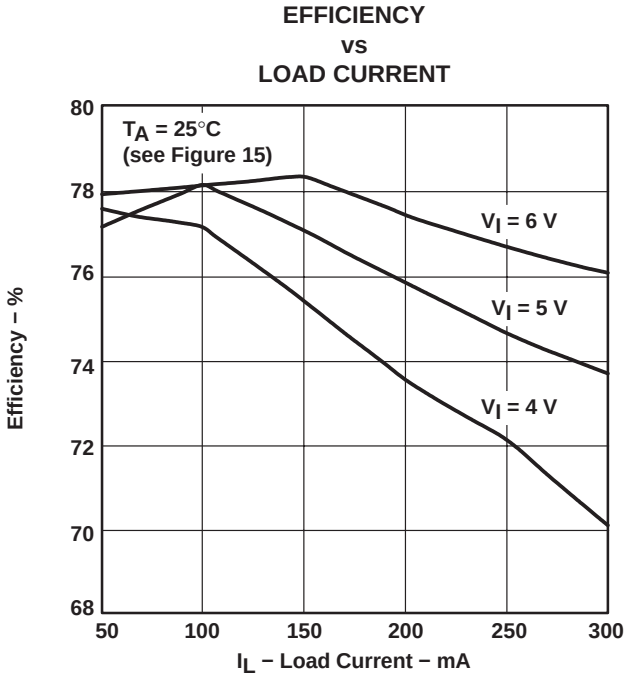

Figure 7

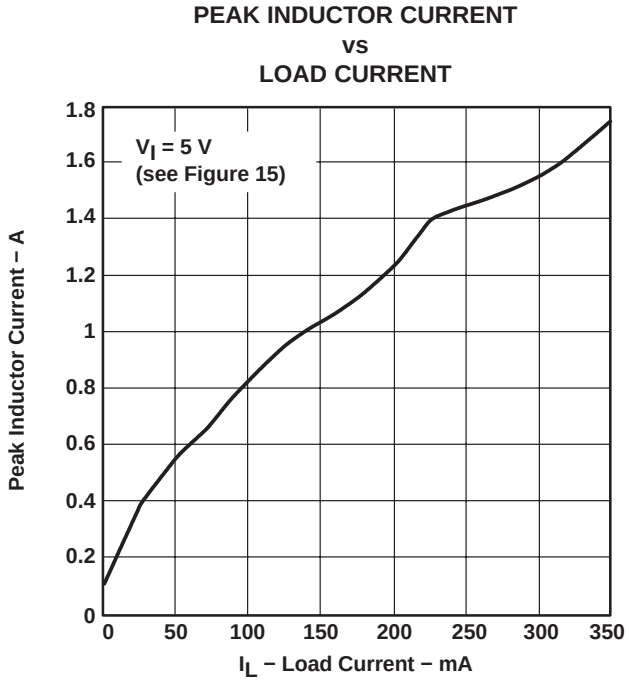

Figure 8

APPLICATION INFORMATION

system typical characteristics (continued)

NO-LOAD SUPPLY CURRENT
vs
SUPPLY VOLTAGE

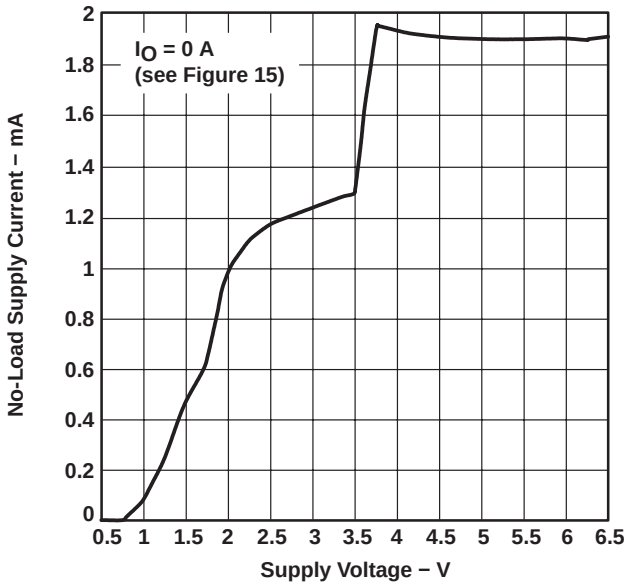

Figure 9

MAXIMUM LOAD CURRENT
vs
SUPPLY VOLTAGE

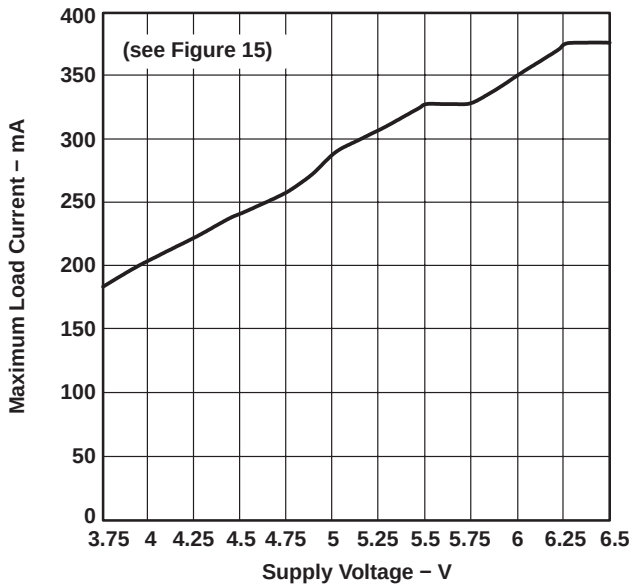

Figure 10

OSCILLATOR FREQUENCY
vs
TEMPERATURE

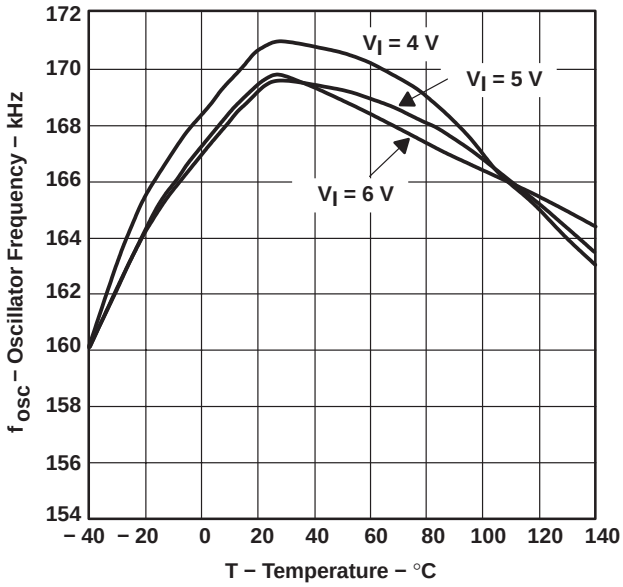

Figure 11

SWITCH CURRENT LIMIT
vs
SOFT-START VOLTAGE

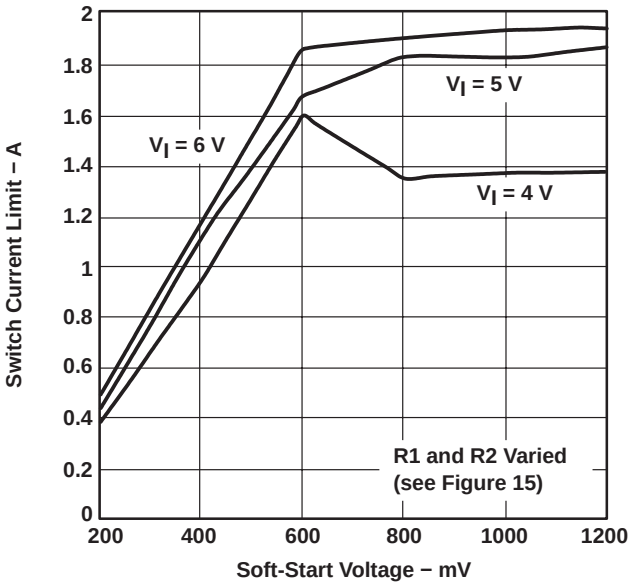

Figure 12

APPLICATION INFORMATION

system typical characteristics (continued)

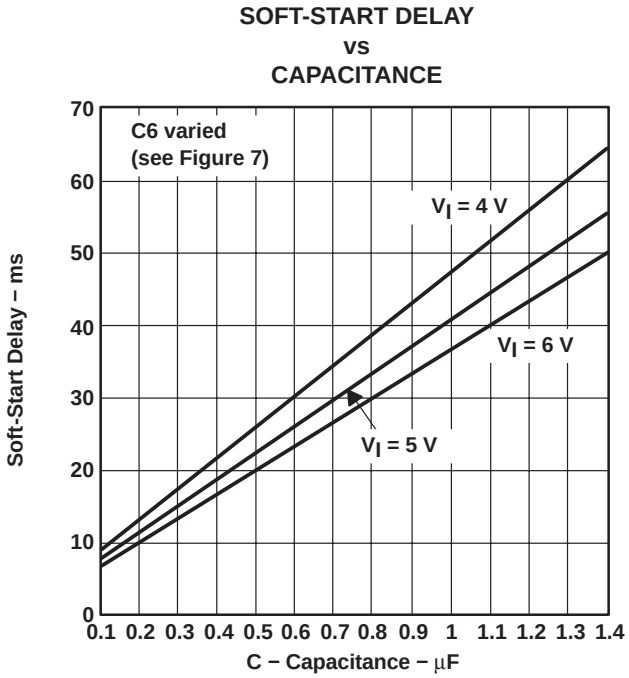

Figure 13

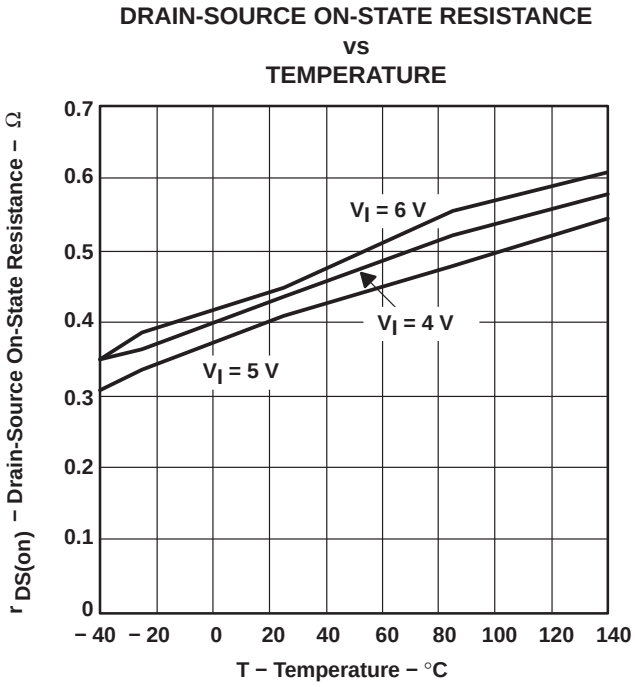

Figure 14

The TPS6735 operates in the voltage-inverting circuit, shown in Figure 15, which can generate a −5-V output. The circuit is ideal for applications that require a negative polarity voltage on the output with respect to the input ground, and for energy management systems. The TPS6735 can be placed in a shutdown mode (1-μA quiescent current) by forcing EN low.

soft start

The soft-start capacitor provides an orderly start-up of the converter by slowly increasing the switch current limit during power-up. The soft-start timing is controlled by the SS capacitance (see Figure 13 for the capacitance value corresponding to the desired delay time). The switch current limit is proportional to the voltage applied to SS, which is internally pulled to REF by a 1.2-MΩ resistor. SS can be externally pulled lower than REF to limit the switch current. A UVLO condition or an overcurrent condition initiates an SS cycle by discharging the SS capacitor to ground through an internal transistor. A minimum of a 10-nF capacitor must be connected to SS to current limit correctly.

inductor selection

The standard 10-μH inductor required by the TPS6735 must have a saturation current greater than the peak switch current at the desired maximum load. Operation over the full voltage range and current range is assured by the 10-μH inductor. To determine the required inductor staturation level, refer to the typical operating characteristics graph for peak inductor current versus load current (see Figure 8).

APPLICATION INFORMATION

output filter capacitor

A low equivalent series resistance (ESR) output filter capacitor is necessary to minimize the output-ripple voltage. An ESR of 100 mΩ limits the output ripple to 90 mV or less for output loads up to 200 mA.

rectifier

A Schottky diode or high-speed silicon rectifier should be used with a maximum continuous current rating of 1 A for operation up to full load (200 mA).

output ripple filtering

A low-pass filter may be added to the converter output to reduce the output voltage ripple (see Figure 15). The LC filter has a cutoff frequency of 7.2 kHz. The inductor filter must have a low resistance to avoid large output voltage drops. The output voltage ripple is reduced to 5 mV when the LC output filter is used. FB must be connected to the output node before the connection for the low-pass filter.

printed circuit board layout

A ground plane is recommended in a printed circuit board (PCB) layout to ensure quiet operation. Attention should be given to minimizing the lengths of the switching loops. Bypass capacitors should be placed as close to the TPS6735 as possible to prevent instability and noise pickup. V_{CC} and GND should be bypassed directly with a 1-μF ceramic capacitor and a large bypass capacitor (e.g. 47 μF) to maximize noise immunity. The TPS6735 should not be used with IC sockets, wire-wrap prototype boards, or other constructions that are susceptible to noise pick-up.

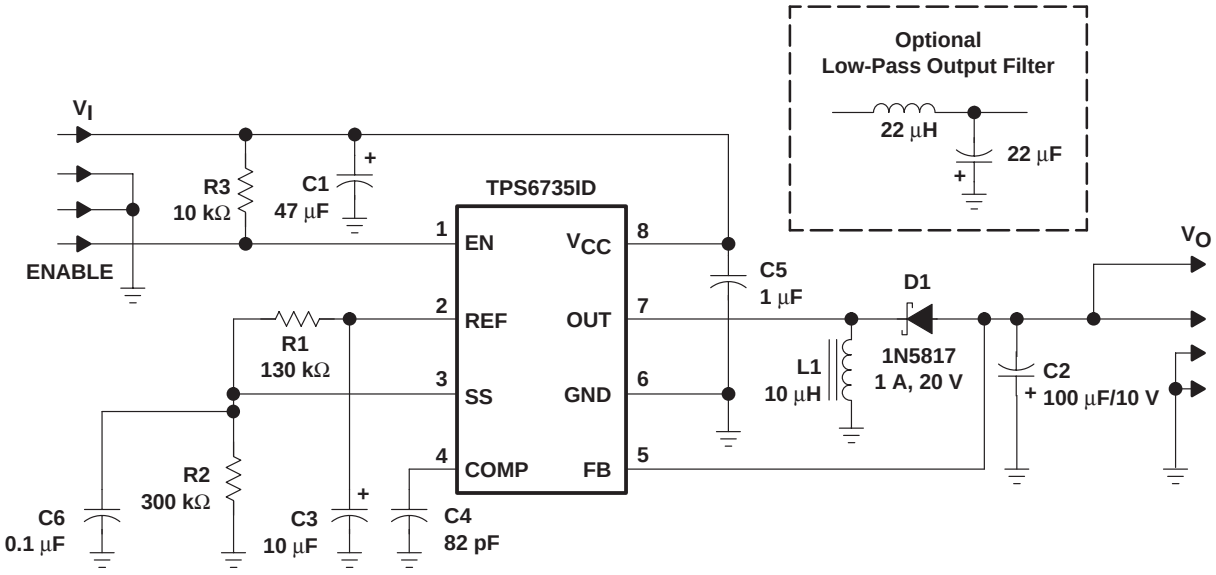

Figure 15. Application Circuit

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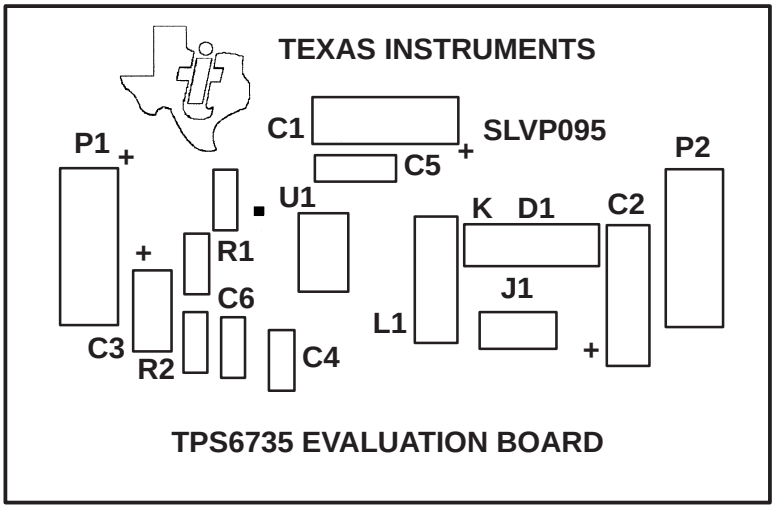
APPLICATION INFORMATION

Table 1. Bill of Materials

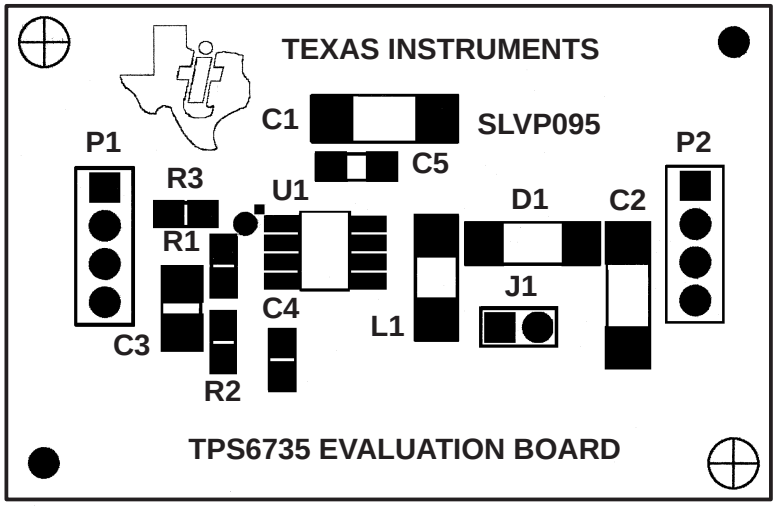
QTY	DESCRIPTION				REF DES	MANUFACTURER PART NO.	MANUFACTURER
1	IC	Power supply	−5 V		U1	TPS6735ID	Texas Instruments
1	Diode	Schottky			D1	1N5817GI	General Instrument
1	Inductor	10 µH			L1	DO1608C-103 CD54-100	Coilcraft, Sumida
1	Capacitor	47 µF tantalum	16 V	7343	C1	593D476X9016D2W TPSD476K016R0100	Sprague, AVX
1	Capacitor	100 µF tantalum	10 V	7343	C2	593D107X9010D2W TPSD107D016R0100	Sprague, AVX
1	Capacitor	10 µF tantalum	10 V	3528	C3	293D106X0010B2W 267E 1002 106	Sprague, MATSUO
1	Capacitor	82 pF ceramic	50 V	0805	C4		
1	Capacitor	1 µF ceramic	16 V	1206	C5		
1	Capacitor	0.1 µF ceramic	50 V	0805	C6		
1	Resistor	130 kΩ		0805	R1		
1	Resistor	300 kΩ		0805	R2		
1	Resistor	10 kΩ		0805	R3		



SILK SCREEN TOP

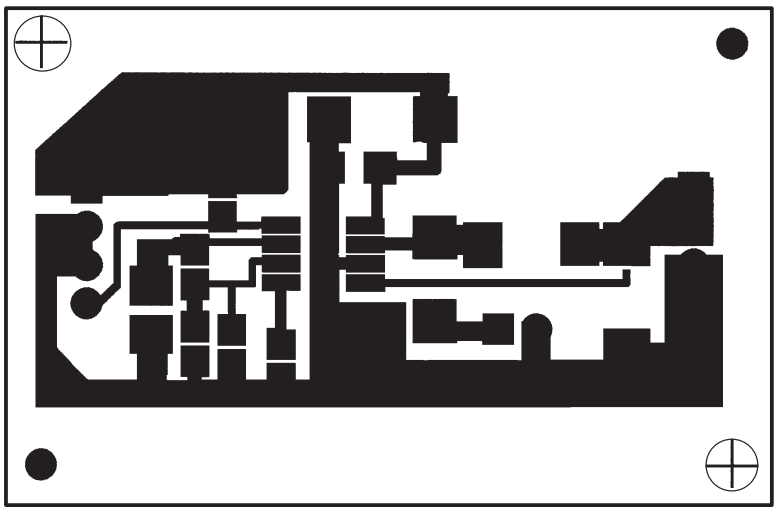
Figure 16. Component Placement

APPLICATION INFORMATION



SOLDER PASTE MASK

Figure 17. Solder Paste Mask



COMPONENT SIDE

Figure 18. PC Component Side

APPLICATION INFORMATION

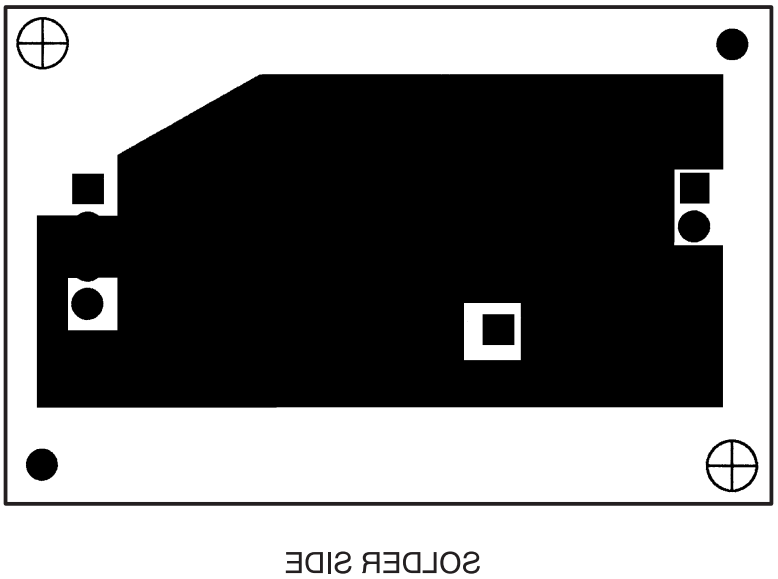
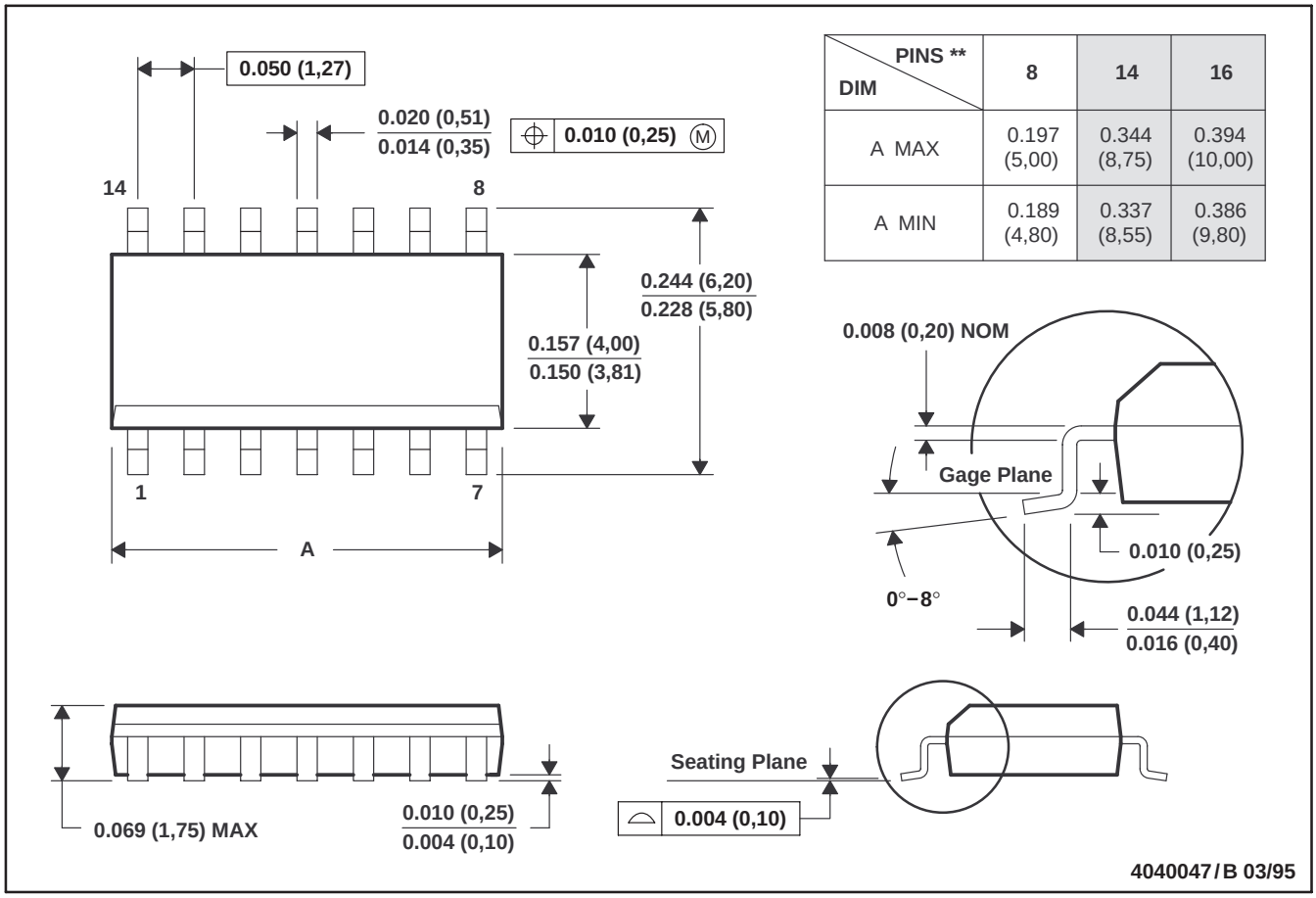


Figure 19. PC Wiring Side (Viewed From Component Side)

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN

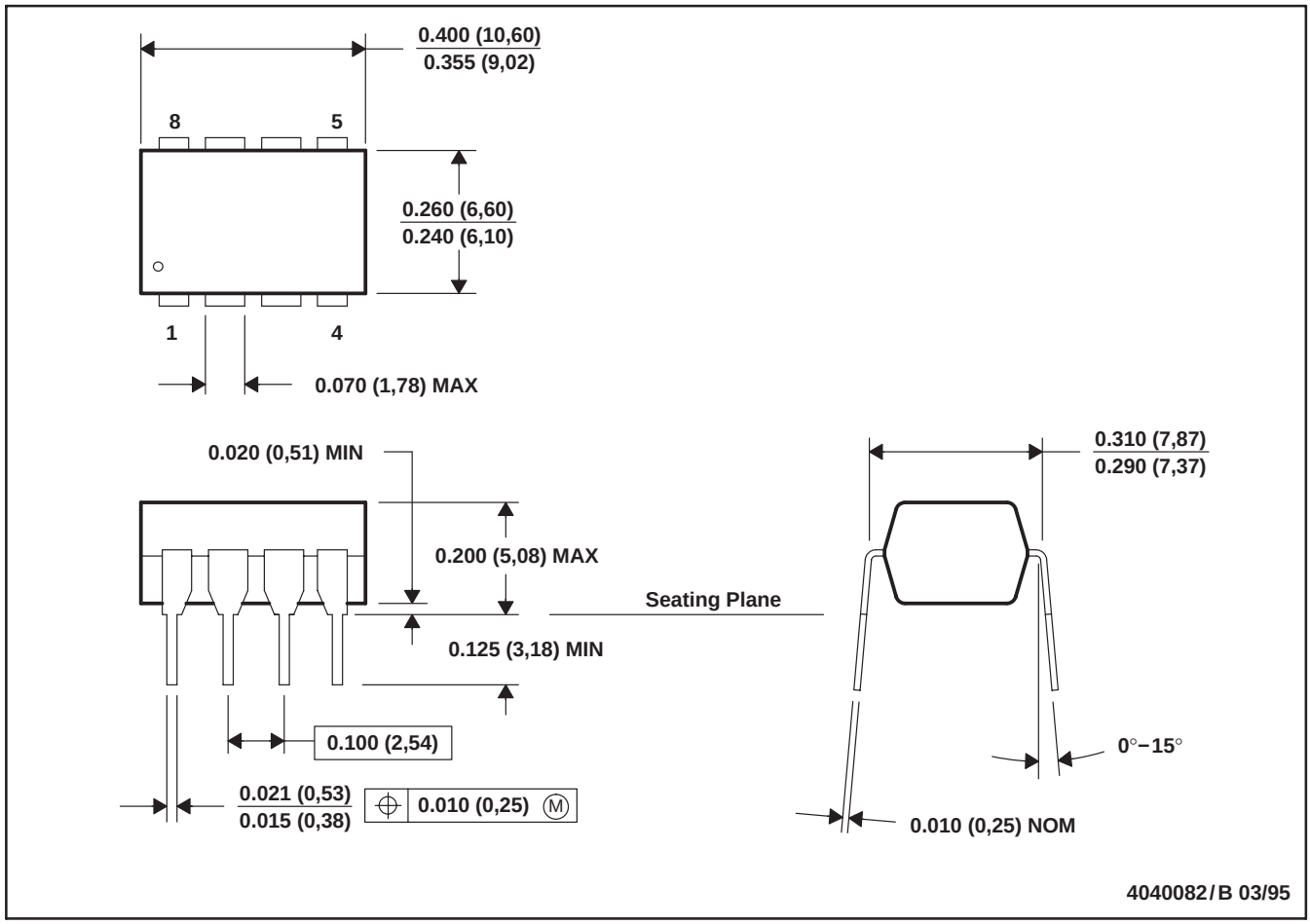


DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Four center pins are connected to die mount pad.
E. Falls within JEDEC MS-012

MECHANICAL DATA

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS6735ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6735I	Samples
TPS6735IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6735I	Samples
TPS6735IDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6735I	Samples
TPS6735IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TPS6735I	Samples
TPS6735IPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TPS6735I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

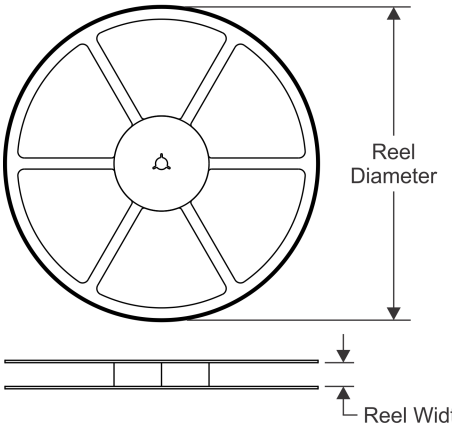
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

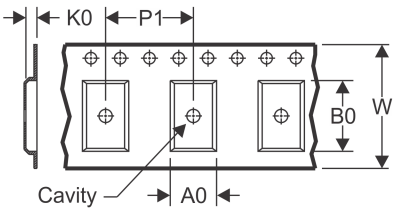
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

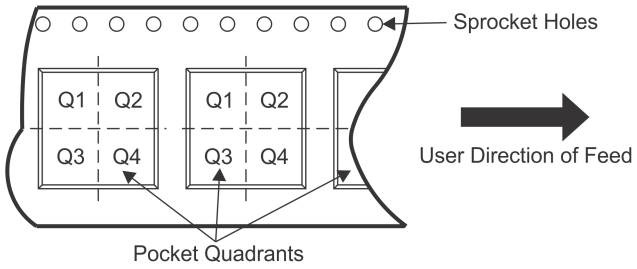


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

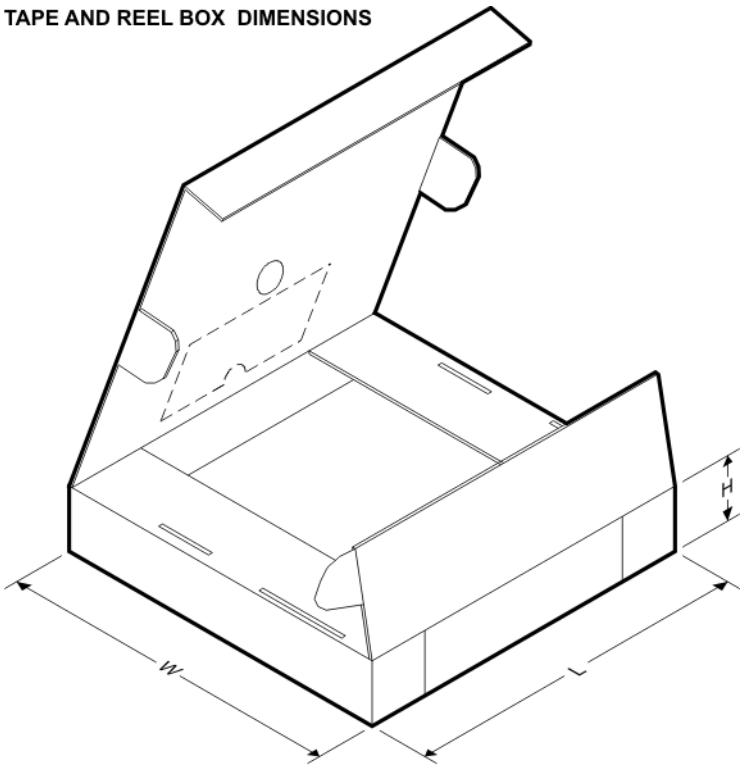
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS6735IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS6735IDR	SOIC	D	8	2500	350.0	350.0	43.0

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