74AHC123A-Q100; 74AHCT123A-Q100

Dual retriggerable monostable multivibrator with reset

Rev. 2 — 17 June 2020 Product data sheet

1. General description

The 74AHC123A-Q100; 74AHCT123A-Q100 is a dual retriggerable monostable multivibrator with reset. The basic output pulse width is programmed by selection of external components (R_{EXT} and C_{EXT}). Once triggered this basic pulse width may be extended by retriggering either of the edge triggered inputs ($n\overline{A}$ or (nB). By repeating this process, the output pulse period (nQ = HIGH, $n\overline{Q} = LOW$) can be made as long as desired. Alternatively, an output delay can be terminated at any time by a LOW-going edge on input $n\overline{R}D$. Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.0 V to 5.5 V
- · DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100 % duty factor
- Direct reset terminates output pulse
- Overvoltage tolerant inputs to 5.5 V
- All inputs have a Schmitt-trigger action
- High noise immunity
- Input levels:
 - For 74AHC123A-Q100: CMOS level
 - For 74AHCT123A-Q100: TTL level
- ESD protection:
 - MIL-STD-883, method 3015 exceeds 2000 V
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- · Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- · Multiple package options
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

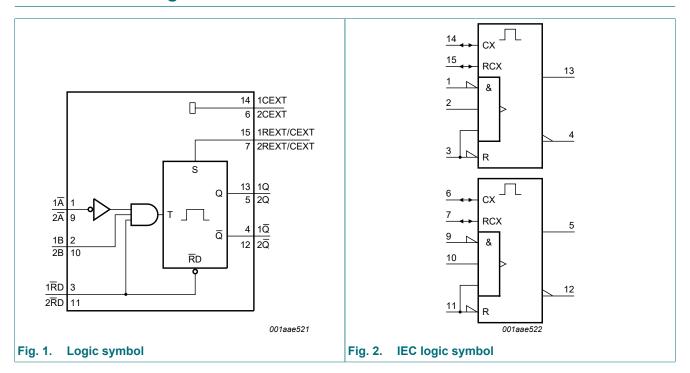


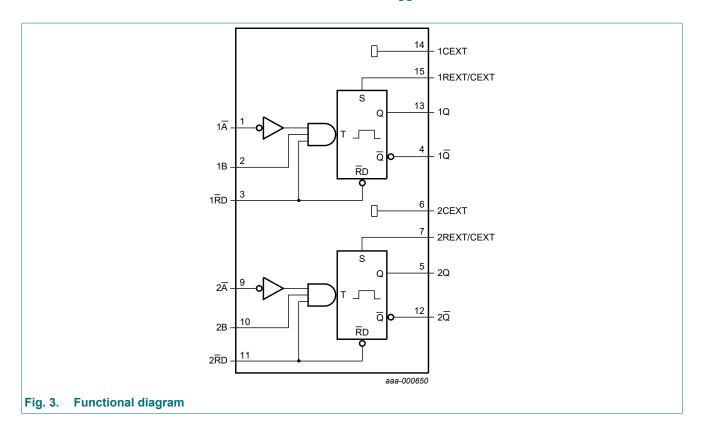
3. Ordering information

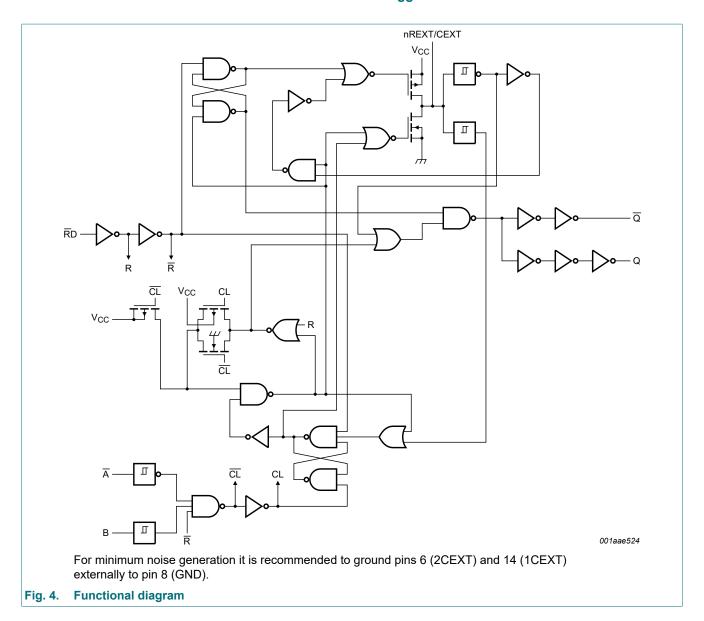
Table 1. Ordering information

Type number	Package								
	Temperature range	Name	Description	Version					
74AHC123AD-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads;	SOT109-1					
74AHCT123AD-Q100			body width 3.9 mm						
74AHC123APW-Q100	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package;	SOT403-1					
74AHCT123APW-Q100			16 leads; body width 4.4 mm						
74AHC123ABQ-Q100	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible	SOT763-1					
74AHCT123ABQ-Q100			thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm						

4. Functional diagram

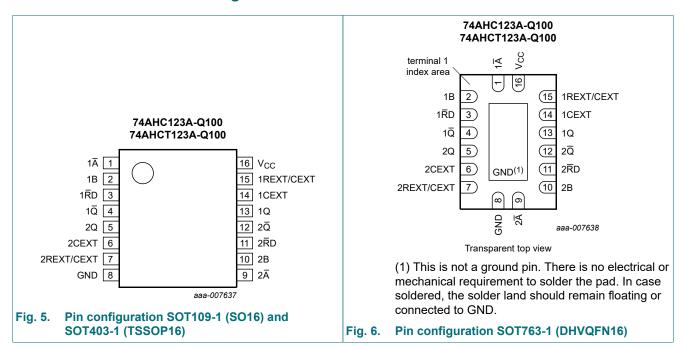






5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1Ā	1	negative-edge triggered input 1
1B	2	positive-edge triggered input 1
1RD	3	direct reset LOW and positive-edge triggered input 1
1Q	4	active LOW output 1
2Q	5	active HIGH output 2
2CEXT	6	external capacitor connection 2
2REXT/CEXT	7	external resistor and capacitor connection 2
GND	8	ground (0 V)
2 A	9	negative-edge triggered input 2
2B	10	positive-edge triggered input 2
2RD	11	direct reset LOW and positive-edge triggered input 2
2Q	12	active LOW output 2
1Q	13	active HIGH output 1
1CEXT	14	external capacitor connection 1
1REXT/CEXT	15	external resistor and capacitor connection 1
V _{CC}	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care;

↑ = LOW-to-HIGH transition;

↓ = HIGH-to-LOW transition;

 Π = one HIGH level output pulse;

I = one LOW level output pulse.

Input			Output					
nRD	nĀ	nB	nQ	nQ				
L	Х	Х	L	Н				
X	Н	Х	L [1]	H [1]				
X	Х	L	L [1]	H [1]				
Н	L	↑	Л	Ц				
Н	\	Н	Л	L				
\uparrow	L	Н	Л	T				

^[1] If the monostable multivibrator was triggered before this condition was established, the pulse will continue as programmed.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
VI	input voltage		-0.5	+7.0	V
I _{IK}	input clamping current	$V_{I} < -0.5 V$ [1]	-20	-	mA
I _{OK}	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$ [1]	-	±20	mA
Io	output current	$V_{O} = -0.5 \text{ V to } (V_{CC} + 0.5 \text{ V})$	-	±25	mA
I _{CC}	supply current		-	75	mA
I _{GND}	ground current		-75	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$ [2]	-	500	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

For SOT403-1 (TSSOP16) package: Ptot derates linearly with 8.5 mW/K above 91 °C.

For SOT763-1 (DHVQFN16) package: Ptot derates linearly with 11.2 mW/K above 106 °C.

^[2] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74Al	74AHC123A-Q100			74AHCT123A-Q100			
			Min	Тур	Max	Min	Тур	Max		
V _{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V	
VI	input voltage		0	-	5.5	0	-	5.5	V	
Vo	output voltage		0	-	V _{CC}	0	-	V _{CC}	V	
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C	
Δt/ΔV	input transition rise and	V _{CC} = 3.3 V ± 0.3 V	-	-	100	-	-	-	ns/V	
	fall rate	V _{CC} = 5.0 V ± 0.5 V	-	-	20	-	-	20	ns/V	

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C			°C to 5 °C	-40 °C to +125 °C		Unit
				Тур	Max	Min	Max	Min	Max	
74AHC1	23A-Q100		'				'	'		
V _{IH}	HIGH-level	V _{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V _{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V _{IL}	LOW-level	V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
	input voltage	V _{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V _{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I _O = -50 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -50 μA; V _{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I _O = -50 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I _O = -8.0 mA; V _{CC} = 4.5 V	3.94	-	-	3.8	-	3.70	-	V
V _{OL}	LOW-level	V _I = V _{IH} or V _{IL}								
	output voltage	I _O = 50 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_{O} = 4.0 mA; V_{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I _O = 8.0 mA; V _{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V

Symbol	Parameter	Conditions		1	25 °C			°C to 5 °C	-40 °C to +125 °C		Unit
			М	lin	Тур	Max	Min	Max	Min	Max	-
l _l	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V									
		nREXT/CEXT	[1]	-	-	±0.25	-	±2.5	-	±10.0	μΑ
		pins nĀ, nB, nĀD		-	-	±0.1	-	±1.0	-	±2.0	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	-	4.0	-	40	-	80	μΑ
		active state (per circuit); V _I = V _{CC} or GND	[1]								
		V _{CC} = 3.0 V		-	160	250	-	280	-	280	μΑ
		V _{CC} = 4.5 V		-	380	500	-	650	-	650	μΑ
		V _{CC} = 5.5 V		-	560	750	-	975	-	975	μΑ
Cı	input capacitance		-	-	5.0	10	-	10	-	10	pF
Co	output capacitance		-	-	4.0	-	-	-	-	-	pF
74AHCT	123A-Q100								ı		
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.	.0	-	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	-	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$									
	output voltage	Ι _Ο = -50 μΑ	4.	.4	4.5	-	4.4	-	4.4	-	V
		I _O = -8.0 mA	3.9	94	-	-	3.8	-	3.70	-	V
V_{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$									
	output voltage	Ι _Ο = 50 μΑ		-	0	0.1	-	0.1	-	0.1	V
		I _O = 8.0 mA		-	-	0.36	-	0.44	-	0.55	V
l _l	input leakage current	nREXT/CEXT; V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	[1]	-	-	±0.25	-	±2.5	-	±10.0	μΑ
		pins n \overline{A} , nB, n $\overline{R}D$; V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	-	±0.1	-	±1.0	-	±2.0	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	-	4.0	-	40	-	80	μΑ
		active state (per circuit); V _I = V _{CC} or GND	[1]								
		V _{CC} = 4.5 V		-	380	500	-	650	-	650	μΑ
		V _{CC} = 5.5 V		-	560	750	-	975	-	975	μΑ
Cı	input capacitance		-	-	3	10	-	10	-	10	pF
C _O	output capacitance			-	4.0	-	-	-	-	-	pF

^[1] Voltage on nREXT/CEXT = $0.5 \times V_{CC}$ and pin nREXT/CEXT in OFF-state during test.

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; For test circuit see Fig. 12.

Symbol	Parameter	Conditions		25 °C		-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	1
74AHC1	23A-Q100									
t _{pd}	propagation	$n\overline{A}$ and nB to nQ and $n\overline{Q}$; see Fig. 7 [2]								
	delay	V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF	-	7.4	20.6	1.0	24.0	1.0	26.0	ns
		V _{CC} = 3.0 V to 3.6 V; C _L = 50 pF	-	10.5	24.1	1.0	27.5	1.0	30.0	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	-	5.1	12.0	1.0	14.0	1.0	15.5	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	-	7.3	14.0	1.0	16.0	1.0	17.5	ns
		\overline{nRD} to \overline{nQ} and \overline{nQ} ; see $\overline{\underline{Fig. 7}}$ [2]								
		V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF	-	8.2	22.4	1.0	26.0	1.0	28.0	ns
		V _{CC} = 3.0 V to 3.6 V; C _L = 50 pF	-	11.7	25.9	1.0	29.5	1.0	32.0	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	-	5.6	12.9	1.0	15.0	1.0	16.5	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	-	8.1	14.9	1.0	17.0	1.0	19.0	ns
		\overline{nRD} to \overline{nQ} and \overline{nQ} (reset); see Fig. 7 [2]								
		V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF	-	6.4	15.8	1.0	18.5	1.0	20.0	ns
		V _{CC} = 3.0 V to 3.6 V; C _L = 50 pF	-	9.2	19.3	1.0	22.0	1.0	24.5	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	-	4.4	9.4	1.0	11.0	1.0	12.0	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	-	6.3	11.4	1.0	13.0	1.0	14.5	ns
t _W	pulse width	inputs; nA = LOW; see Fig. 7								
		V _{CC} = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.0	-	ns
		V _{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
		inputs; nB = HIGH; see Fig. 7								
		V _{CC} = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.0	-	ns
		V _{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
		inputs; nRD = LOW; see Fig. 7								
		V _{CC} = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.0	-	ns
		V _{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
		outputs; $n\overline{Q}$ = LOW and [3] nQ = HIGH; C_L = 50 pF; see Fig. 7, Fig. 8, Fig. 9 and Fig. 10								
		C_{EXT} = 28 pF; R_{EXT} = 2 k Ω								
		V _{CC} = 3.0 V to 3.6 V	-	115	240	-	300	-	300	ns
		V _{CC} = 4.5 V to 5.5 V	-	100	200	-	240	-	240	ns
		$C_{EXT} = 0.01 \mu F; R_{EXT} = 10 k\Omega$								
		V _{CC} = 3.0 V to 3.6 V	90	100	110	90	110	85	115	μs
		V _{CC} = 4.5 V to 5.5 V	90	100	110	90	110	85	115	μs
		$C_{EXT} = 0.1 \mu F; R_{EXT} = 10 k\Omega;$								1
		V _{CC} = 3.0 V to 3.6 V	0.9	1	1.1	0.9	1.1	0.85	1.15	ms
		V _{CC} = 4.5 V to 5.5 V	0.9	1	1.1	0.9	1.1	0.85	1.15	ms

Symbol	Parameter	Conditions		25 °C			°C to 5 °C	-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t _{rtrig}	retrigger time	$n\overline{A}$ to nB; C _{EXT} = 100 pF; R _{EXT} = 1 kΩ; C _L = 50 pF; see <u>Fig. 8</u> and <u>Fig. 10</u>								
		V _{CC} = 3.0 V to 3.6 V	-	60	-	-	-	-	-	ns
		V _{CC} = 4.5 V to 5.5 V	-	39	-	-	-	-	-	ns
		$n\overline{A}$ to nB; C_{EXT} = 0.01 μF; R_{EXT} = 1 kΩ; C_L = 50 pF; see Fig. 8 and Fig. 10								
		V _{CC} = 3.0 V to 3.6 V	-	1.5	-	-	-	-	-	μs
		V _{CC} = 4.5 V to 5.5 V	-	1.2	-	-	-	-	-	μs
C _{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 1 MHz; [4] V_I = GND to V_{CC}	-	57	-	-	-	-	-	pF
74AHCT	123A-Q100									
t _{pd}	propagation	$n\overline{A}$ and nB to nQ and $n\overline{Q}$; see Fig. 7 [2]								
	delay	V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	-	5.0	12.0	1.0	14.0	1.0	15.5	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	-	7.1	14.0	1.0	16.0	1.0	17.5	ns
		\overline{nRD} to \overline{nQ} and \overline{nQ} ; see $\overline{Fig. 7}$								
		V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	-	5.2	12.9	1.0	15.0	1.0	16.5	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	-	7.5	14.9	1.0	17.0	1.0	18.5	ns
		nRD to nQ and nQ (reset); see Fig. 7 [2]								
		V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	-	4.7	9.4	1.0	11.0	1.0	12.0	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	-	6.7	11.4	1.0	13.0	1.0	14.5	ns
t _W	pulse width	inputs; $n\overline{A}$ = LOW; C_L = 50 pF; see Fig. 7								
		V _{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
		inputs; nB = HIGH; C _L = 50 pF; see Fig. 7								
		V _{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
		inputs; $n\overline{R}D = LOW$; $C_L = 50 pF$; see Fig. 7								
		V _{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
		outputs; $n\overline{Q}$ = LOW and [3] nQ = HIGH; C_L = 50 pF; C_{EXT} = 28 pF; R_{EXT} = 2 k Ω ; see Fig. 7, Fig. 8, Fig. 9 and Fig. 10								
		V _{CC} = 4.5 V to 5.5 V	-	100	200	-	240	-	240	ns
		$C_{EXT} = 0.01 \mu F; R_{EXT} = 10 k\Omega$								
		V _{CC} = 4.5 V to 5.5 V	90	100	110	90	110	85	115	μs
		$C_{EXT} = 0.1 \mu F; R_{EXT} = 10 k\Omega$								
		V _{CC} = 4.5 V to 5.5 V	0.9	1	1.1	0.9	1.1	0.85	1.15	ms

Symbol	Parameter	Conditions		25 °C			-40 °C to +85 °C		-40 °C to +125 °C	
				Typ[1]	Max	Min	Max	Min	Max	1
t _{rtrig}	retrigger time	$n\overline{A}$ to nB; C_{EXT} = 100 pF; R_{EXT} = 1 k Ω ; C_L = 50 pF; see Fig. 8 and Fig. 10								
		V _{CC} = 4.5 V to 5.5 V	-	60	-	-	-	-	-	ns
		n \overline{A} to nB; C _{EXT} = 0.01 μF; R _{EXT} = 1 k Ω ; C _L = 50 pF; see Fig. 8 and Fig. 10								
		V _{CC} = 4.5 V to 5.5 V	-	1.5	-	-	-	-	-	μs
C _{PD}	power dissipation capacitance	$C_L = 50 \text{ pF}; f_i = 1 \text{ MHz};$ [4] $V_I = \text{GND to } V_{CC}$	-	58	-	-	-	-	-	pF
External	components		'							'
R _{EXT}	external	V _{CC} = 2.0 V	5	-	-	-	-	-	-	kΩ
	resistance	V _{CC} > 3.0 V	1	-	-	-	-	-	-	kΩ
C _{EXT}	external	$V_{CC} = 2.0 \text{ V}$ [5]	-	-	-	-	-	-	-	pF
	capacitance	$V_{CC} > 3.0 \text{ V}$ [5]	-	-	-	-	-	-	-	pF

- Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).
- [2] t_{pd} is the same as t_{PLH} and t_{PHL}; C_{EXT} = 0 pF; R_{EXT} = 5 kΩ.
 [3] For C_{EXT} ≥ 10 nF the typical value of the pulse width t_W (μs) = C_{EXT} (nF) × R_{EXT} (kΩ).
 [4] C_{PD} is used to determine the dynamic power dissipation P_D (μW).
 P_D = C_{PD} × V_{CC}² × f_i + Σ(C_L × V_{CC}² × f_o) where:

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$$
 where:

 f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V.

[5] C_{EXT} has no limits.

10.1. Waveforms

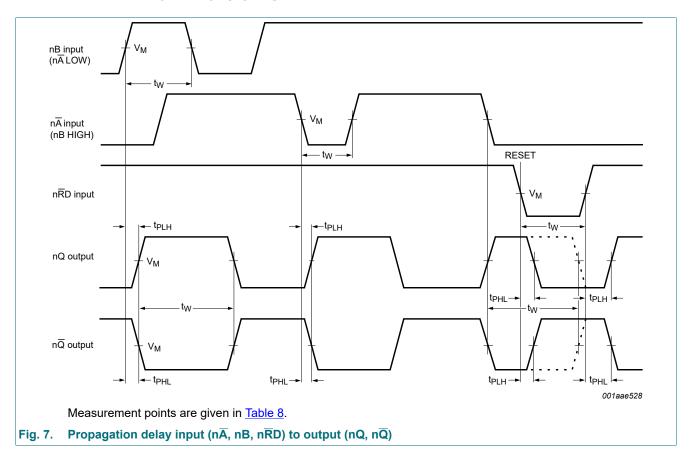
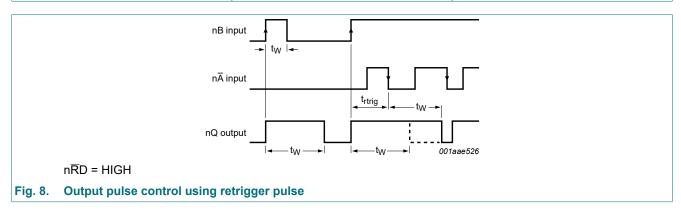
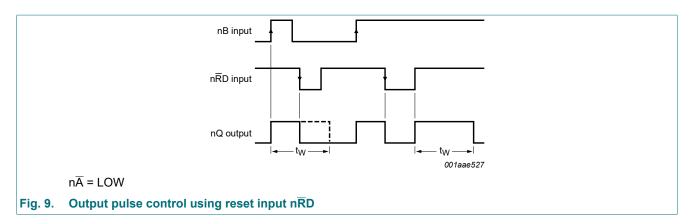
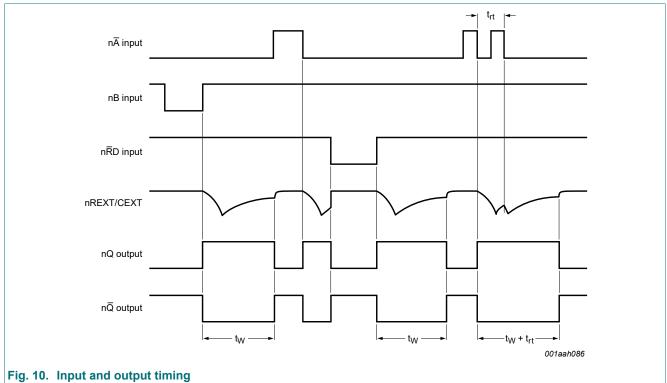


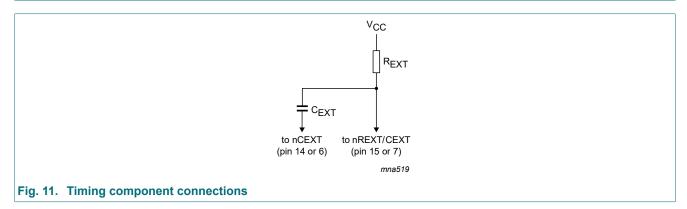
Table 8. Measurement points

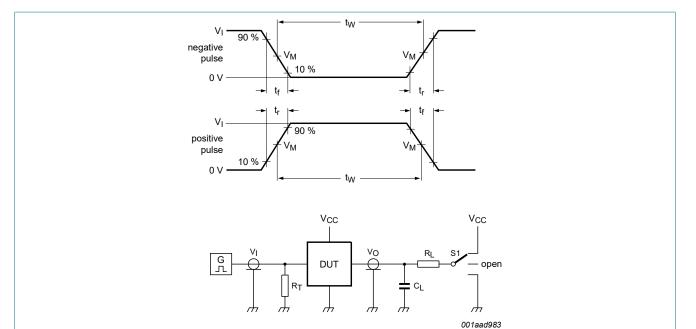
Туре	Input	Output
	V _M	V _M
74AHC123A-Q100	0.5V _{CC}	0.5V _{CC}
74AHCT123A-Q100	1.5 V	0.5V _{CC}











Test data is given in Table 9.

Definitions test circuit:

 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator

C_L = Load capacitance including jig and probe capacitance

R_I = Load resistance

S1 = Test selection switch

Fig. 12. Test circuit for measuring switching times

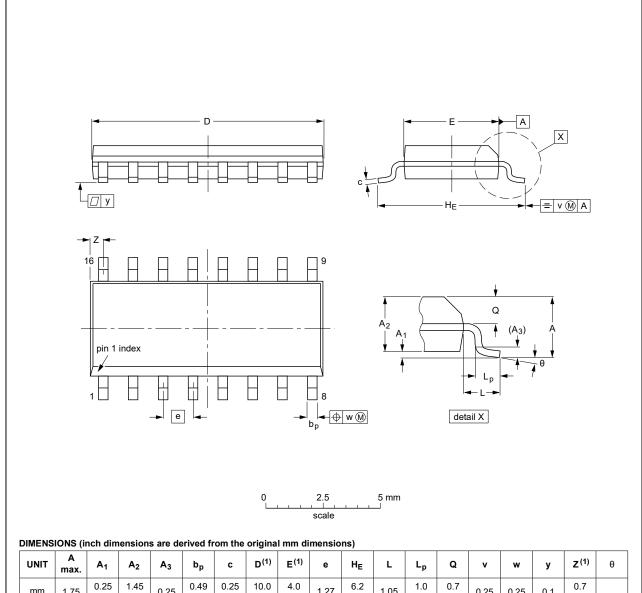
Table 9. Test data

Туре	Input		Load		S1 position			
	V _I	t _r , t _f	C _L R _L t _P		t _{PHL} , t _{PLH}	t _{PZH} , t _{PHZ}	t_{PZL}, t_{PLZ}	
74AHC123A-Q100	V _{CC}	3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V _{CC}	
74AHCT123A-Q100	3.0 V	3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V _{CC}	

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	0°

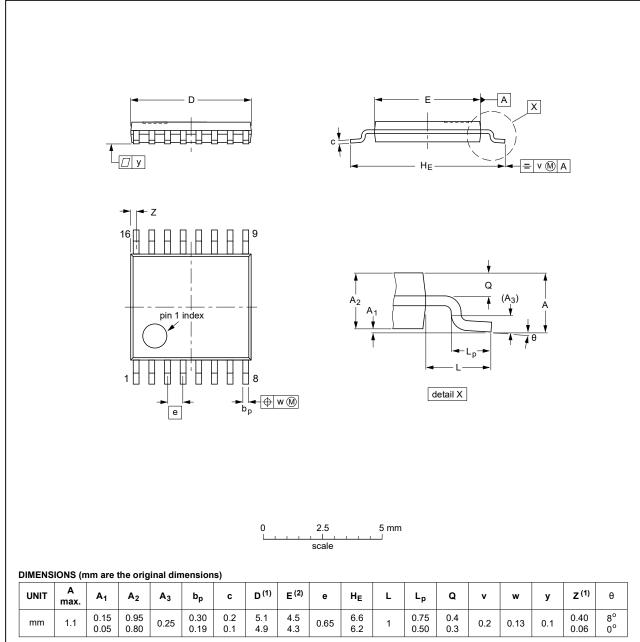
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT109-1	076E07	MS-012				99-12-27 03-02-19	

Fig. 13. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT403-1		MO-153				99-12-27 03-02-18	

Fig. 14. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm SOT763-1

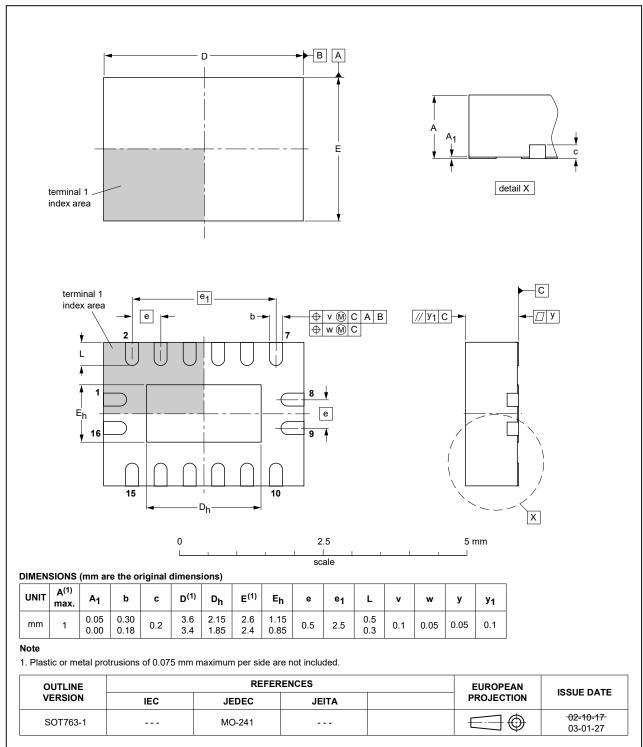


Fig. 15. Package outline SOT763-1 (DHVQFN16)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged-Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT123A_Q100 v.2	20200617	Product data sheet	-	74AHC_AHCT123A_Q100 v.1
Modifications:	guidelines of Nexperia.		n redesigned to comply with the identity new company name where appropriate. power dissipation updated.	
74AHC_AHCT123A_Q100 v.1	20130523	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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