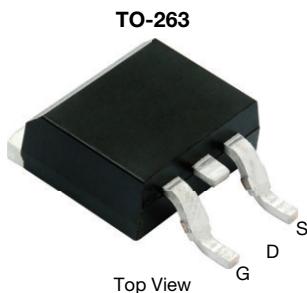


P-Channel 80 V (D-S) MOSFET



Top View

FEATURES

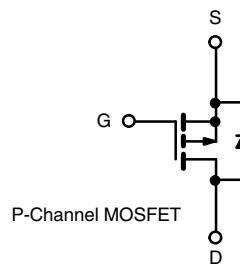
- TrenchFET® power MOSFET
- Package with low thermal resistance
- Maximum 175 °C junction temperature
- Low $R_{DS(on)}$ minimizes power loss from conduction
- Compatible with logic-level gate driving
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Battery protection
- Motor drive control
- Load switch



PRODUCT SUMMARY

V_{DS} (V)	-80
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -10$ V	0.0061
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -4.5$ V	0.0086
Q_g typ. (nC)	145
I_D (A)	-150
Configuration	Single

ORDERING INFORMATION

Package	TO-263
Lead (Pb)-free and halogen-free	SUM60061EL-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	-80	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current ^d ($T_J = 175$ °C)	I_D	-150 ^d	A
		-150 ^d	
Pulsed drain current (100 μ s)	I_{DM}	-250	
Avalanche current	I_{AS}	-75	
Single pulse avalanche energy ^a	E_{AS}	281	mJ
Power dissipation	P_D	375	
		125	W
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +175	°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	R_{thJA}	40	°C/W
Junction-to-case	R_{thJC}	0.4	

Notes

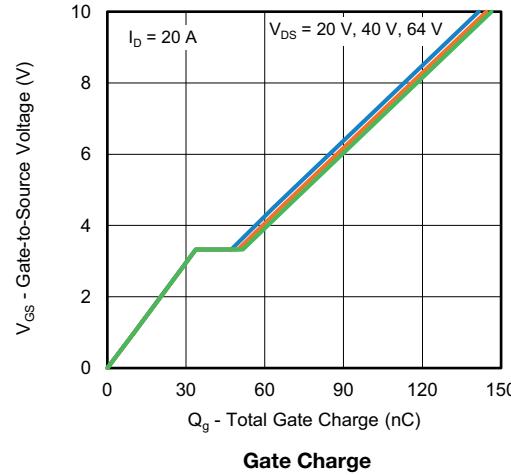
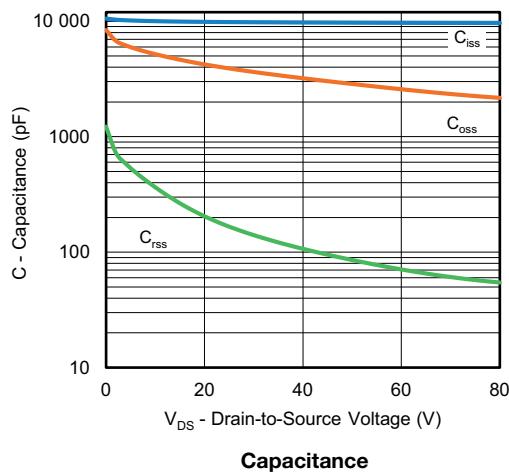
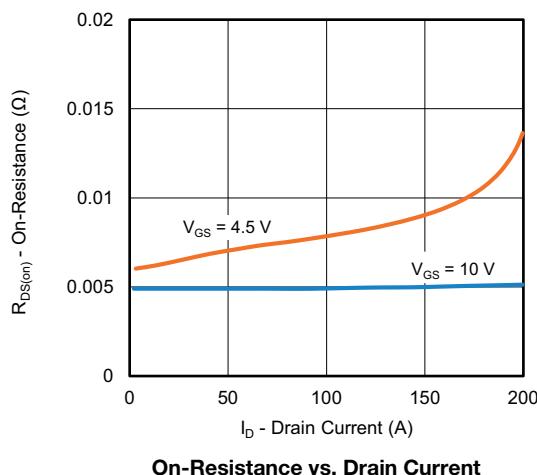
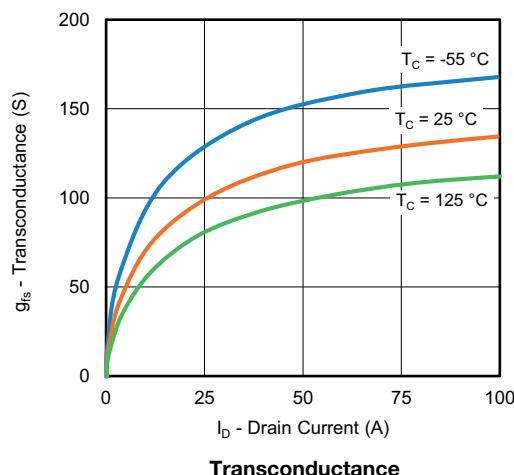
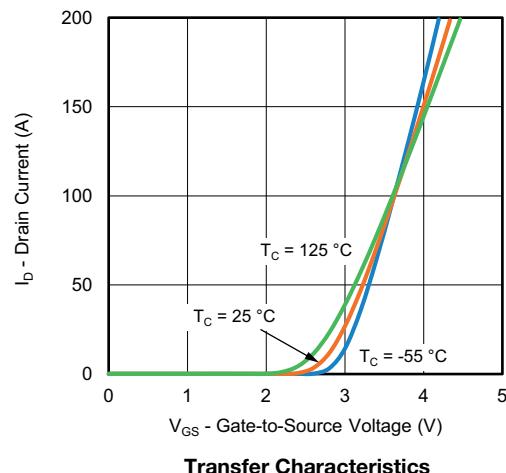
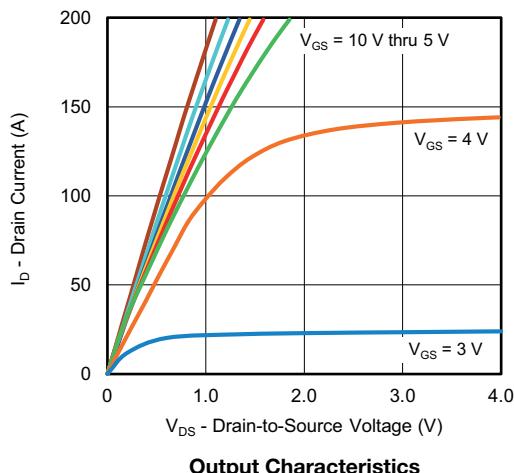
- Duty cycle ≤ 1 %
- When mounted on 1" square PCB (FR4 material)
- See SOA curve for voltage derating
- Limited by package

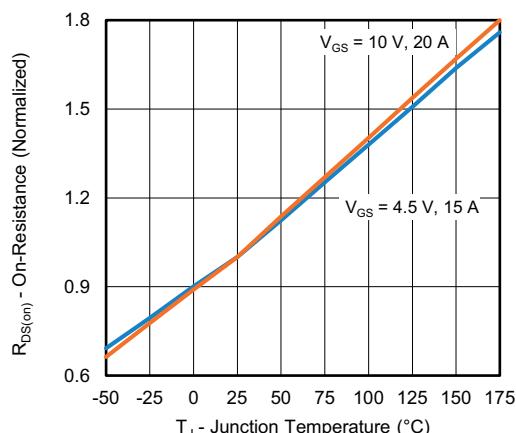
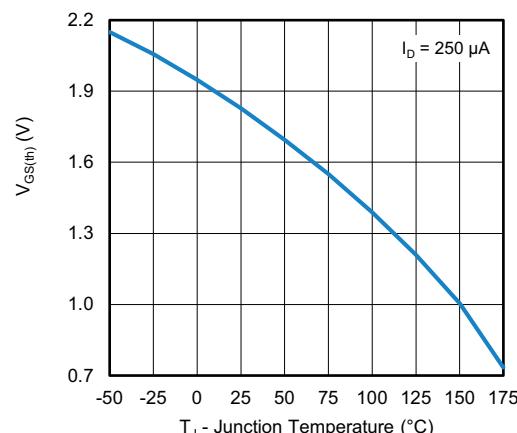
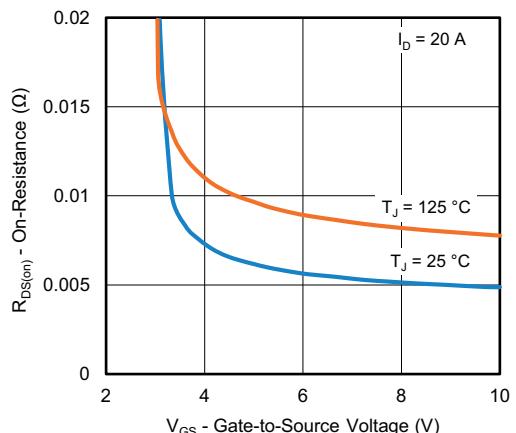
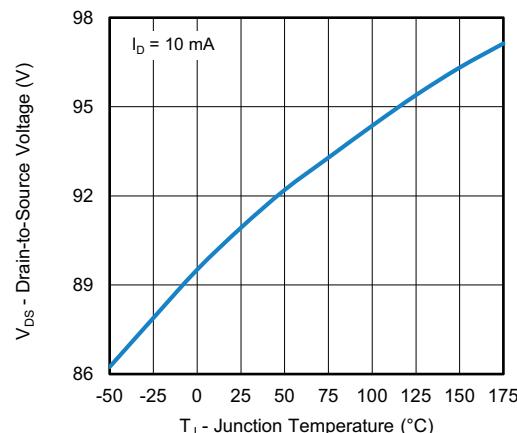
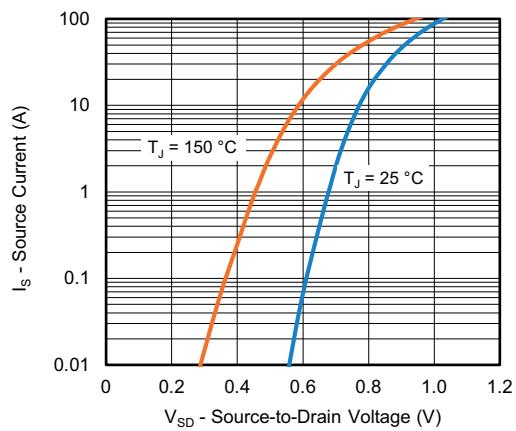
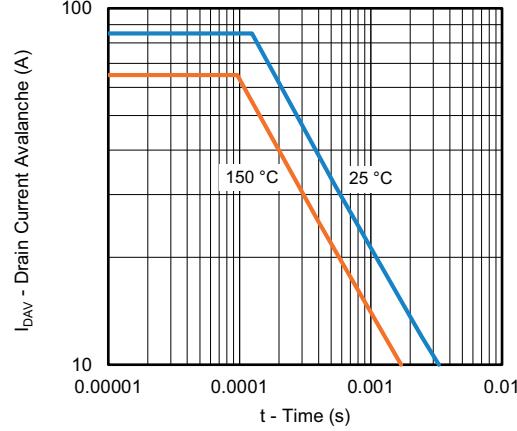
SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = -10 \text{ mA}$	-80	-	-	V
Gate threshold voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = -250 \mu\text{A}$	-1.5	-	-2.5	
Gate-body leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = -80 \text{ V}$, $V_{GS} = 0 \text{ V}$	-	-	-1	
		$V_{DS} = -80 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 125^\circ\text{C}$	-	-	-50	μA
		$V_{DS} = -80 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 175^\circ\text{C}$	-	-	-250	
On-state drain current ^a	$I_{D(\text{on})}$	$V_{DS} \leq -5 \text{ V}$, $V_{GS} = -10 \text{ V}$	-30	-	-	A
Drain-source on-state resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = -10 \text{ V}$, $I_D = -20 \text{ A}$	-	0.0051	0.0061	Ω
		$V_{GS} = -4.5 \text{ V}$, $I_D = -15 \text{ A}$	-	0.0069	0.0086	
Forward transconductance ^a	g_{fs}	$V_{DS} = -15 \text{ V}$, $I_D = -15 \text{ A}$	-	80	-	S
Dynamic ^b						
Input capacitance	C_{iss}	$V_{GS} = 0 \text{ V}$, $V_{DS} = -40 \text{ V}$, $f = 1 \text{ MHz}$	-	9600	-	
Output capacitance	C_{oss}		-	3300	-	pF
Reverse transfer capacitance	C_{rss}		-	110	-	
Total gate charge ^c	Q_g	$V_{DS} = -40 \text{ V}$, $V_{GS} = -10 \text{ V}$, $I_D = -110 \text{ A}$	-	145	218	
Gate-source charge ^c	Q_{gs}		-	34	-	nC
Gate-drain charge ^c	Q_{gd}		-	16	-	
Gate resistance	R_g		$f = 1 \text{ MHz}$	0.46	2.3	4.6
Turn-on delay time ^c	$t_{d(\text{on})}$	$V_{DD} = -40 \text{ V}$, $R_L = 0.71 \Omega$ $I_D \equiv -20 \text{ A}$, $V_{GEN} = -10 \text{ V}$, $R_g = 1 \Omega$	-	25	35	
Rise time ^c	t_r		-	20	30	ns
Turn-off delay time ^c	$t_{d(\text{off})}$		-	90	140	
Fall time ^c	t_f		-	20	30	
Drain-Source Body Diode Characteristics ($T_C = 25^\circ\text{C}$ ^b)						
Continuous current	I_S	$I_F = -10 \text{ A}$, $V_{GS} = 0 \text{ V}$	-	-	-150	
Pulsed current	I_{SM}		-	-	-250	A
Forward voltage ^a	V_{SD}	$I_F = -20 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}$	-	-0.8	-1.5	V
Reverse recovery time	t_{rr}		-	90	135	ns
Peak reverse recovery charge	$I_{RM(\text{REC})}$		-	-2.8	-4.2	A
Reverse recovery charge	Q_{rr}		-	145	218	nC

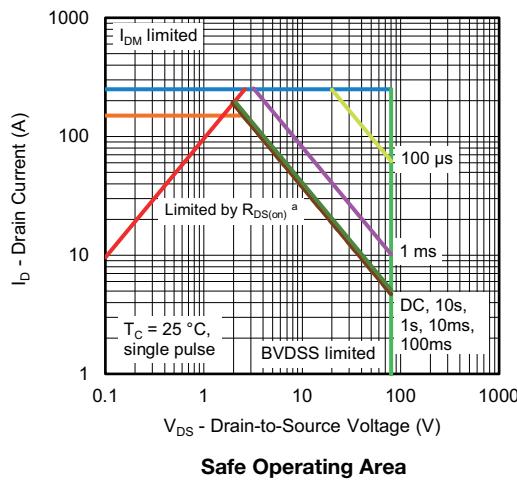
Notes

- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

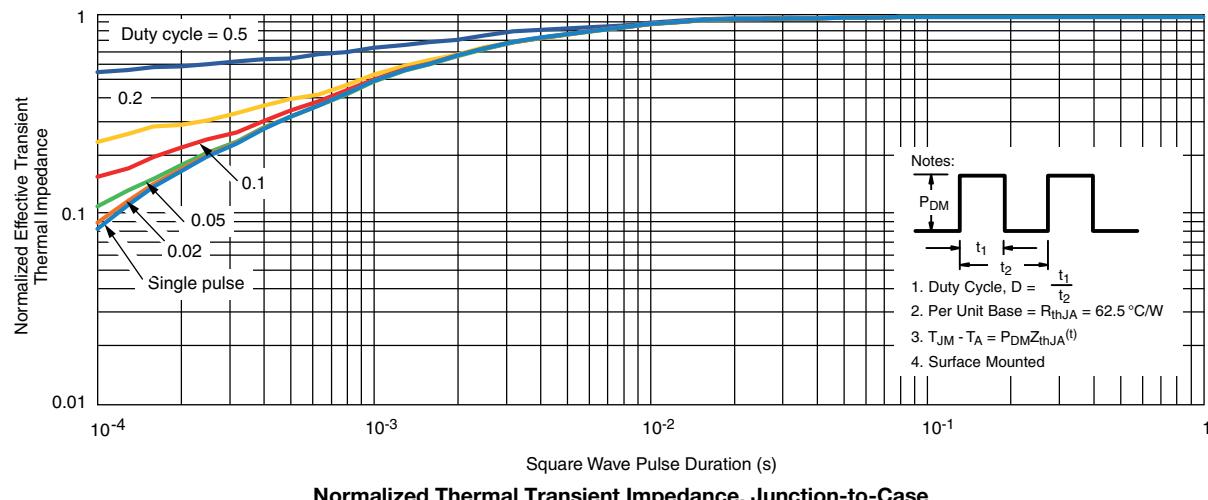
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)


TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

On-Resistance vs. Junction Temperature

Threshold Voltage

On-Resistance vs. Gate-to-Source Voltage

Drain Source Breakdown vs. Junction Temperature

Source Drain Diode Forward Voltage

Avalanche Current vs. Time

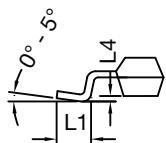
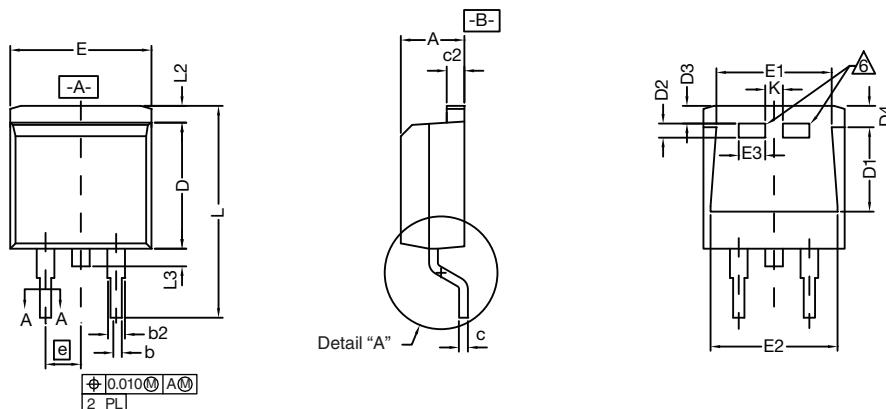
THERMAL RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

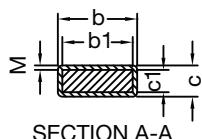


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TO-263 (D²PAK): 3-LEAD



DETAIL A (ROTATED 90°)



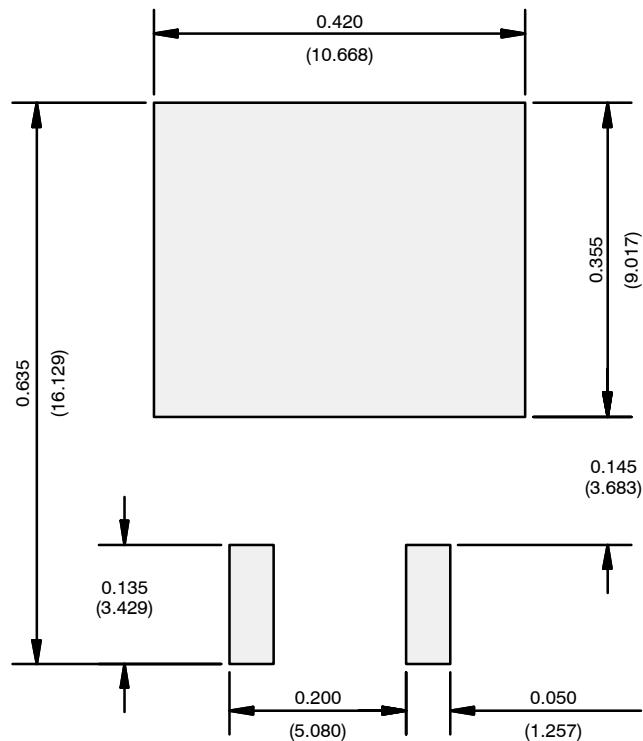
SECTION A-A

Notes

1. Plane B includes maximum features of heat sink tab and plastic.
2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
3. Pin-to-pin coplanarity max. 4 mils.
4. *: Thin lead is for SUB, SYB.
Thick lead is for SUM, SYM, SQM.
5. Use inches as the primary measurement.

 This feature is for thick lead.

DIM.	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	0.160	0.190	4.064	4.826	
b	0.020	0.039	0.508	0.990	
b1	0.020	0.035	0.508	0.889	
b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2	0.045	0.055	1.143	1.397	
D	0.340	0.380	8.636	9.652	
D1	0.220	0.240	5.588	6.096	
D2	0.038	0.042	0.965	1.067	
D3	0.045	0.055	1.143	1.397	
D4	0.044	0.052	1.118	1.321	
E	0.380	0.410	9.652	10.414	
E1	0.245	-	6.223	-	
E2	0.355	0.375	9.017	9.525	
E3	0.072	0.078	1.829	1.981	
e	0.100 BSC		2.54 BSC		
K	0.045	0.055	1.143	1.397	
L	0.575	0.625	14.605	15.875	
L1	0.090	0.110	2.286	2.794	
L2	0.040	0.055	1.016	1.397	
L3	0.050	0.070	1.270	1.778	
L4	0.010 BSC		0.254 BSC		
M	-	0.002	-	0.050	
ECN: T13-0707-Rev. K, 30-Sep-13					
DWG: 5843					

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead

Recommended Minimum Pads
Dimensions in Inches/(mm)

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