

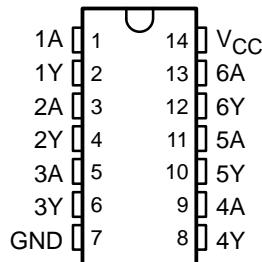
- Operating Range 2-V to 5.5-V  $V_{CC}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

### description/ordering information

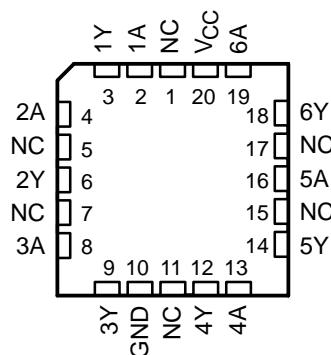
The 'AHC05 devices contain six independent inverters. These devices perform the Boolean function  $Y = \bar{A}$ .

The open-drain outputs require pullup resistors to perform correctly. They can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

SN54AHC05 . . . J OR W PACKAGE  
SN74AHC05 . . . D, DB, DGV, N, OR PW PACKAGE  
(TOP VIEW)



SN54AHC05 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74AHC05N	SN74AHC05N
	SOIC – D	Tube	SN74AHC05D	AHC05
		Tape and reel	SN74AHC05DR	
	SSOP – DB	Tape and reel	SN74AHC05DBR	HA05
	TSSOP – PW	Tube	SN74AHC05PW	HA05
		Tape and reel	SN74AHC05PWR	
–55°C to 125°C	TVSOP – DGV	Tape and reel	SN74AHC05DGVR	HA05
	CDIP – J	Tube	SNJ54AHC05J	SNJ54AHC05J
	CFP – W	Tube	SNJ54AHC05W	SNJ54AHC05W
	LCCC – FK	Tube	SNJ54AHC05FK	SNJ54AHC05FK

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

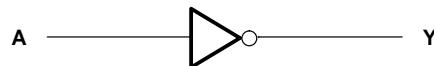
**SN54AHC05, SN74AHC05  
HEX INVERTERS  
WITH OPEN-DRAIN OUTPUTS**

SCLS357H – MAY 1997 – REVISED JULY 2003

**FUNCTION TABLE  
(each inverter)**

INPUT A	OUTPUT Y
H	L
L	H

**logic diagram, each inverter (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) .....	–0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	±25 mA
Continuous current through $V_{CC}$ or GND .....	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package .....	86°C/W
DB package .....	96°C/W
DGV package .....	127°C/W
N package .....	80°C/W
PW package .....	113°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JEDEC 51-7.

**recommended operating conditions (see Note 3)**

			SN54AHC05	SN74AHC05	UNIT		
			MIN	MAX			
V <sub>CC</sub>	Supply voltage		2	5.5	2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5	1.5	V		
		V <sub>CC</sub> = 3 V	2.1	2.1			
		V <sub>CC</sub> = 5.5 V	3.85	3.85			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0.5	0.5	V		
		V <sub>CC</sub> = 3 V	0.9	0.9			
		V <sub>CC</sub> = 5.5 V	1.65	1.65			
V <sub>I</sub>	Input voltage		0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V	50	50	μA		
		V <sub>CC</sub> = 3.3 V ± 0.3 V	4	4	mA		
		V <sub>CC</sub> = 5 V ± 0.5 V	8	8			
Δt/ΔV	Input transition rise or fall rate	V <sub>CC</sub> = 3.3 V ± 0.3 V	100	100	ns/V		
		V <sub>CC</sub> = 5 V ± 0.5 V	20	20			
T <sub>A</sub>	Operating free-air temperature		-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AHC05	SN74AHC05	UNIT
			MIN	TYP	MAX	MIN	MAX	
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V		0.1		0.1	0.1	V
		3 V		0.1		0.1	0.1	
		4.5 V		0.1		0.1	0.1	
	I <sub>OL</sub> = 4 mA	3 V		0.36		0.5	0.44	
	I <sub>OL</sub> = 8 mA	4.5 V		0.36		0.5	0.44	
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V		±0.1		±1*	±1	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		2		20	20	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2.5	10		10	pF

\* On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

**switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN54AHC05	SN74AHC05	UNIT	
				MIN	TYP	MAX	MIN	MAX		
t <sub>PLZ</sub>	A	Y	C <sub>L</sub> = 15 pF	2.9**	7.1**		1**	8.5**	1	8.5
				4**	7.1**		1**	8.5**	1	8.5
t <sub>PZL</sub>	A	Y	C <sub>L</sub> = 50 pF	4.7	10.6		1	12	1	12
				5.8	10.6		1	12	1	12

\*\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**SN54AHC05, SN74AHC05  
HEX INVERTERS  
WITH OPEN-DRAIN OUTPUTS**

SCLS357H – MAY 1997 – REVISED JULY 2003

**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC05	SN74AHC05	UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{PLZ}$	A	Y	$C_L = 15 \text{ pF}$	2.2*	5.5*	1*	6.5*	1	6.5
$t_{PZL}$				2.9*	5.5*	1*	6.5*	1	6.5
$t_{PLZ}$	A	Y	$C_L = 50 \text{ pF}$	3.4	7.5	1	8.5	1	8.5
$t_{PZL}$				4.2	7.5	1	8.5	1	8.5

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**operating characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$**

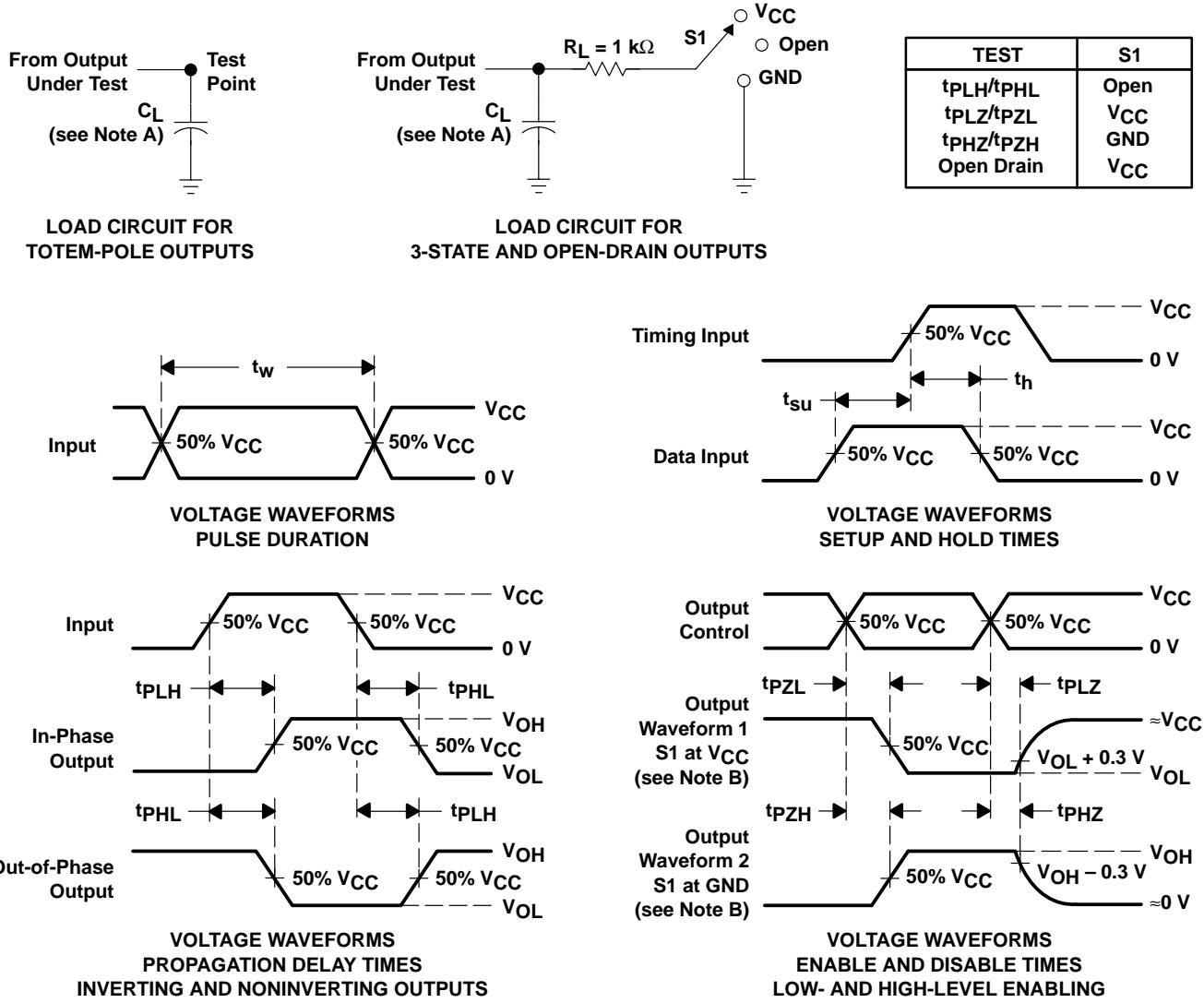
PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load, $f = 1 \text{ MHz}$	3	pF

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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PARAMETER MEASUREMENT INFORMATION



NOTES:

- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 3 \text{ ns}$ ,  $t_f \leq 3 \text{ ns}$ .
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC05D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC05	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC05DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA05	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC05DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC05	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC05N	ACTIVE	PDIP	N	14	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHC05N	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC05PW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA05	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC05PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA05	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



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## PACKAGE OPTION ADDENDUM

10-Dec-2020

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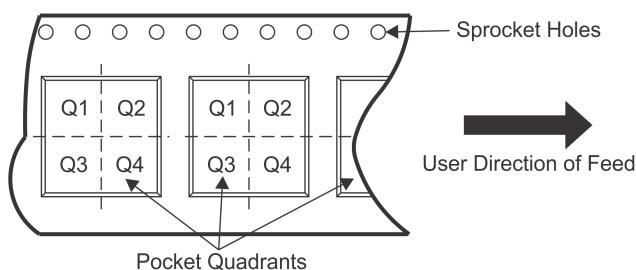
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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


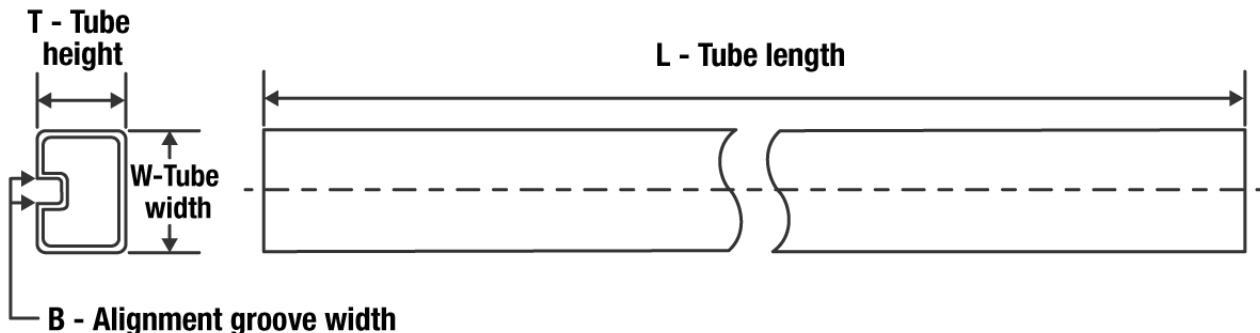
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC05DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC05DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC05PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC05DBR	SSOP	DB	14	2000	853.0	449.0	35.0
SN74AHC05DR	SOIC	D	14	2500	853.0	449.0	35.0
SN74AHC05PWR	TSSOP	PW	14	2000	853.0	449.0	35.0

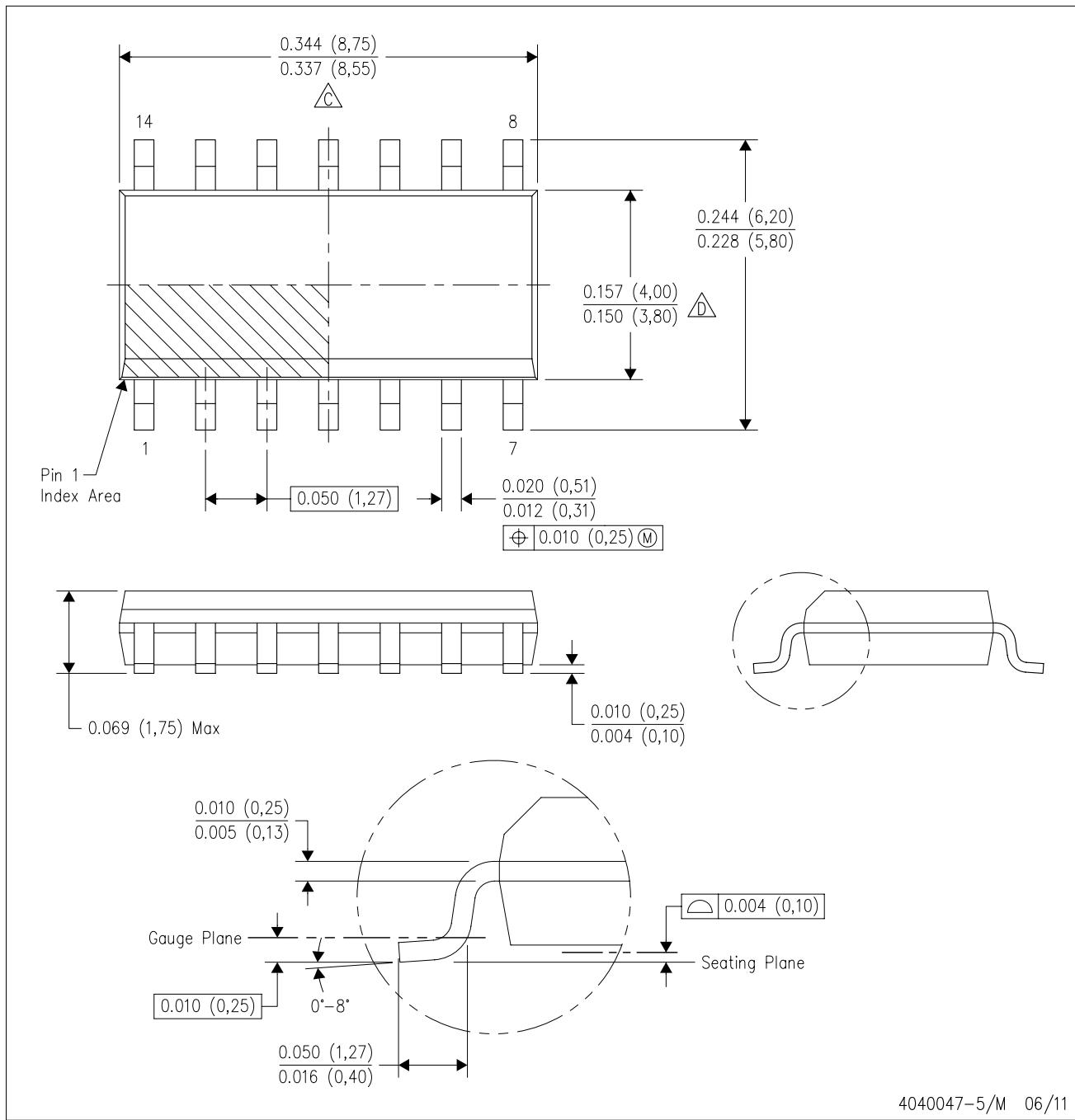
**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74AHC05D	D	SOIC	14	50	506.6	8	3940	4.32
SN74AHC05N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC05PW	PW	TSSOP	14	90	530	10.2	3600	3.5

D (R-PDSO-G14)

## PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

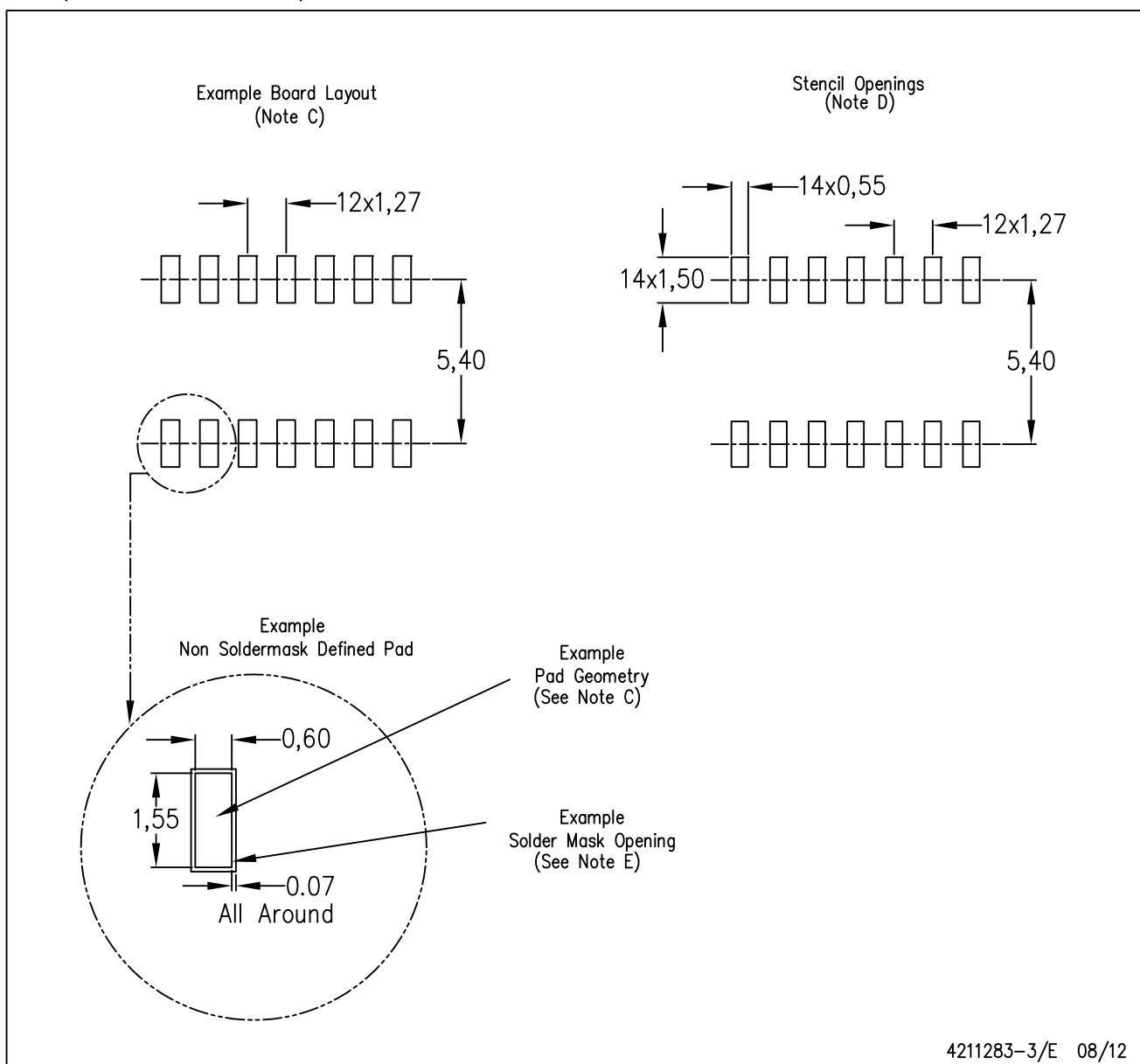
 Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

 Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.  
E. Reference JEDEC MS-012 variation AB.

E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



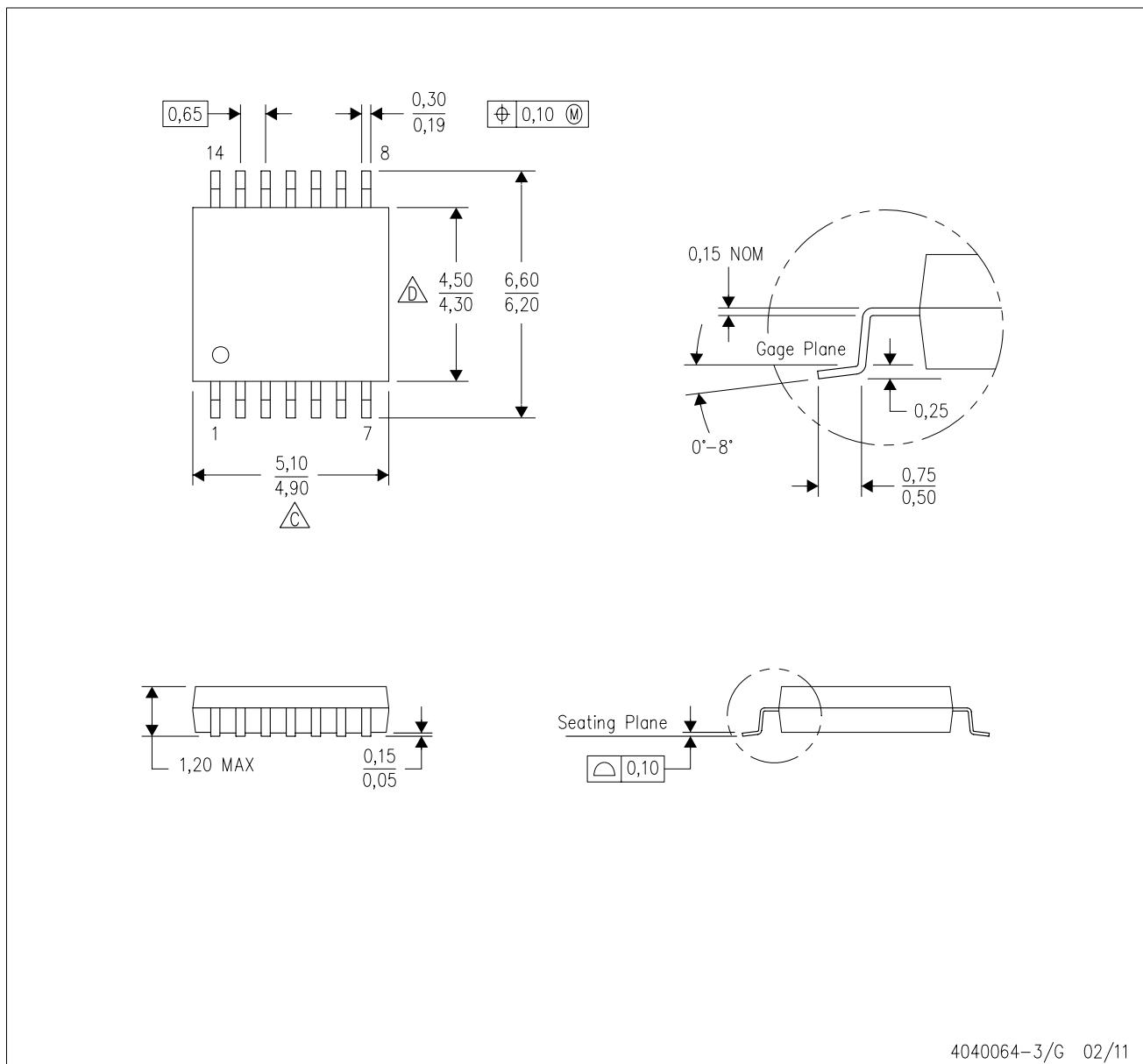
4211283-3/E 08/12

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

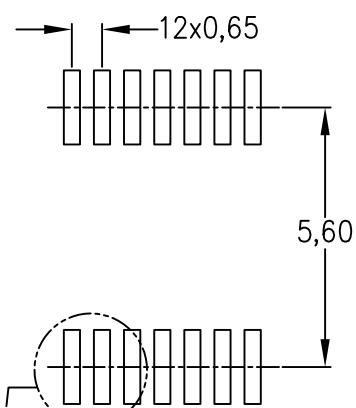
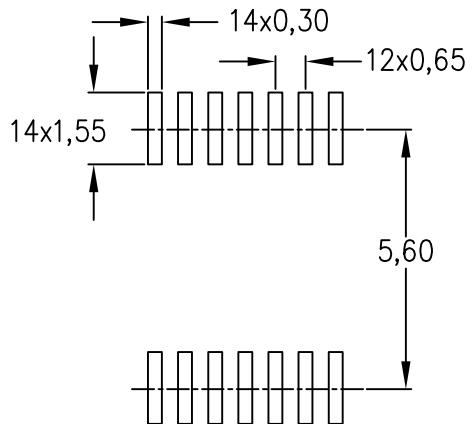
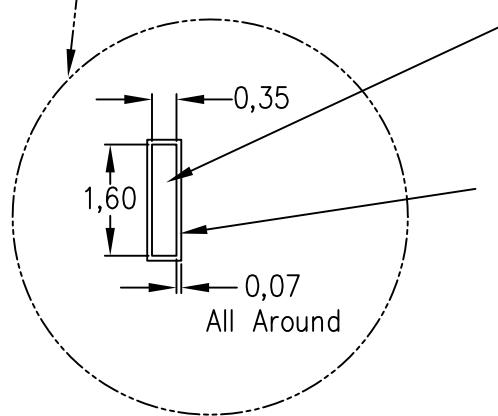
 D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

4040064-3/G 02/11

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)Example  
Non Soldermask Defined PadExample  
Pad Geometry  
(See Note C)Example  
Solder Mask Opening  
(See Note E)

4211284-2/G 08/15

## NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

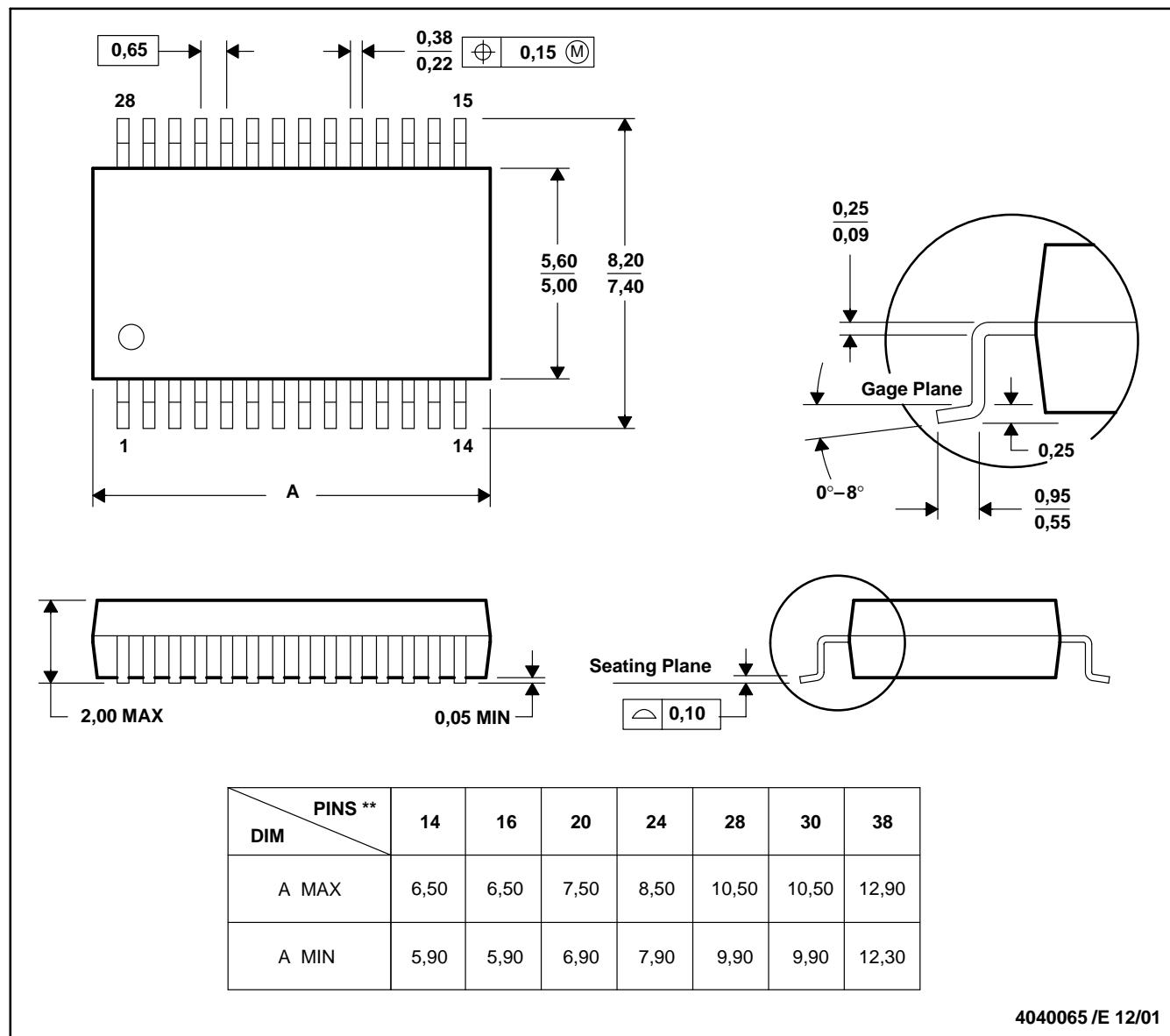
## PLASTIC DUAL-IN-LINE PACKAGE



## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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