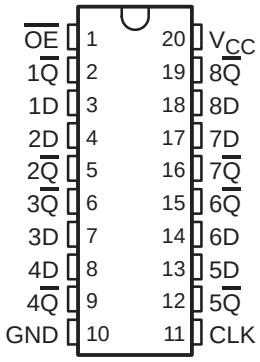
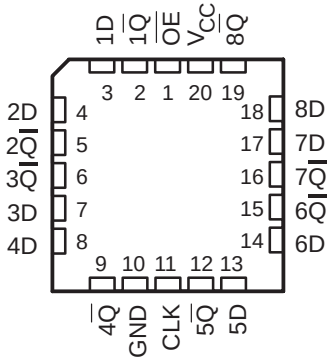
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical $V_{OLP}$ (Output Ground Bounce) < 1 V at $V_{CC}$ = 5 V, $T_A$ = 25°C**
- **High-Drive Outputs (–32-mA $I_{OH}$, 64-mA $I_{OL}$)**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Plastic (N) and Ceramic (J) DIPs, and Ceramic Flat (W) Package**

**SN54ABT534 . . . J OR W PACKAGE**
**SN74ABT534A . . . DB, DW, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54ABT534 . . . FK PACKAGE**
**(TOP VIEW)**




## description

These 8-bit flip-flops with 3-state outputs are designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK), the $\overline{Q}$ outputs are set to the complement of the logic levels set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the flip-flop. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

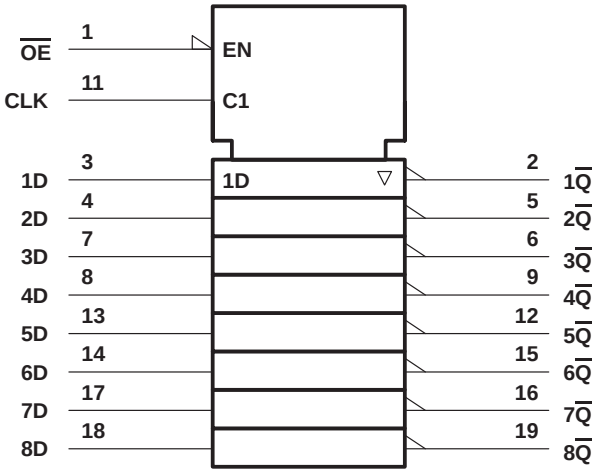
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT534 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT534A is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each flip-flop)**

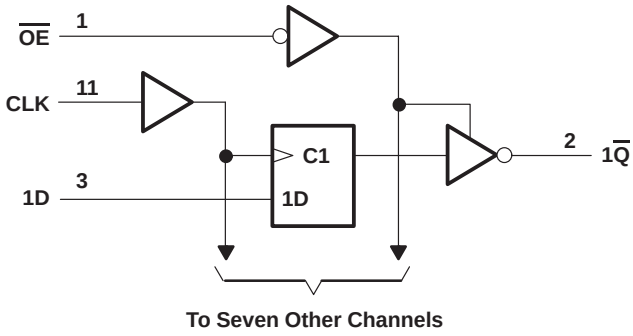
| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | CLK | D | $\overline{Q}$ |
| L | ↑ | H | L |
| L | ↑ | L | H |
| L | H or L | X | $\overline{Q}_0$ |
| H | X | X | Z |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ . . . . . –0.5 V to 5.5 V
Current into any output in the low state, $I_O$: SN54ABT534 . . . . . 96 mA
SN74ABT534A . . . . . 128 mA
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –18 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) . . . . . –50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package . . . . . 115°C/W
DW package . . . . . 97°C/W
N package . . . . . 67°C/W
PW package . . . . . 128°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

| | | | SN54ABT534 | | SN74ABT534A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | | –24 | | –32 | mA |
| $I_{OL}$ | Low-level output current | | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 5 | | 5 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | | $T_A$ = 25°C | | | SN54ABT534 | | SN74ABT534A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | | –1.2 | | –1.2 | | –1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –3 mA | | 2.5 | | | 2.5 | | 2.5 | | V |
| | $V_{CC}$ = 5 V, | $I_{OH}$ = –3 mA | | 3 | | | 3 | | 3 | | |
| | $V_{CC}$ = 4.5 V | $I_{OH}$ = –24 mA | | 2 | | | 2 | | | | |
| | | $I_{OH}$ = –32 mA | | 2* | | | | | 2 | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | | | 0.55 | | 0.55 | | | V |
| | | $I_{OL}$ = 64 mA | | | | 0.55* | | | | 0.55 | |
| $V_{hys}$ | | | | | 100 | | | | | | mV |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or GND | | | | ±1 | | ±1 | | ±1 | µA |
| $I_{OZH}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | | 10‡ | | 10‡ | | 10‡ | µA |
| $I_{OZL}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | | –10‡ | | –10‡ | | –10‡ | µA |
| $I_{off}$ | $V_{CC}$ = 0, | $V_I$ or $V_O \le$ 4.5 V | | | | ±100 | | | | ±100 | µA |
| $I_{CEX}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 5.5 V | Outputs high | | | 50 | | 50 | | 50 | µA |
| $I_O$§ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.5 V | | –50 | –100 | –180‡ | –50 | –180‡ | –50 | –180‡ | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | | Outputs high | | 1 | 250 | | 250 | | 250 | µA |
| | | | Outputs low | | 24 | 30 | | 30 | | 30 | mA |
| | | | Outputs disabled | | 0.5 | 250 | | 250 | | 250 | µA |
| $\Delta I_{CC}$¶ | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | | | 1.5 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I$ = 2.5 V or 0.5 V | | | | 3.5 | | | | | | pF |
| $C_o$ | $V_O$ = 2.5 V or 0.5 V | | | | 6.5 | | | | | | pF |

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC}$ = 5 V.
‡ This data sheet limit may vary among suppliers.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)**

| | | | SN54ABT534 | | | UNIT |
|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | MIN MAX | |
| | | | MIN | MAX | | |
| $f_{clock}$ | Clock frequency | | | 125 | 125 | MHz |
| $t_w$ | Pulse duration | CLK high or low | 3.5 | | 3.5 | ns |
| $t_{su}$ | Setup time, data before CLK↑ | High or low | 1.6 | | 1.6 | ns |
| $t_h$ | Hold time, data after CLK↑ | High or low | 1.6 | | 1.6 | ns |

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)**

| | | | SN74ABT534A | | | UNIT |
|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | MIN MAX | |
| | | | MIN | MAX | | |
| $f_{clock}$ | Clock frequency | | | 125 | 125 | MHz |
| $t_w$ | Pulse duration | CLK high or low | 3.5 | | 3.5 | ns |
| $t_{su}$ | Setup time, data before CLK↑ | High or low | 1.6 | | 1.6 | ns |
| $t_h$ | Hold time, data after CLK↑ | High or low | 2† | | 2† | ns |

† This data sheet limit may vary among suppliers.

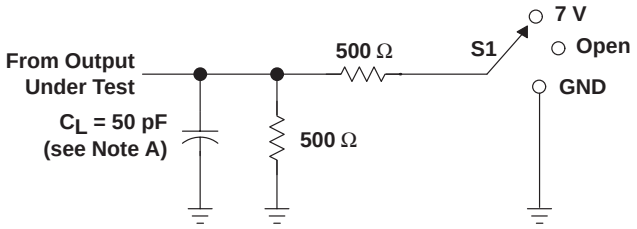
**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ABT534 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | MIN | MAX | |
| | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | 125 | 175 | | 125 | | MHz |
| $t_{PLH}$ | CLK | $\overline{Q}$ | 2.6 | 4.5 | 6.1 | 2.6 | 7 | ns |
| $t_{PHL}$ | | | 3.4 | 5.5 | 6.7 | 3.4 | 7.9 | |
| $t_{PZH}$ | $\overline{OE}$ | $\overline{Q}$ | 1 | 3.4 | 5.2 | 1 | 5.8 | ns |
| $t_{PZL}$ | | | 2.6 | 4 | 5.8 | 2.6 | 7 | |
| $t_{PHZ}$ | $\overline{OE}$ | $\overline{Q}$ | 2.4 | 4.7 | 6.6 | 2.4 | 7.6 | ns |
| $t_{PLZ}$ | | | 2.3 | 3.8 | 5.8 | 2.3 | 6.8 | |

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)**

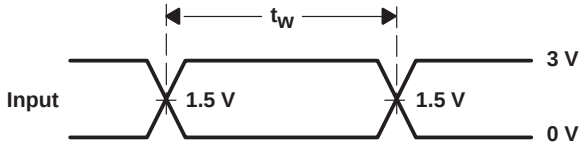
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74ABT534A | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | MIN | MAX | |
| | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | 125 | 175 | | 125 | | MHz |
| $t_{PLH}$ | CLK | $\overline{Q}$ | 2.6 | 4.5 | 5.9 | 2.6 | 6.7 | ns |
| $t_{PHL}$ | | | 3.4 | 5.5 | 6.7 | 3.4 | 7.6 | |
| $t_{PZH}$ | $\overline{OE}$ | $\overline{Q}$ | 1 | 3.4 | 4.2 | 1 | 5 | ns |
| $t_{PZL}$ | | | 2.6 | 4 | 5.8 | 2.6 | 6.8 | |
| $t_{PHZ}$ | $\overline{OE}$ | $\overline{Q}$ | 2.4 | 4.7 | 6.6 | 2.4 | 7.3 | ns |
| $t_{PLZ}$ | | | 2.3 | 3.8 | 5.8 | 2.3 | 6.5 | |

## PARAMETER MEASUREMENT INFORMATION

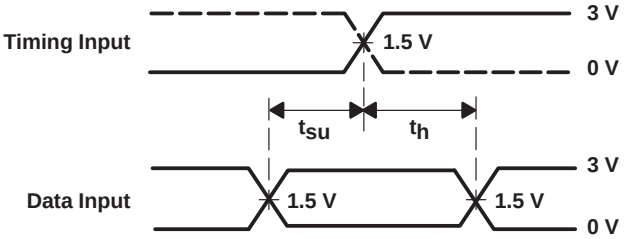



| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |

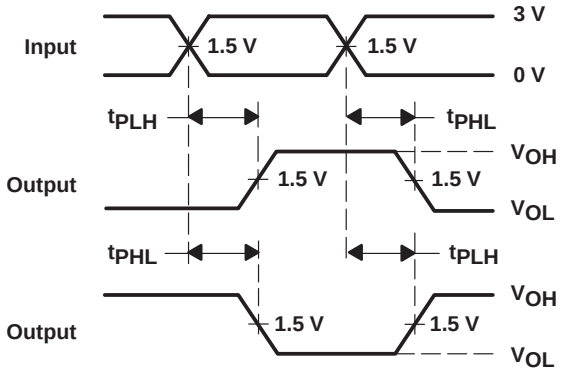
LOAD CIRCUIT



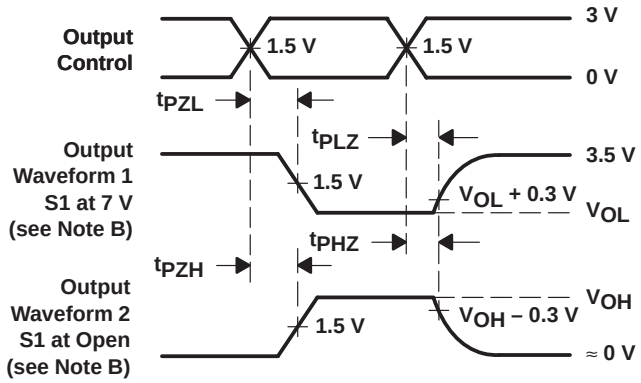

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-9314701QRA | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9314701QRA SNJ54ABT534J | Samples |
| 5962-9314701QSA | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9314701QSA SNJ54ABT534W | Samples |
| SN74ABT534ADBR | ACTIVE | SSOP | DB | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AB534A | Samples |
| SN74ABT534ADW | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ABT534A | Samples |
| SN74ABT534ADWR | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ABT534A | Samples |
| SN74ABT534AN | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN74ABT534AN | Samples |
| SN74ABT534ANE4 | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN74ABT534AN | Samples |
| SNJ54ABT534J | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9314701QRA SNJ54ABT534J | Samples |
| SNJ54ABT534W | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9314701QSA SNJ54ABT534W | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

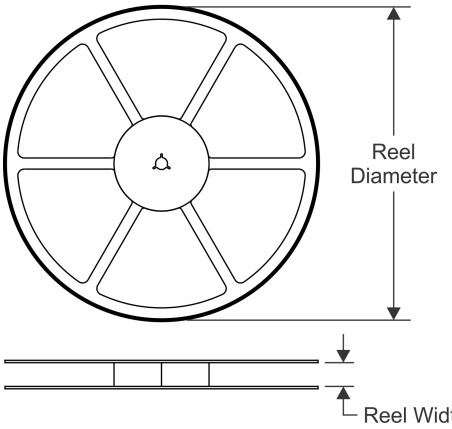
**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

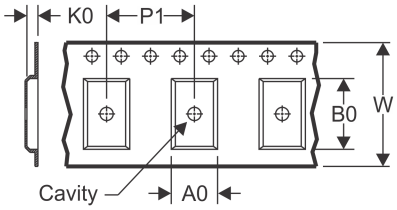
**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

REEL DIMENSIONS

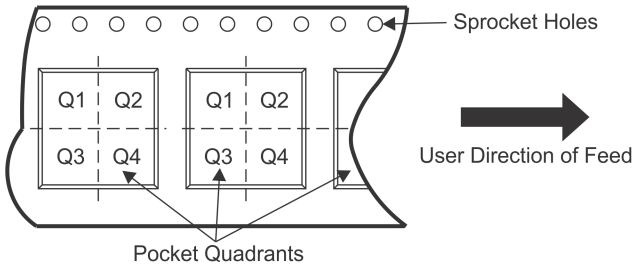



TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

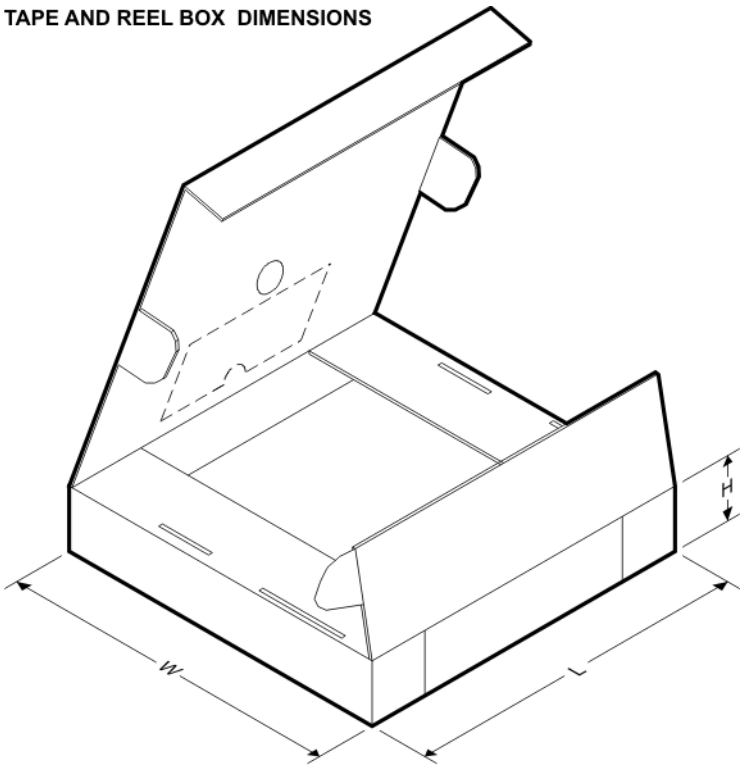
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74ABT534ADBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74ABT534ADWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |

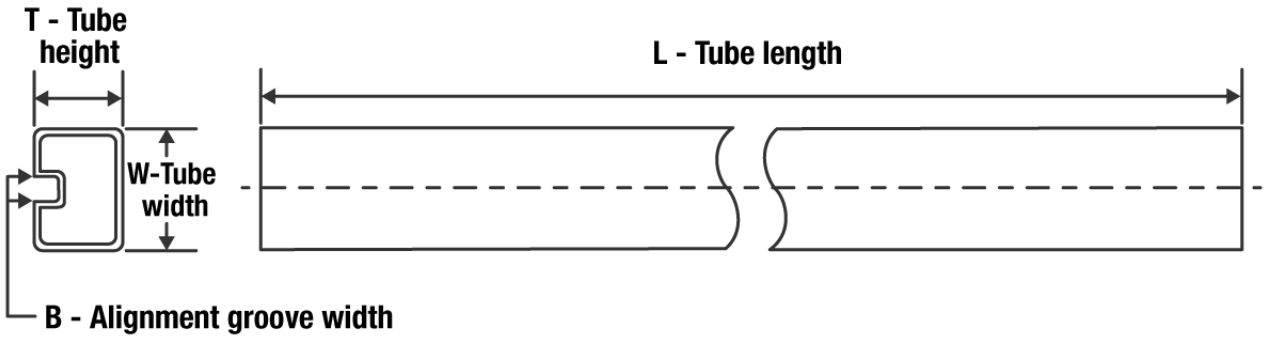
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74ABT534ADBR | SSOP | DB | 20 | 2000 | 853.0 | 449.0 | 35.0 |
| SN74ABT534ADWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |

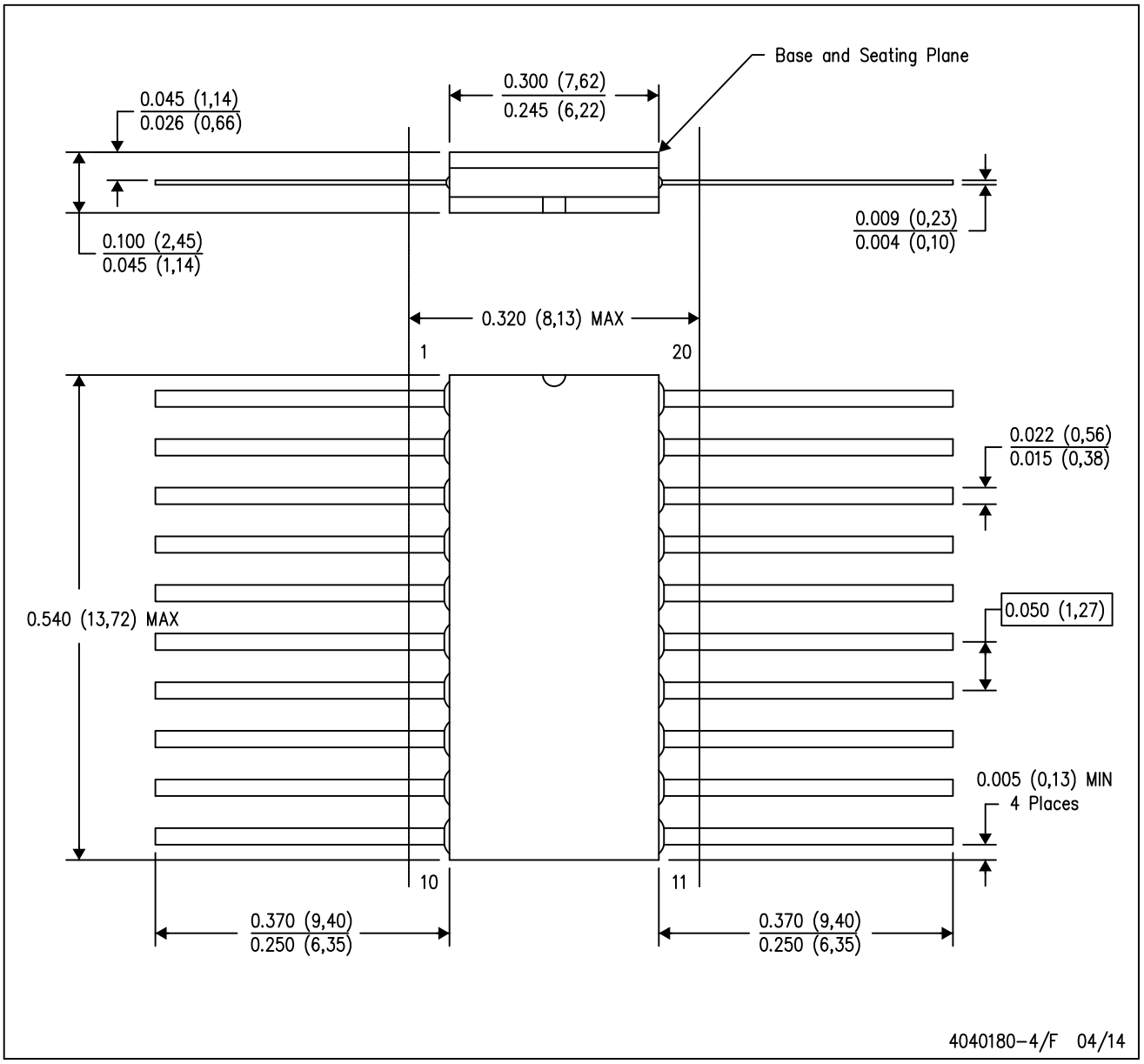
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN74ABT534ADW | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN74ABT534AN | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74ABT534ANE4 | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |

W (R–GDFP–F20) CERAMIC DUAL FLATPACK



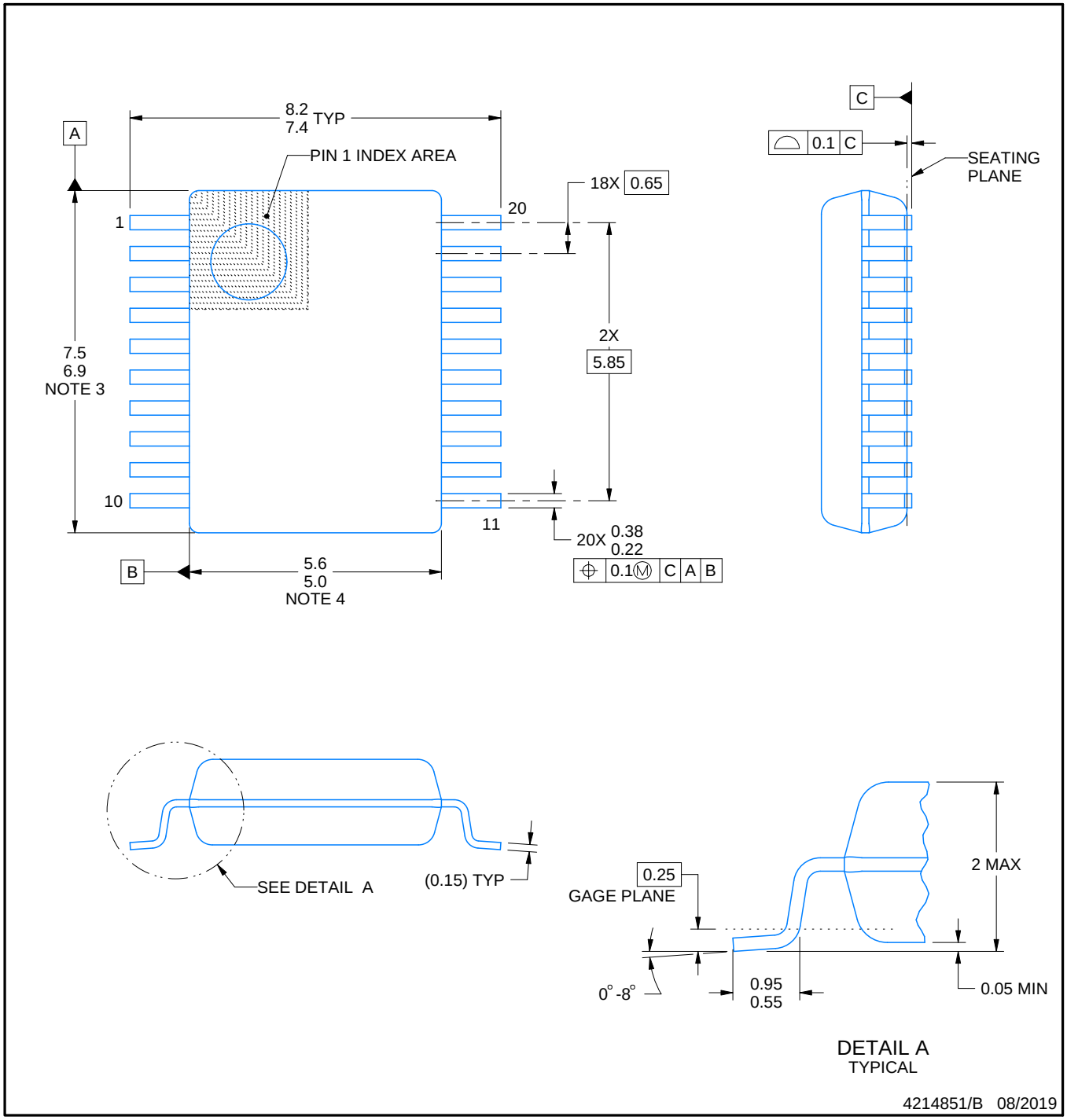

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

# PACKAGE OUTLINE

## DB0020A

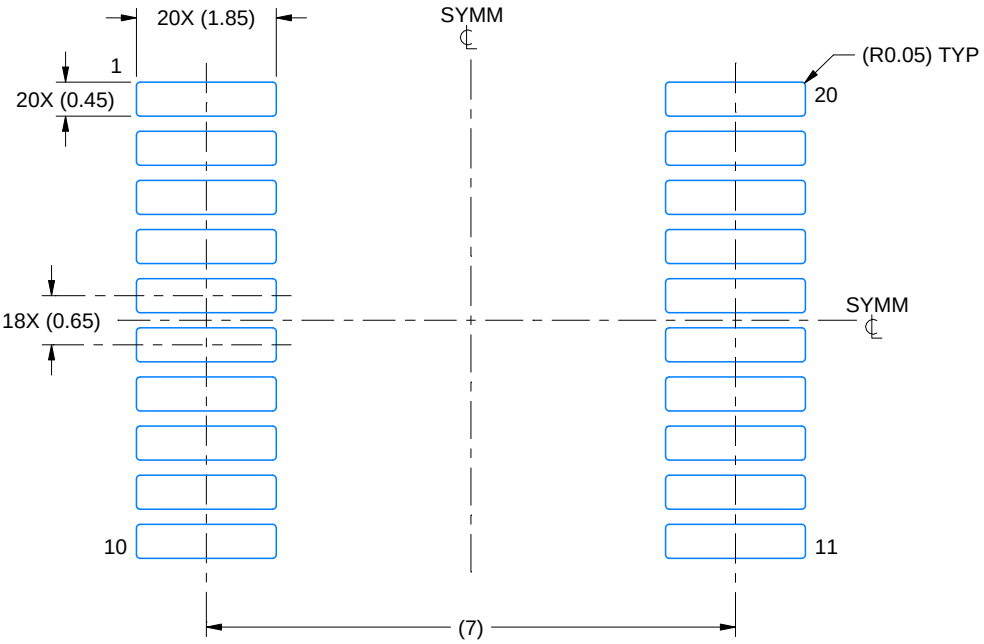
## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

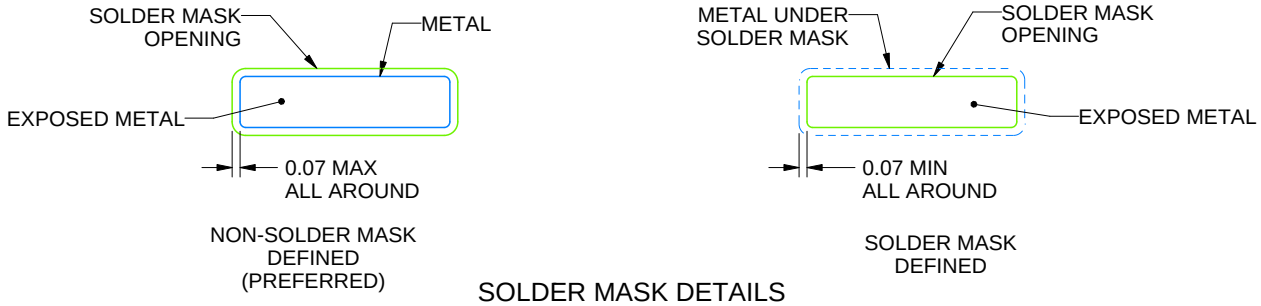



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X




SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

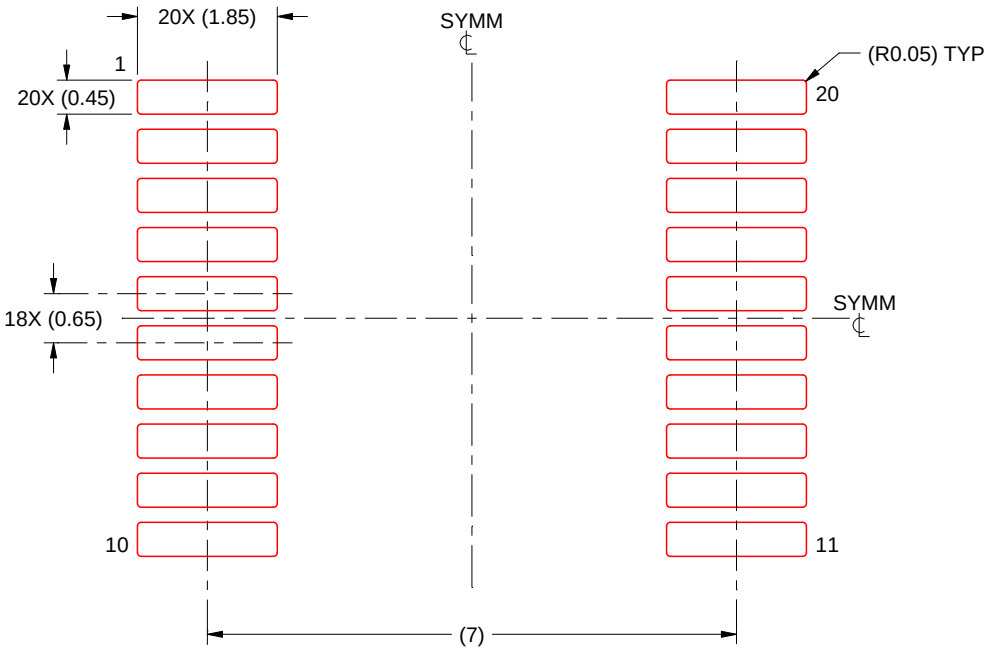
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DB0020A

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

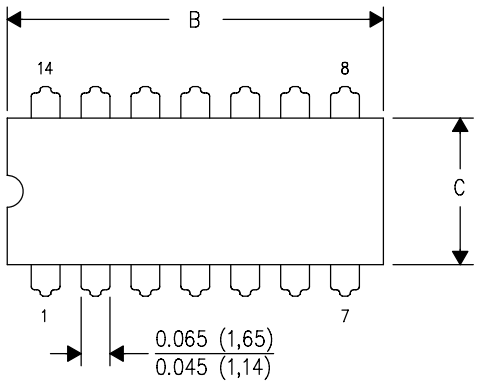
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

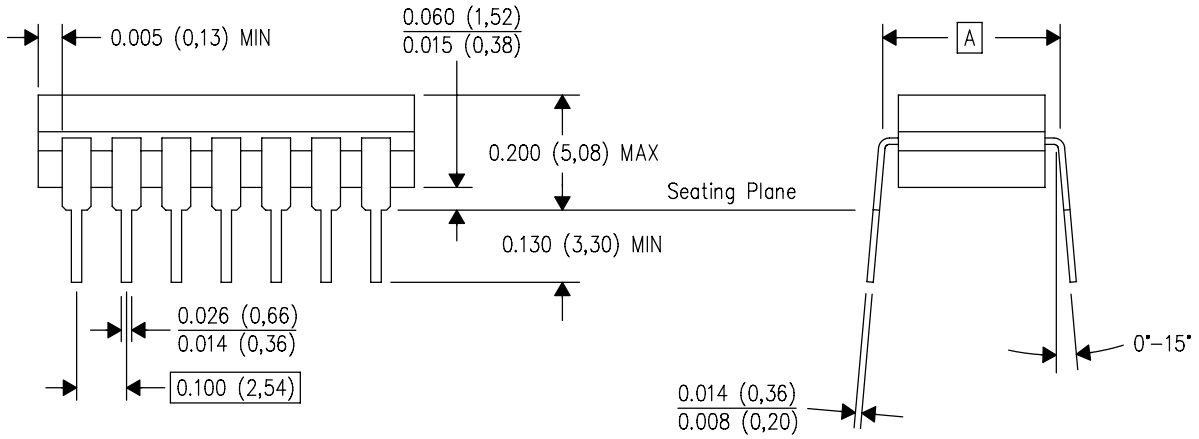
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



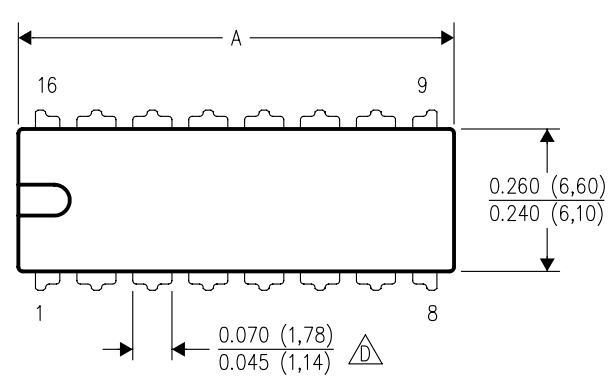

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

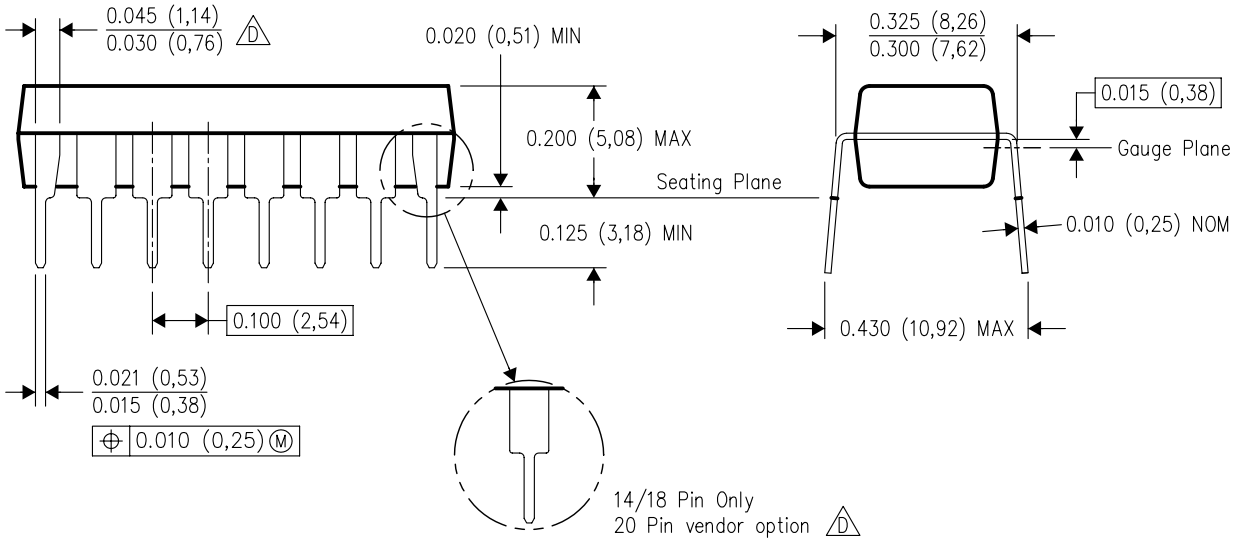
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

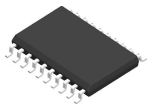



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

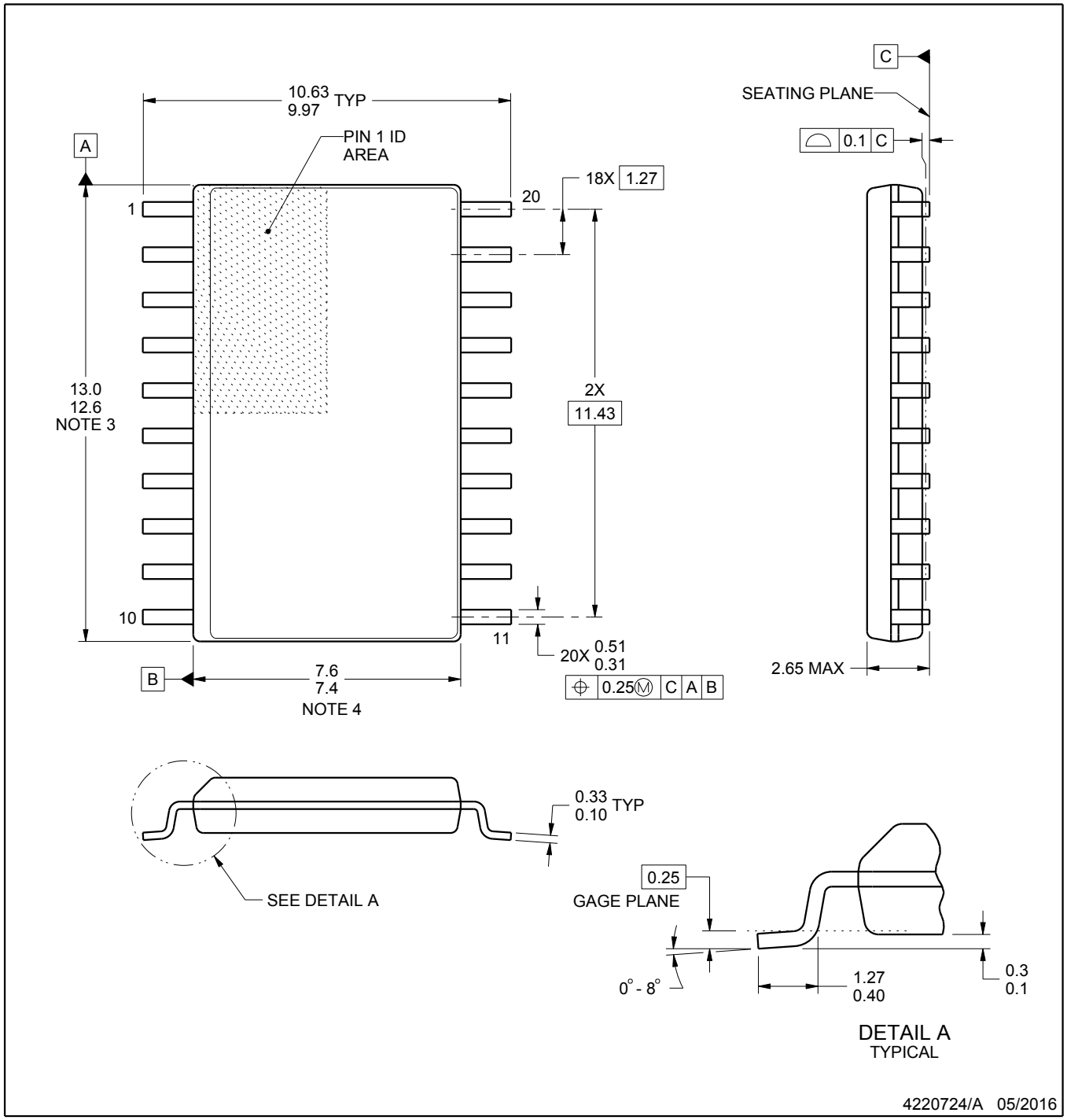


# PACKAGE OUTLINE

## DW0020A

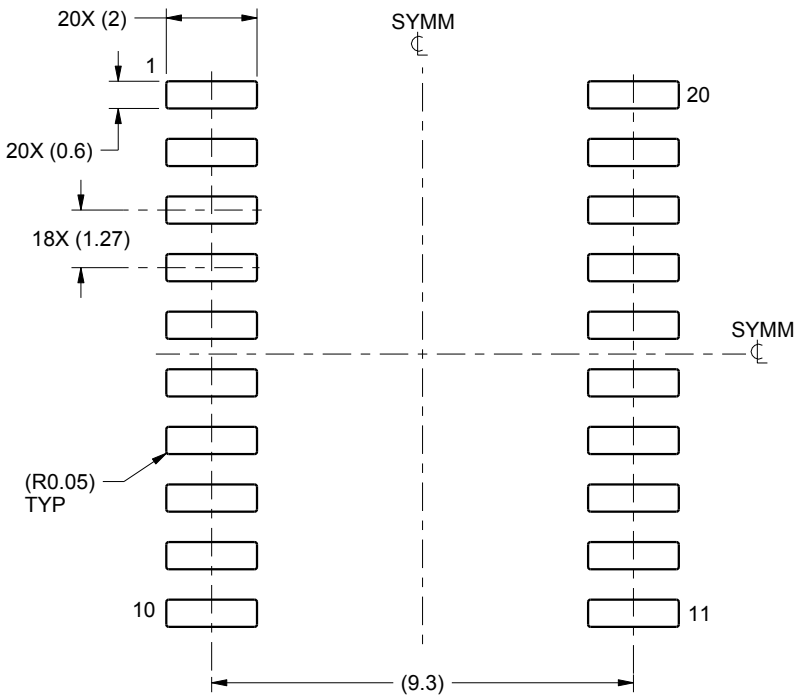
## SOIC - 2.65 mm max height

SOIC

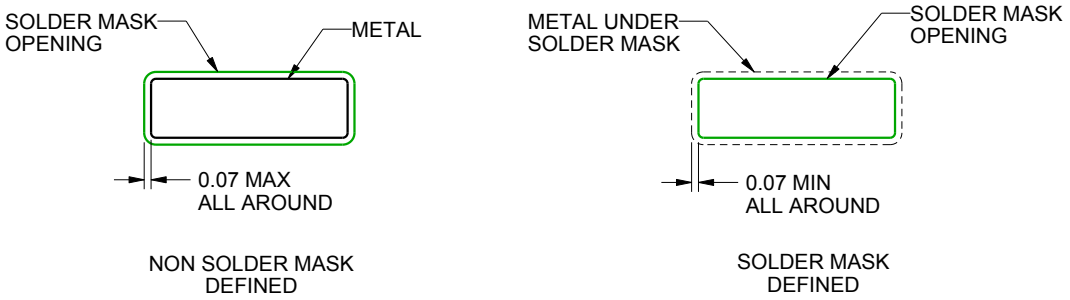



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:6X

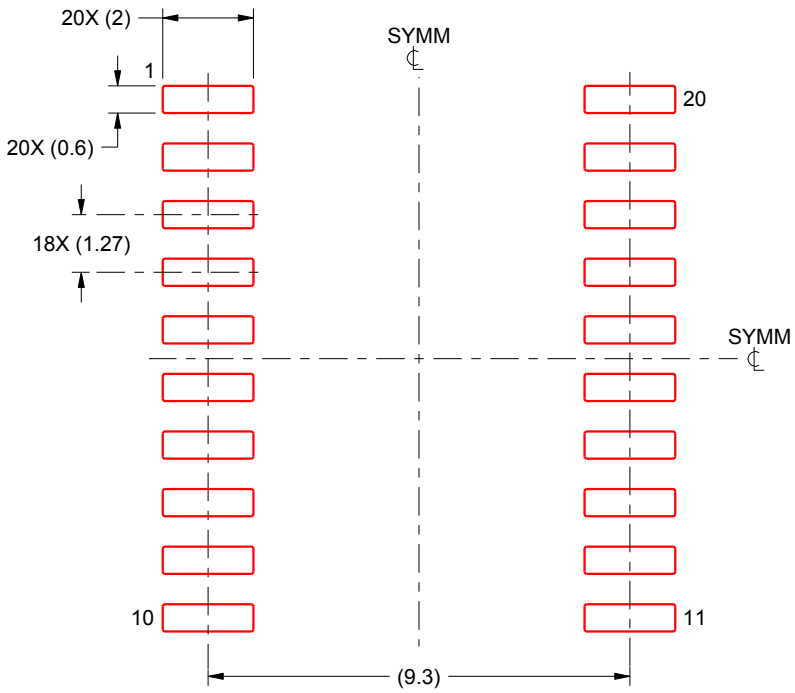



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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