

SN54ALS541, SN74ALS540, SN74ALS541 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SDAS025D – APRIL 1982 – REVISED MARCH 2002

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- pnp Inputs Reduce dc Loading
- Data Flowthrough Pinout (All Inputs on Opposite Side From Outputs)

description

These octal buffers and line drivers are designed to have the performance of the popular SN54ALS240A/SN74ALS240A series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly facilitates printed circuit board layout.

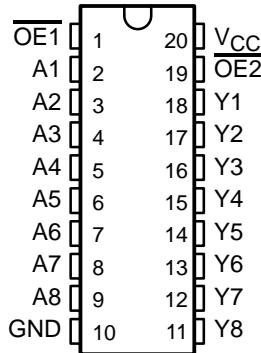
The 3-state control gate is a 2-input NOR gate such that, if either output-enable (\overline{OE}_1 or \overline{OE}_2) input is high, all eight outputs are in the high-impedance state.

The SN74ALS540 provides inverted data. The 'ALS541 provide true data at the outputs.

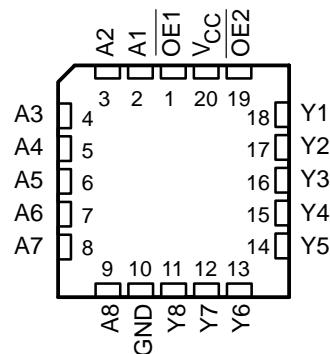
The -1 versions of SN74ALS540 and SN74ALS541 are identical to the standard versions, except that the recommended maximum I_{OL} is increased to 48 mA. There is no -1 version of the SN54ALS541.

SN54ALS541 . . . J PACKAGE
SN74ALS540 . . . DW, N, OR NS PACKAGE
SN74ALS541 . . . DB, DW, N, OR NS PACKAGE

(TOP VIEW)



SN54ALS541 . . . FK PACKAGE
(TOP VIEW)




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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**SN54ALS541, SN74ALS540, SN74ALS541
OCTAL BUFFERS AND LINE DRIVERS
WITH 3-STATE OUTPUTS**

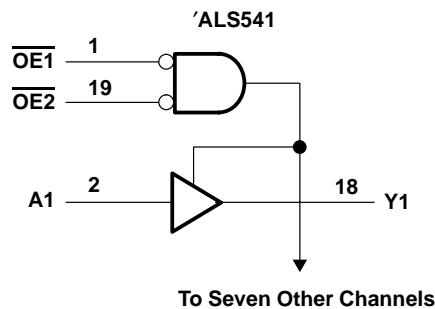
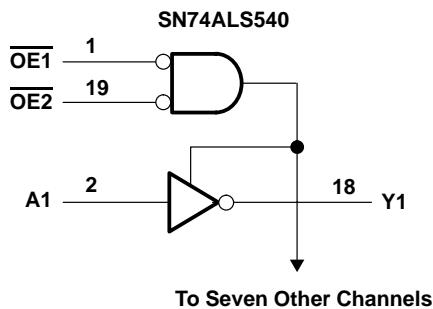
SDAS025D – APRIL 1982 – REVISED MARCH 2002

ORDERING INFORMATION

TA	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74ALS540N	SN74ALS540N
			SN74ALS540-1N	SN74ALS540-1N
			SN74ALS541N	SN74ALS541N
			SN74ALS541-1N	SN74ALS541-1N
	SOIC – DW	Tube	SN74ALS540DW	ALS540
		Tape and reel	SN74ALS540DWR	
		Tube	SN74ALS540-1DW	ALS540-1
		Tube	SN74ALS541DW	ALS541
		Tape and reel	SN74ALS541DWR	
		Tube	SN74ALS541-1DW	ALS541-1
	SOP – NS	Tape and reel	SN74ALS540NSR	ALS540
		Tape and reel	SN74ALS540-1NSR	ALS540-1
			SN74ALS541NSR	ALS541
			SN74ALS541-1NSR	ALS541-1
-55°C to 125°C	SSOP – DB	Tape and reel	SN74ALS541DBR	G541
			SN74ALS541-1DBR	G541-1
	CDIP – J	Tube	SNJ54ALS541J	SNJ54ALS541J
	LCCC – FK	Tube	SNJ54ALS541FK	SNJ54ALS541FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

logic diagrams (positive logic)



SN54ALS541, SN74ALS540, SN74ALS541 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Package thermal impedance, θ_{JA} (see Note 1):	
DB package	70°C/W
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
Storage temperature range, T_{STG}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		SN54ALS541			SN74ALS540 SN74ALS541			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2			2		V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current			-12			-15	mA
I _{OL}	Low-level output current			12			24	mA
							48†	
T _A	Operating free-air temperature	-55		125	0		70	°C

[†] Applies only to the -1 version and only if V_{CC} is between 4.75 V and 5.25 V

**SN54ALS541, SN74ALS540, SN74ALS541
OCTAL BUFFERS AND LINE DRIVERS
WITH 3-STATE OUTPUTS**

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS541			SN74ALS540 SN74ALS541			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2			-1.2	V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA	V _{CC} - 2			V _{CC} - 2			V
	V _{CC} = 4.5 V	I _{OH} = -3 mA	2.4	3.2	2.4	3.2		
		I _{OH} = -12 mA	2					
		I _{OH} = -15 mA				2		
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 12 mA	0.25	0.4	0.25	0.4		V
		I _{OL} = 24 mA			0.35	0.5		
		I _{OL} = 48 mA [†]			0.35	0.5		
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V			20			20	µA
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.4 V			-20			-20	µA
I _I	V _{CC} = 5.5 V, V _I = 7 V			0.1			0.1	mA
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V			20			20	µA
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V			-0.2			-0.1	mA
I _O [§]	V _{CC} = 5.5 V, V _O = 2.25 V	-20	-112	-30	-112			mA
I _{CC}	SN74ALS540 V _{CC} = 5.5 V	Outputs high				5	10	mA
		Outputs low				13	22	
		Outputs disabled				11	19	
	'ALS541 V _{CC} = 5.5 V	Outputs high	6	14		6	14	
		Outputs low	15	25		15	25	
		Outputs disabled	13.5	32		13.5	22	

[†] Applies only to the -1 version and only if V_{CC} is between 4.75 V and 5.25 V

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX [¶]					UNIT	
			SN54ALS541		SN74ALS540		SN74ALS541		
			MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	4	17	2	12	4	14	ns
			2	14	2	9	2	10	
t _{PHL}	OE	Y	5	18	5	15	5	15	ns
			8	28	8	20	8	20	
t _{PZH}	OE	Y	1	12	1	10	1	10	ns
			2	14	2	12	2	12	
t _{PZL}									

[¶] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES

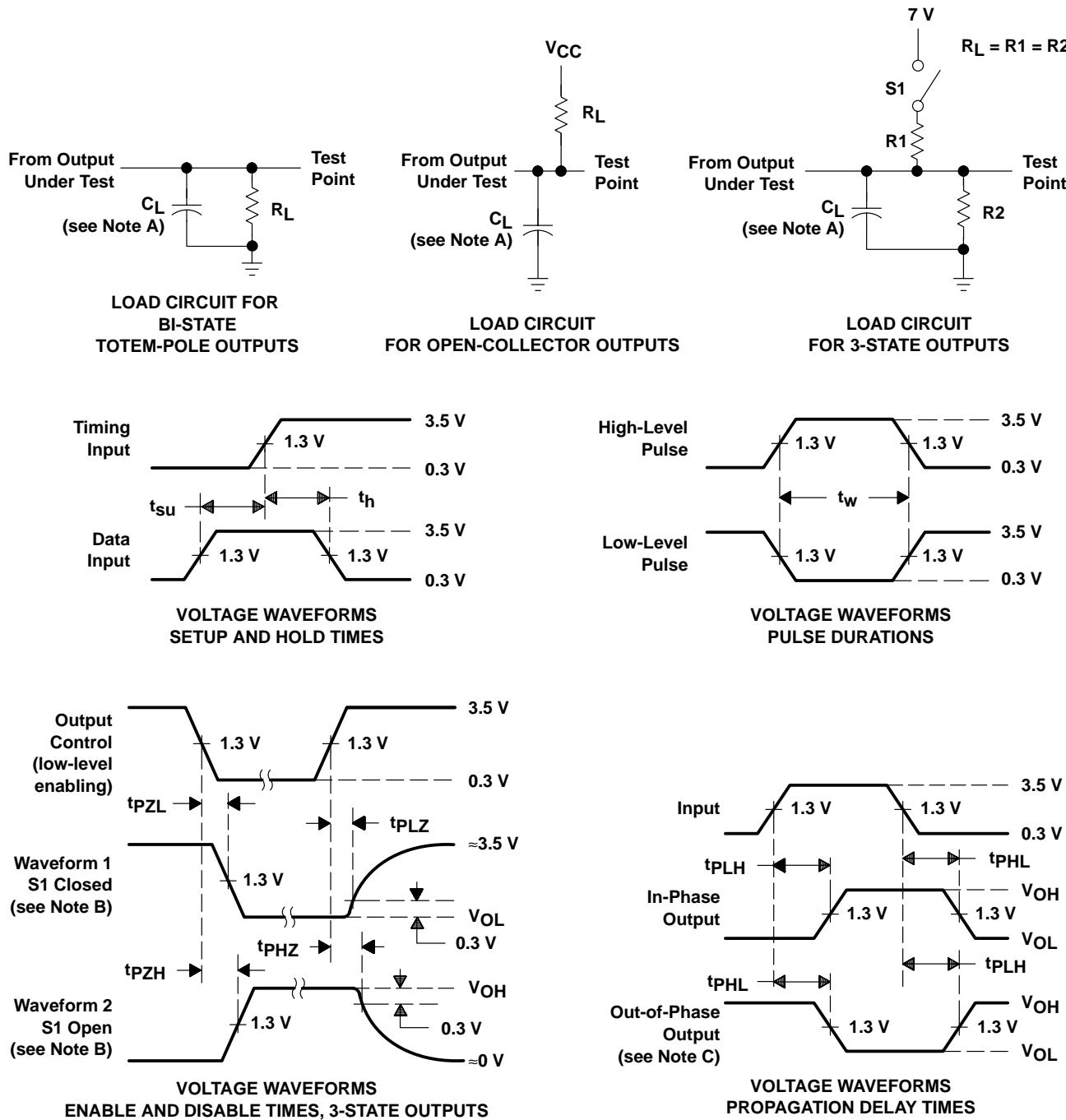


Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8960201RA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8960201RA SNJ54ALS541J	Samples
SN54ALS541J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54ALS541J	Samples
SN74ALS540-1N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS540-1N	Samples
SN74ALS540-1NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS540-1	Samples
SN74ALS540DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS540	Samples
SN74ALS540DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS540	Samples
SN74ALS540N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS540N	Samples
SN74ALS540NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS540	Samples
SN74ALS540NSRG4	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS540	Samples
SN74ALS541-1DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS541-1	Samples
SN74ALS541-1N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS541-1N	Samples
SN74ALS541-1NE4	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS541-1N	Samples
SN74ALS541-1NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS541-1	Samples
SN74ALS541-1NSRE4	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS541-1	Samples
SN74ALS541DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	G541	Samples
SN74ALS541DBRG4	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	G541	Samples
SN74ALS541DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS541	Samples
SN74ALS541DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS541	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALS541N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS541N	Samples
SN74ALS541NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS541	Samples
SN74ALS541NSRE4	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS541	Samples
SN74ALS541NSRG4	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS541	Samples
SNJ54ALS541J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8960201RA SNJ54ALS541J	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54ALS541, SN74ALS541 :

- Catalog : [SN74ALS541](#)
- Military : [SN54ALS541](#)

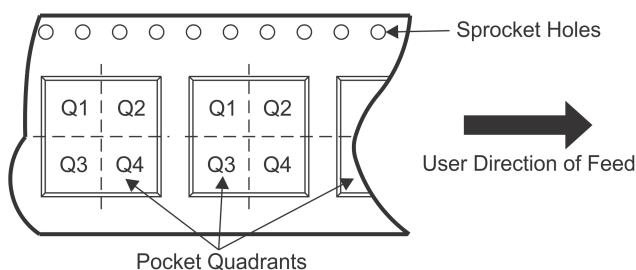
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


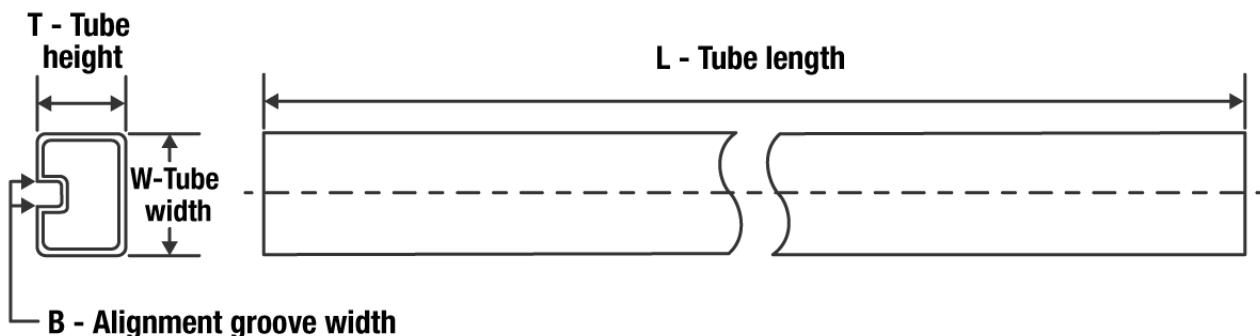
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS540-1NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74ALS540DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ALS540NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74ALS541-1NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74ALS541DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ALS541DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ALS541NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS540-1NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74ALS540DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74ALS540NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74ALS541-1NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74ALS541DBR	SSOP	DB	20	2000	853.0	449.0	35.0
SN74ALS541DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74ALS541NSR	SO	NS	20	2000	367.0	367.0	45.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ALS540-1N	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS540DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS540N	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS541-1DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS541-1N	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS541-1NE4	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS541DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS541N	N	PDIP	20	20	506	13.97	11230	4.32

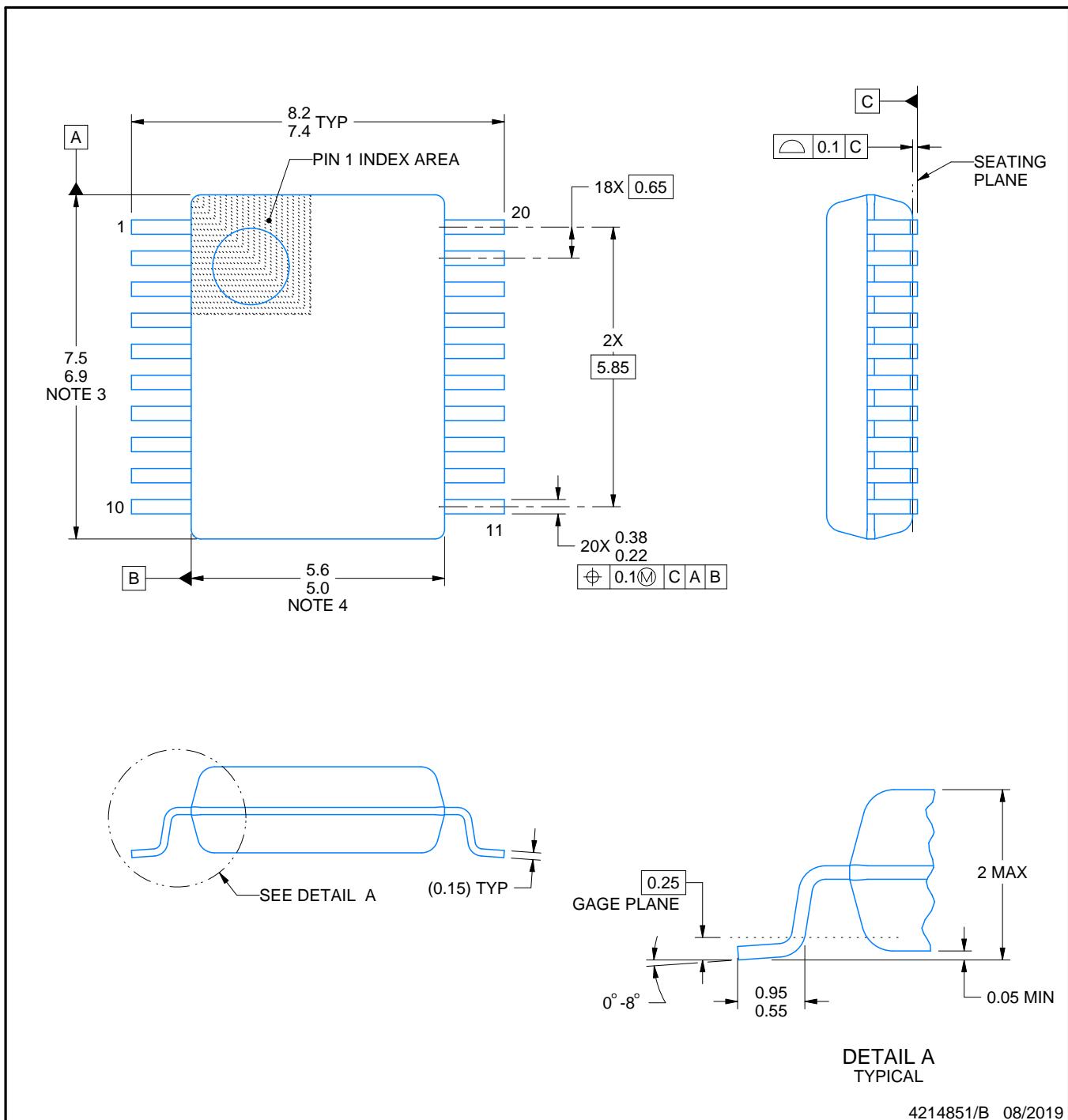
PACKAGE OUTLINE

DB0020A



SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

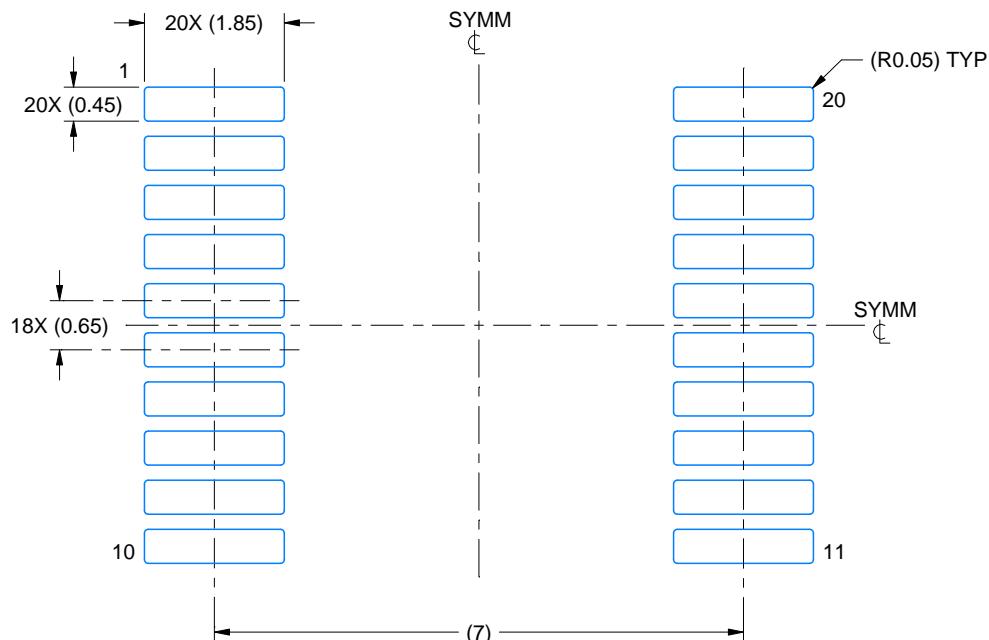
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

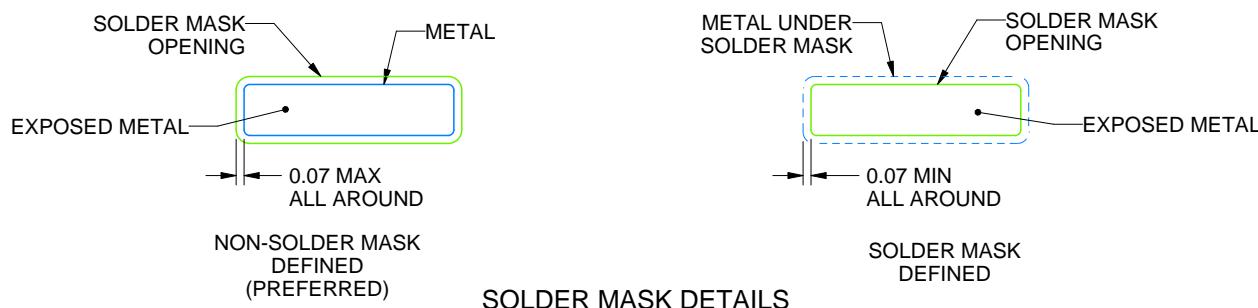
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

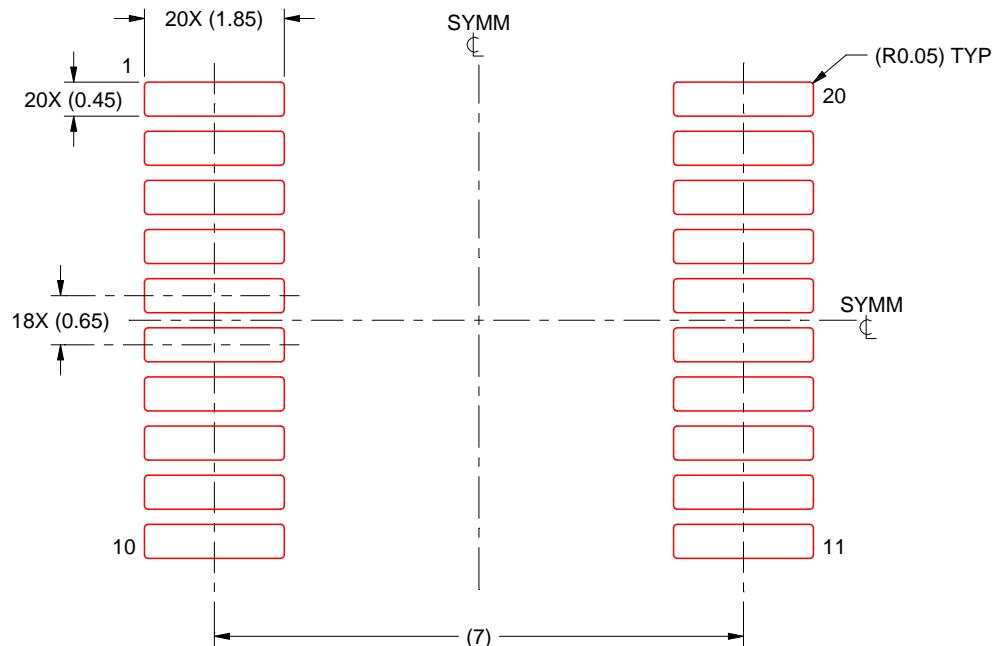
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



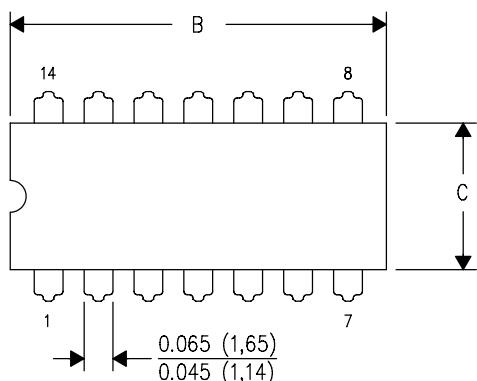
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

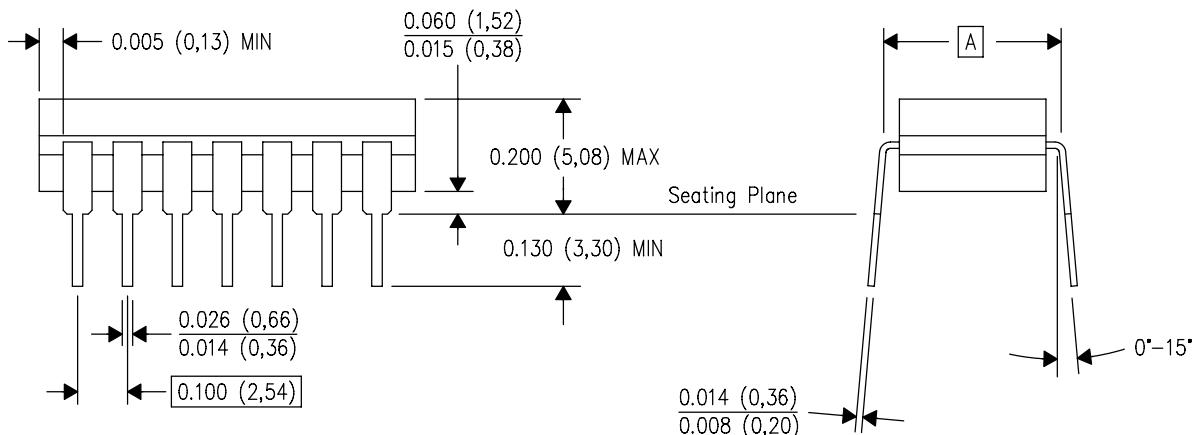
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



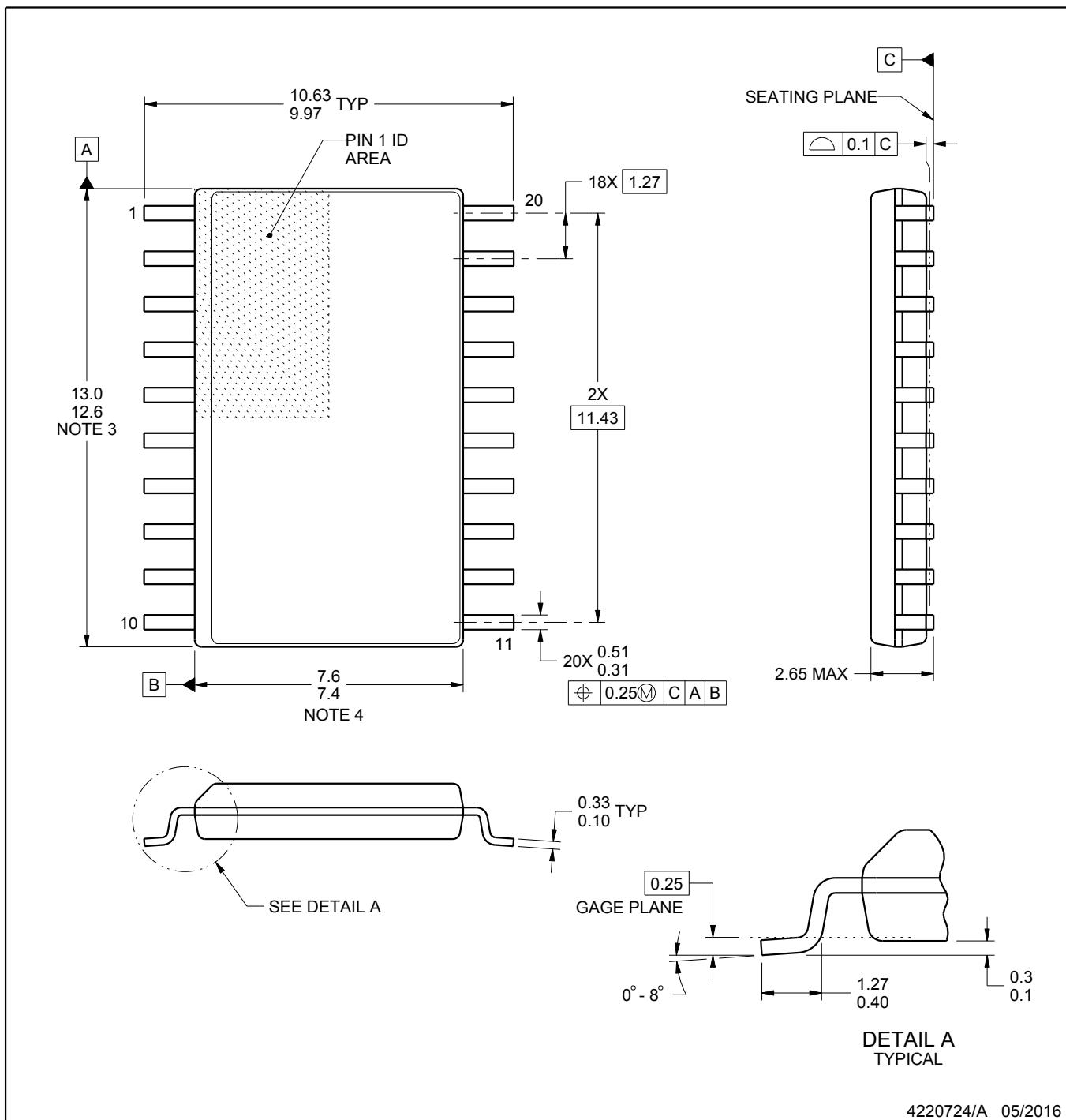
PACKAGE OUTLINE

DW0020A



SOIC - 2.65 mm max height

SOIC



NOTES:

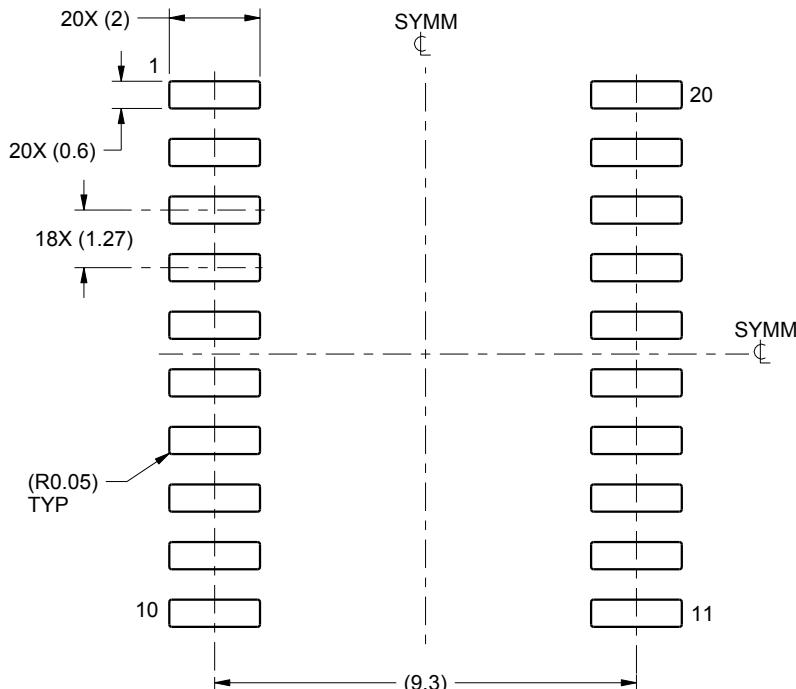
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

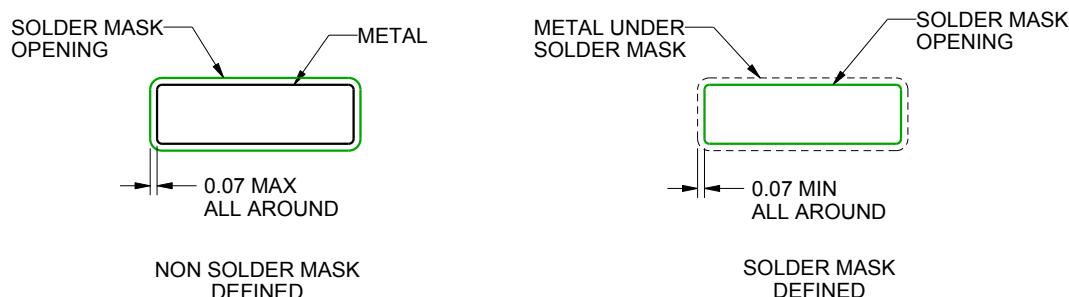
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

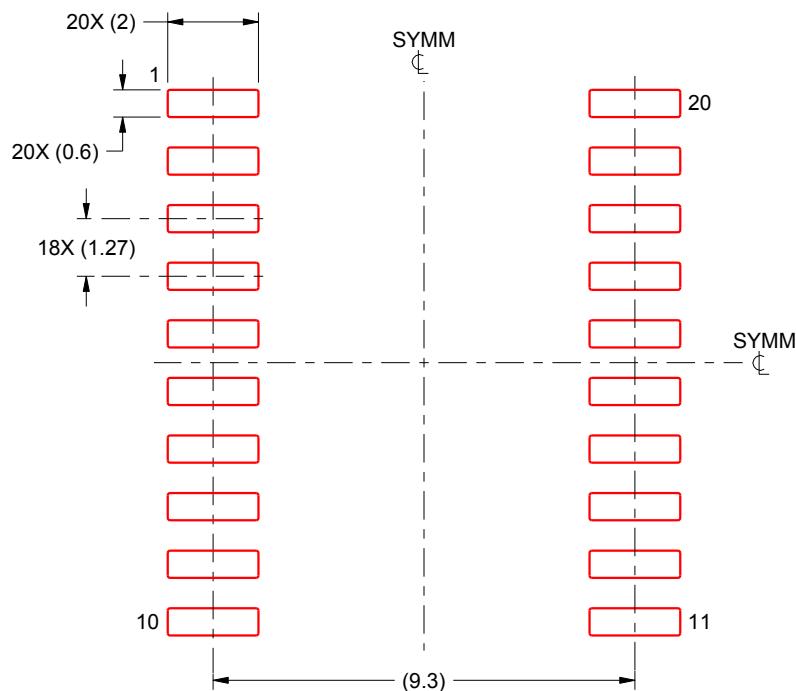
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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