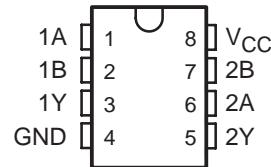


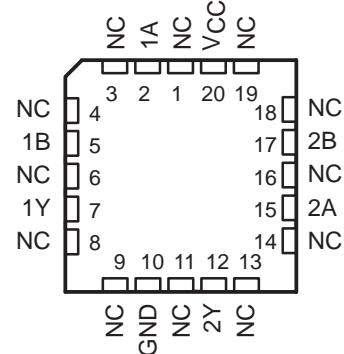
**PERIPHERAL DRIVERS FOR
HIGH-VOLTAGE, HIGH-CURRENT DRIVER
APPLICATIONS**

- Characterized for Use to 300 mA
- High-Voltage Outputs
- No Output Latch-Up at 30 V (After Conducting 300 mA)
- Medium-Speed Switching
- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL-Compatible Diode-Clamped Inputs
- Standard Supply Voltages
- Plastic DIP (P) With Copper Lead Frame for Cooler Operation and Improved Reliability
- Package Options Include Plastic Small Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

SN55461, SN55462, SN55463 . . . JG PACKAGE
SN75461, SN75462, SN75463 . . . D OR P PACKAGE
(TOP VIEW)



SN55461, SN55462, SN55463 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

SUMMARY OF SERIES 55461/75461

DEVICE	LOGIC	PACKAGES
SN55461	AND	FK, JG
SN55462	NAND	FK, JG
SN55463	OR	FK, JG
SN75461	AND	D, P
SN75462	NAND	D, P
SN75463	OR	D, P

description

These dual peripheral drivers are functionally interchangeable with SN55451B through SN55453B and SN75451B through SN75453B peripheral drivers, but are designed for use in systems that require higher breakdown voltages than those devices can provide at the expense of slightly slower switching speeds. Typical applications include logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers.

The SN55461/SN75461, SN55462/SN75462, and SN55463/SN75463 are dual peripheral AND, NAND, and OR drivers respectively (assuming positive logic), with the output of the gates internally connected to the bases of the npn output transistors.

Series SN55461 drivers are characterized for operation over the full military temperature range of -55°C to 125°C . Series SN75461 drivers are characterized for operation from 0°C to 70°C .

SN55461 THRU SN55463

SN75461 THRU SN75463

DUAL PERIPHERAL DRIVERS

SLRS022A - DECEMBER 1976 - REVISED OCTOBER 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

	SN55'	SN75'	UNIT
Supply voltage, V_{CC} (see Note 1)	7	7	V
Input voltage, V_I	5.5	5.5	V
Integrator voltage (see Note 2)	5.5	5.5	V
Off-state output voltage, V_O	35	35	V
Continuous collector or output current (see Note 3)	400	400	mA
Peak collector or output current ($t_W \leq 10$ ms, duty cycle $\leq 50\%$, see Note 4)	500	500	mA
Continuous total power dissipation	See Dissipation Rating Table		
Operating free-air temperature range, T_A	-55 to 125	0 to 70	°C
Storage temperature range, T_{STG}	-65 to 150	-65 to 150	°C
Case temperature for 60 seconds, T_C	FK package	260	°C
Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds	JG package	300	°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	D or P package	260	°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network GND unless otherwise specified.

2. This is the voltage between two emitters A and B.

3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500Ω .

4. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
			$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	-
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	-

recommended operating conditions

	SN55'			SN75'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
Operating free-air temperature, T_A	-55	125		0	70		°C



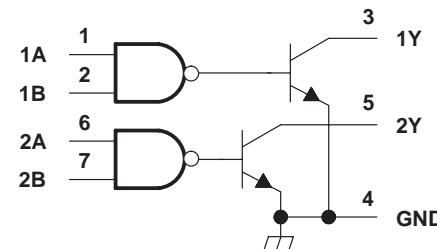
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, JG, and P packages.

logic diagram (positive logic)

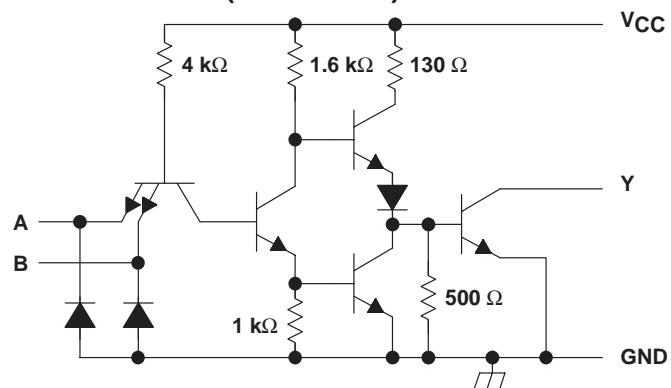


FUNCTION TABLE
(each driver)

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

positive logic:
 $Y = AB \text{ or } \bar{A} + \bar{B}$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS†	SN55461			SN75461			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$	-1.2	-1.5		-1.2	-1.5		V
I_{OH}	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{OH} = 35 \text{ V}$		300			100		μA
V_{OL}	$V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 100 \text{ mA}$	0.25	0.5		0.25	0.4		V
	$V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 300 \text{ mA}$	0.5	0.8		0.5	0.7		
I_I	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$		1			1		mA
I_{IH}	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$		40			40		μA
I_{IL}	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$	-1	-1.6		-1	-1.6		mA
I_{CCH}	$V_{CC} = \text{MAX}$, $V_I = 5 \text{ V}$	8	11		8	11		mA
I_{CCL}	$V_{CC} = \text{MAX}$, $V_I = 0$	56	76		56	76		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	$I_O \approx 200 \text{ mA}$, $C_L = 15 \text{ pF}$, $R_L = 50 \Omega$, See Figure 1	30	55		ns
t_{PHL}		25	40		
t_{TLH}		8	20		
t_{THL}		10	20		
V_{OH}	$SN55461$	$V_S = 30 \text{ V}$, $I_O \approx 300 \text{ mA}$, See Figure 2	$V_S - 10$		mV
	$SN75461$		$V_S - 10$		

**SN55461 THRU SN55463
SN75461 THRU SN75463
DUAL PERIPHERAL DRIVERS**

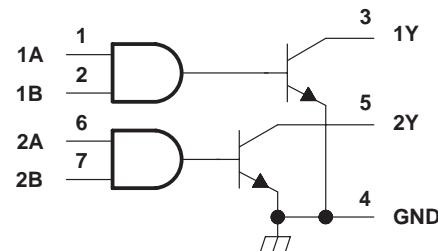
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, JG, and P packages.

logic diagram (positive logic)

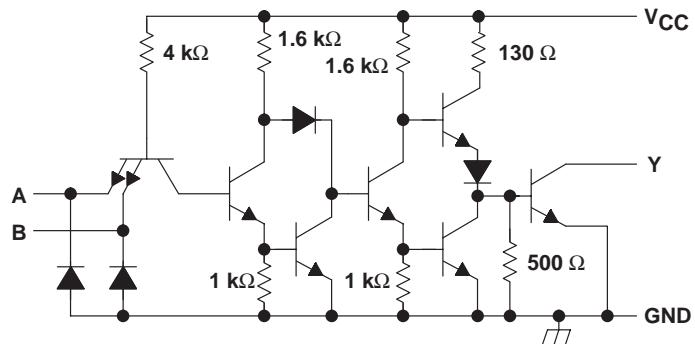


**FUNCTION TABLE
(each driver)**

A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

positive logic:
 $Y = AB \text{ or } A + B$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS†	SN55462			SN75462			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$		-1.2	-1.5		-1.2	-1.5	V
I_{OH}	$V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $V_{OH} = 35 \text{ V}$		300			100		μA
V_{OL}	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $I_{OL} = 100 \text{ mA}$		0.25	0.5		0.25	0.4	V
	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $I_{OL} = 300 \text{ mA}$		0.5	0.8		0.5	0.7	
I_I	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$		1			1		mA
I_{IH}	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$		40			40		μA
I_{IL}	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$	-1.1	-1.6		-1.1	-1.6		mA
I_{CCH}	$V_{CC} = \text{MAX}$, $V_I = 0$	13	17		13	17		mA
I_{CLL}	$V_{CC} = \text{MAX}$, $V_I = 5 \text{ V}$	61	76		61	76		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

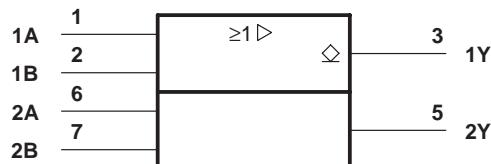
switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	$I_O \approx 200 \text{ mA}$, $C_L = 15 \text{ pF}$, $R_L = 50 \Omega$, See Figure 1		45	65	ns
t_{PHL}			30	50	
t_{TLH}			13	25	
t_{THL}			10	20	
V_{OH}	SN55462 SN75462	$V_S = 30 \text{ V}$, $I_O \approx 300 \text{ mA}$			mV
		$V_S - 10$			
		$V_S - 10$			

 **TEXAS
INSTRUMENTS**

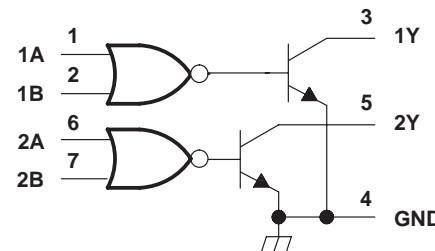
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984
 and IEC Publication 617-12.
 Pin numbers shown are for D, JG, and P packages.

logic diagram (positive logic)

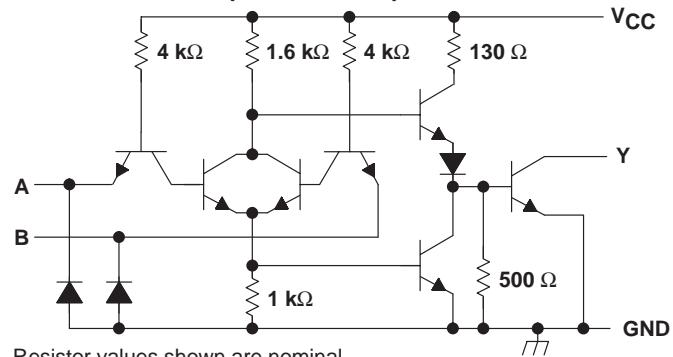


**FUNCTION TABLE
 (each driver)**

A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

positive logic:
 $Y = A + B \text{ or } \overline{A} \overline{B}$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS†	SN55463			SN75463			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -12 mA		-1.2	-1.5		-1.2	-1.5	V
I _{OH} High-level output current	V _{CC} = MIN, V _{IH} = MIN, V _{OH} = 35 V		300			100		µA
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OL} = 100 mA		0.25	0.5		0.25	0.4	V
	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OL} = 300 mA		0.5	0.8		0.5	0.7	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V		1			1		mA
I _{IH} High-level input current	V _{CC} = MAX, V _I = 2.4 V		40			40		µA
I _{IL} Low-level input current	V _{CC} = MAX, V _I = 0.4 V		-1	-1.6		-1	-1.6	mA
I _{CCH} Supply current, outputs high	V _{CC} = MAX, V _I = 5 V		8	11		8	11	mA
I _{CCL} Supply current, outputs low	V _{CC} = MAX, V _I = 0		58	76		58	76	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

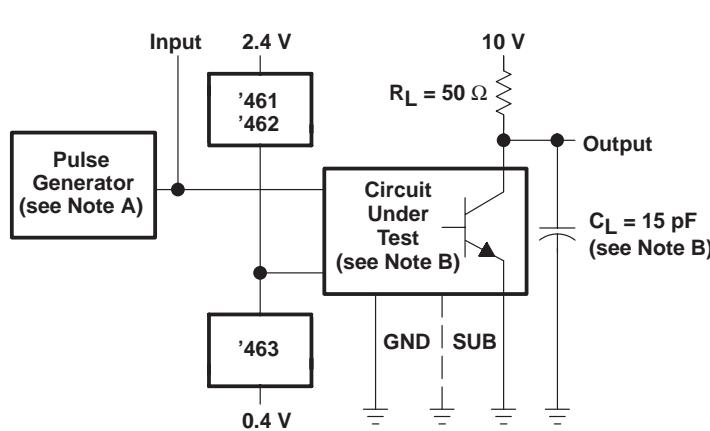
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH} Propagation delay time, low-to-high-level output	I _O ≈ 200 mA, C _L = 15 pF, R _L = 50 Ω, See Figure 1		30	55	ns
t _{PHL} Propagation delay time, high-to-low-level output			25	40	
t _{TLH} Transition time, low-to-high-level output			8	25	
t _{THL} Transition time, high-to-low-level output			10	25	
V _{OH} High-level output voltage after switching	SN55463 SN75463	V _S = 30 V, I _O ≈ 300 mA, See Figure 2	V _S - 10		mV
			V _S - 10		

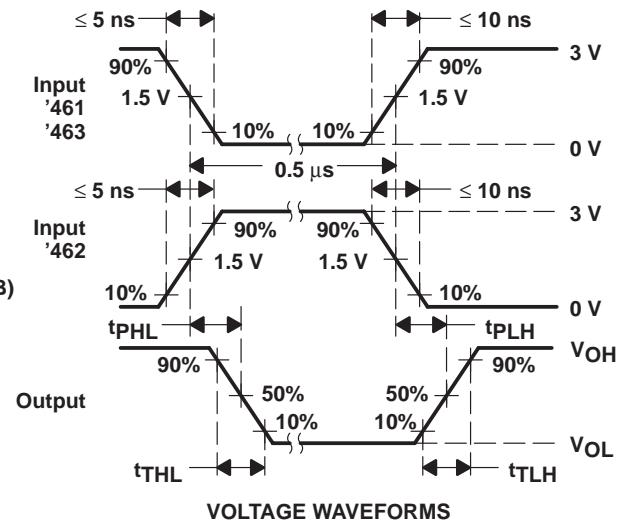
**SN55461 THRU SN55463
SN75461 THRU SN75463
DUAL PERIPHERAL DRIVERS**

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PARAMETER MEASUREMENT INFORMATION

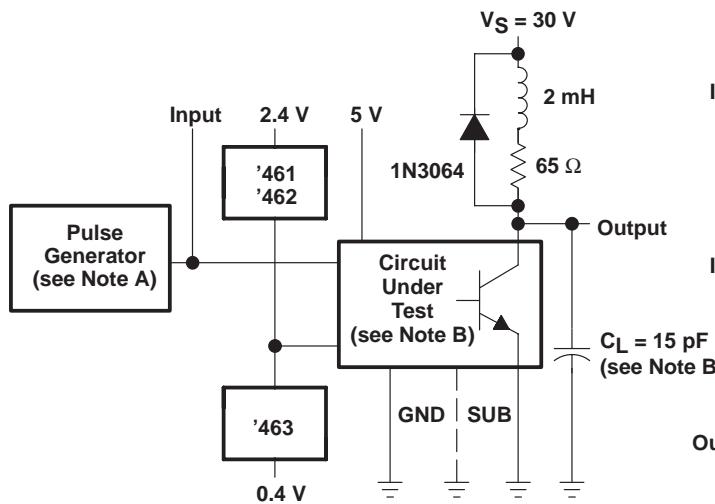


TEST CIRCUIT

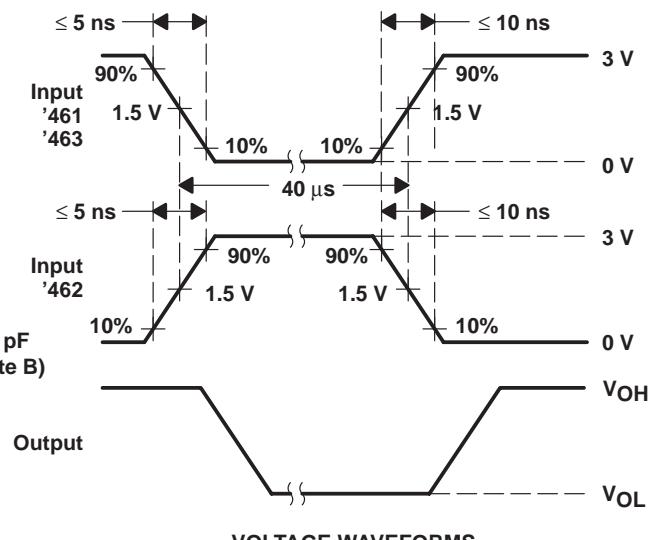


NOTES: A. The pulse generator has the following characteristics: PRR \leq 1 MHz, $Z_O \approx 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms for Switching Times



TEST CIRCUIT



NOTES: A. The pulse generator has the following characteristics: PRR \leq 12.5 kHz, $Z_O = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms for Latch-Up Test

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/12908BPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510 /12908BPA	Samples
M38510/12908BPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510 /12908BPA	Samples
SN75462D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75462	Samples
SN75462DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75462	Samples
SN75462P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75462P	Samples
SN75462PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75462P	Samples
SN75463P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75463P	Samples
SNJ55462FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ55 462FK	Samples
SNJ55462JG	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ55462JG	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN55462, SN75462 :

- Catalog : [SN75462](#)
- Military : [SN55462](#)

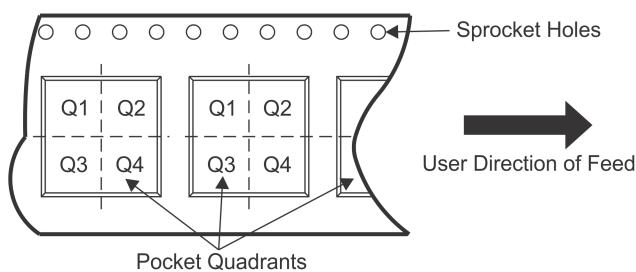
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


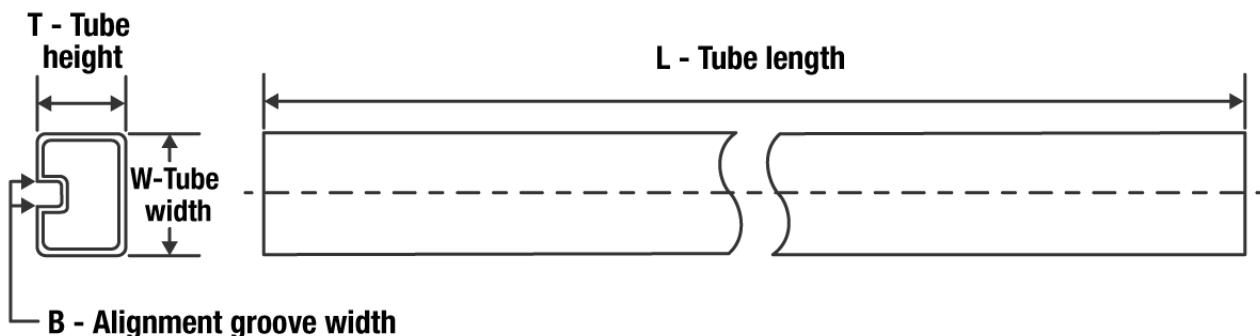
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75462DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75462DR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75462D	D	SOIC	8	75	507	8	3940	4.32
SN75462P	P	PDIP	8	50	506	13.97	11230	4.32
SN75462PE4	P	PDIP	8	50	506	13.97	11230	4.32
SN75463P	P	PDIP	8	50	506	13.97	11230	4.32
SNJ55462FK	FK	LCCC	20	1	506.98	12.06	2030	NA

FK (S-CQCC-N**)

28 TERMINAL SHOWN

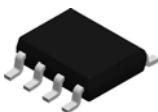
LEADLESS CERAMIC CHIP CARRIER



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

4040140/D 01/11

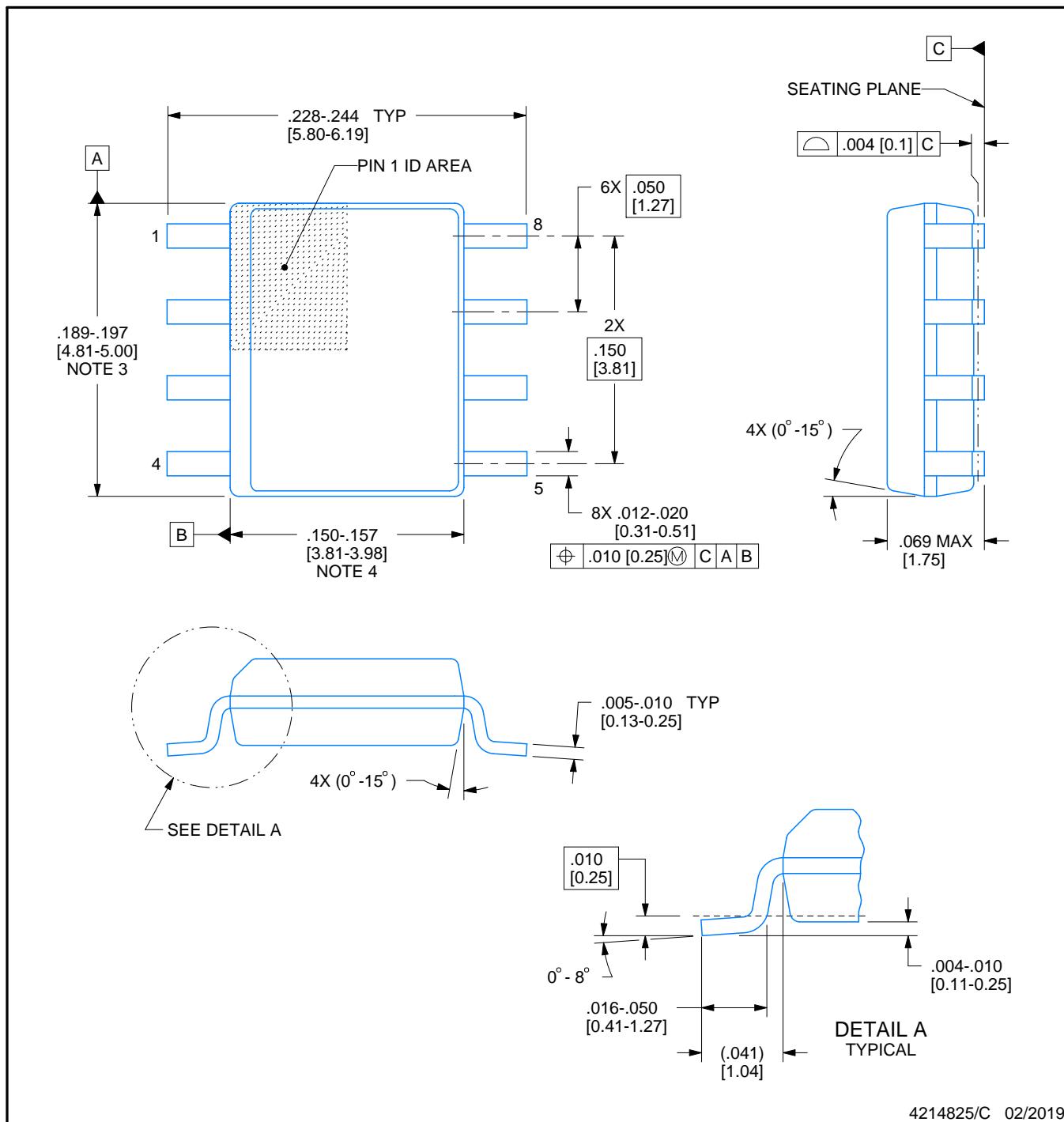


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

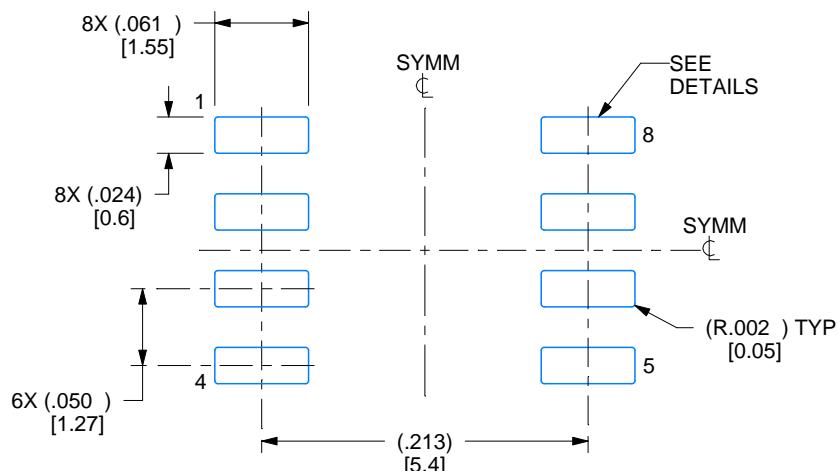
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

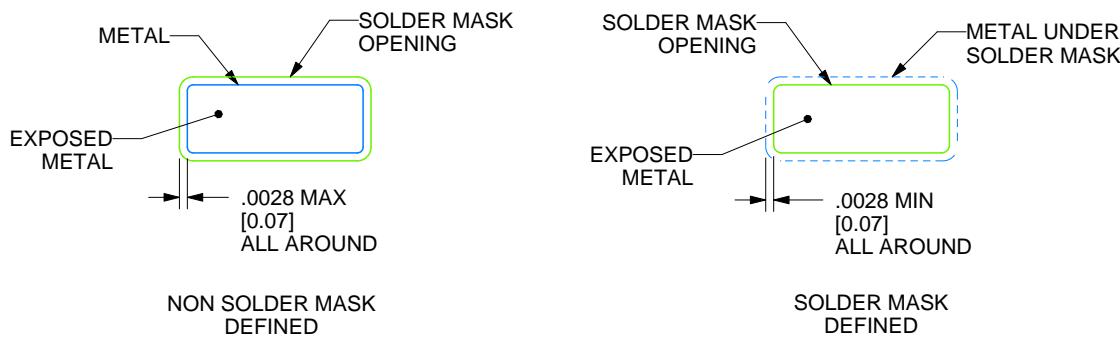
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

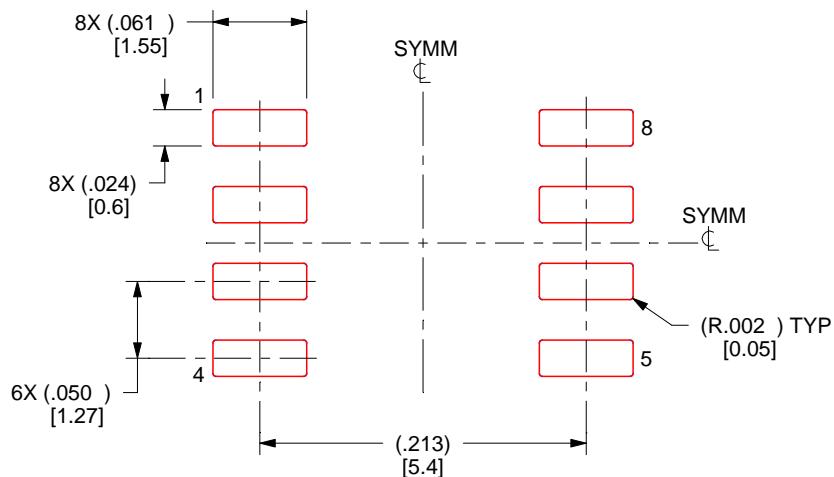
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

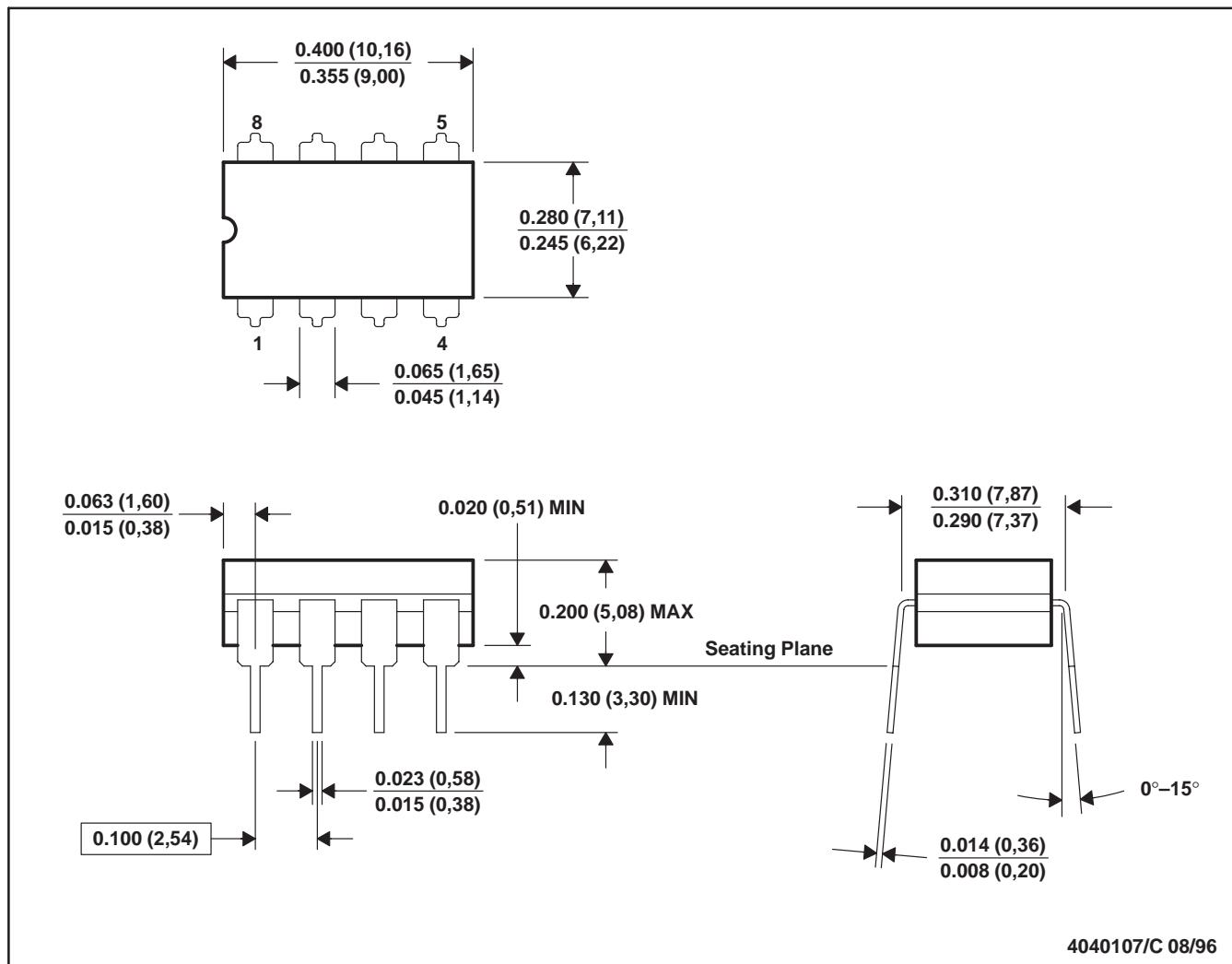
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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

JG (R-GDIP-T8)

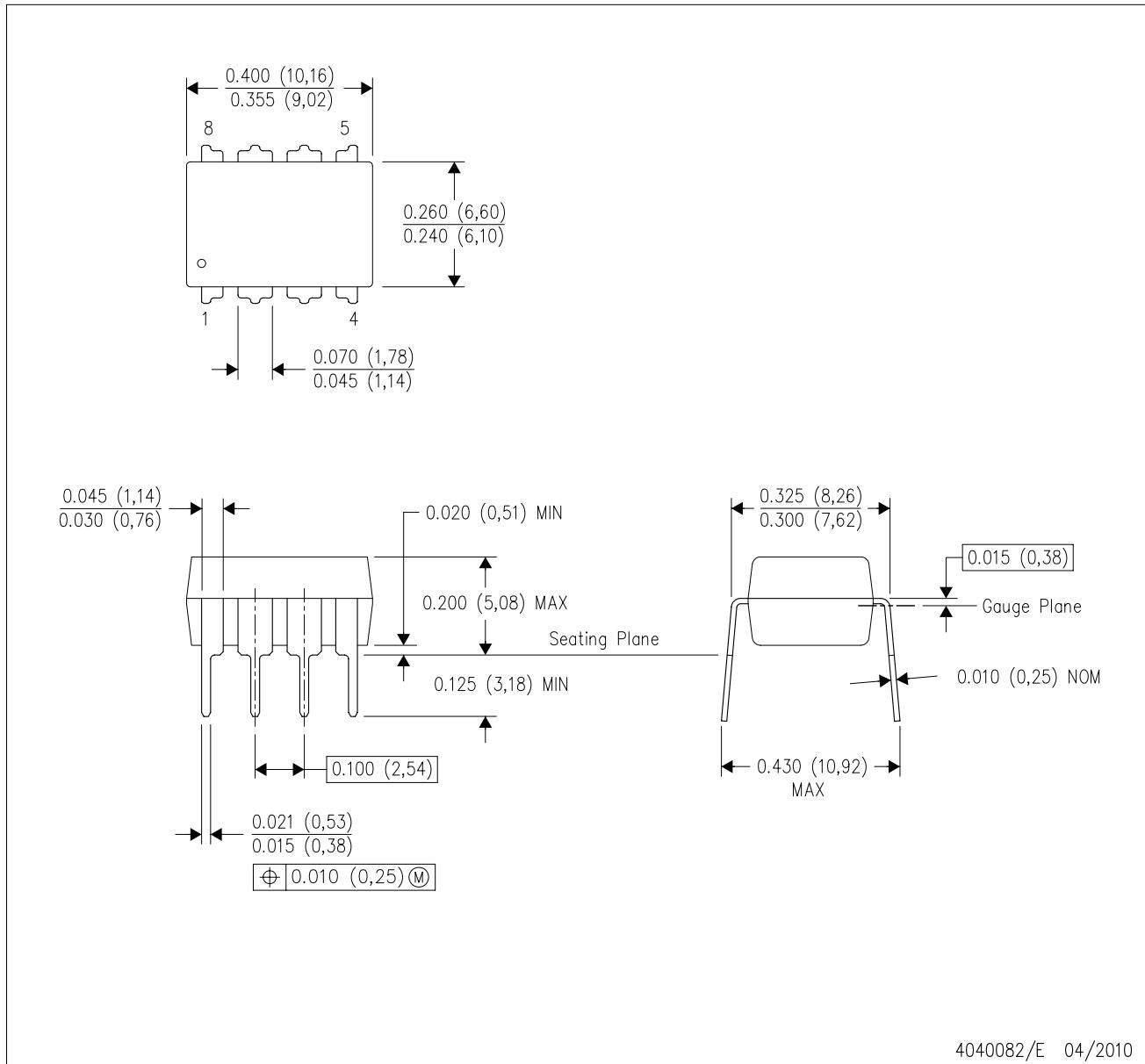
CERAMIC DUAL-IN-LINE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP1-T8

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



4040082/E 04/2010

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.

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