

# MOSFET - Power, Single N-Channel, TOLL 60 V, 0.75 mΩ, 470 A

## NTBLS0D7N06C

### Features

- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- Lowers Switching Noise/EMI
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- Power Tools, Battery Operated Vacuums
- UAV/Drones, Material Handling
- BMS/Storage, Home Automation

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			$V_{DSS}$	60	V
Gate-to-Source Voltage			$V_{GS}$	$\pm 20$	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	$T_C = 25^{\circ}\text{C}$	$I_D$	470	A
Power Dissipation $R_{\theta JC}$ (Note 2)		$T_C = 25^{\circ}\text{C}$	$P_D$	314	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^{\circ}\text{C}$	$I_D$	54	A
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		$T_A = 25^{\circ}\text{C}$	$P_D$	4.2	W
Pulsed Drain Current	$T_A = 25^{\circ}\text{C}$ , $t_p = 10\text{ }\mu\text{s}$		$I_{DM}$	900	A
Operating Junction and Storage Temperature Range			$T_J$ , $T_{stg}$	-55 to +175	$^{\circ}\text{C}$
Source Current (Body Diode)			$I_S$	260	A
Single Pulse Drain-to-Source Avalanche Energy ( $I_{L(pk)} = 40\text{ A}$ )			$E_{AS}$	800	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)			$T_L$	260	$^{\circ}\text{C}$

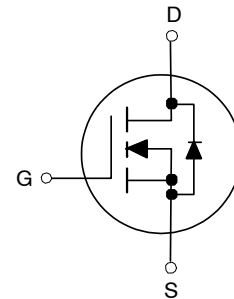
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 2)	$R_{\theta JC}$	0.48	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	36	

1. Surface-mounted on FR4 board using a 1 in<sup>2</sup> pad size, 2 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
60 V	0.75 mΩ @ 10 V	470 A
	1.2 mΩ @ 6 V	



H-PSOF8L  
CASE 100CU

### ORDERING INFORMATION

Device	Package	Shipping†
NTBLS0D7N06C	H-PSOF8L (Pb-Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTBLS0D7N06C

**Table 1. ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0\ \text{V}$	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 661\ \mu\text{A}$ , ref to $25^\circ\text{C}$		26.5		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 60\ \text{V}$ , $V_{GS} = 0\ \text{V}$	$T_J = 25^\circ\text{C}$		10	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		100	$\mu\text{A}$
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\ \text{V}$ , $V_{GS} = 20\ \text{V}$			100	nA

## ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$ , $I_D = 661\ \mu\text{A}$	2.0	2.8	4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(th)}/T_J$	$I_D = 661\ \mu\text{A}$ , ref to $25^\circ\text{C}$		9.8		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\ \text{V}$ , $I_D = 80\ \text{A}$		0.56	0.75	m $\Omega$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 6\ \text{V}$ , $I_D = 66\ \text{A}$		0.85	1.20	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS} = 10\ \text{V}$ , $I_D = 80\ \text{A}$		310		S
Gate-Resistance	$R_G$	$T_A = 25^\circ\text{C}$		0.6		$\Omega$

## CHARGES & CAPACITANCES

Input Capacitance	$C_{iss}$	$V_{GS} = 0\ \text{V}$ , $V_{DS} = 30\ \text{V}$ , $f = 10\ \text{kHz}$		13730		pF
Output Capacitance	$C_{oss}$			6912		pF
Reverse Transfer Capacitance	$C_{rss}$			92		pF
Total Gate Charge	$Q_{G(tot)}$	$V_{GS} = 10\ \text{V}$ , $V_{DS} = 30\ \text{V}$ , $I_D = 80\ \text{A}$		170		nC
Threshold Gate Charge	$Q_{G(th)}$			39		nC
Gate-to-Source Charge	$Q_{gs}$			62		nC
Gate-to-Drain Charge	$Q_{gd}$			16		nC
Total Gate Charge	$Q_{G(tot)}$	$V_{GS} = 6\ \text{V}$ , $V_{DS} = 30\ \text{V}$ , $I_D = 80\ \text{A}$		102		nC

## SWITCHING CHARACTERISTICS, $V_{GS} = 10\ \text{V}$ (Note 3)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10\ \text{V}$ , $V_{DS} = 30\ \text{V}$ , $I_D = 80\ \text{A}$ , $R_G = 6\ \Omega$		37		ns
Rise Time	$t_r$			57		ns
Turn-Off Delay Time	$t_{d(off)}$			146		ns
Fall Time	$t_f$			105		ns

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$I_S = 80\ \text{A}$ , $V_{GS} = 0\ \text{V}$	$T_J = 25^\circ\text{C}$		0.79	1.2	V
		$I_S = 80\ \text{A}$ , $V_{GS} = 0\ \text{V}$	$T_J = 125^\circ\text{C}$		0.66		V
Reverse Recovery Time	$t_{rr}$	$V_{GS} = 0\ \text{V}$ , $dI_S/dt = 100\ \text{A}/\mu\text{s}$ , $I_S = 66\ \text{A}$		132			ns
Charge Time	$t_a$			64			ns
Discharge Time	$t_b$			68			ns
Reverse Recovery Charge	$Q_{rr}$			386			nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

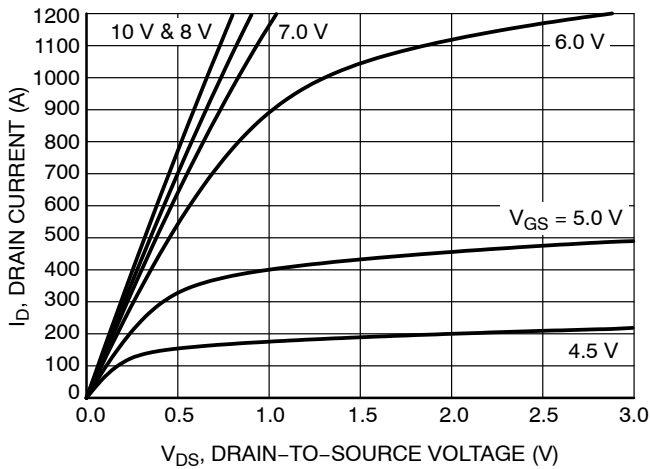


Figure 1. On-Region Characteristics

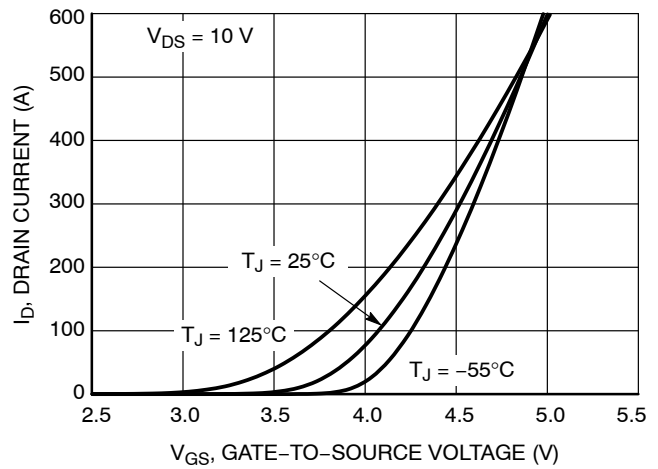


Figure 2. Transfer Characteristics

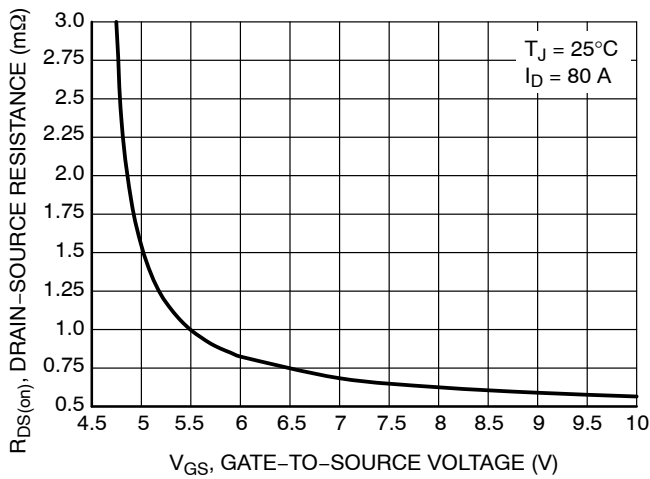


Figure 3. On-Resistance vs.  $V_{GS}$

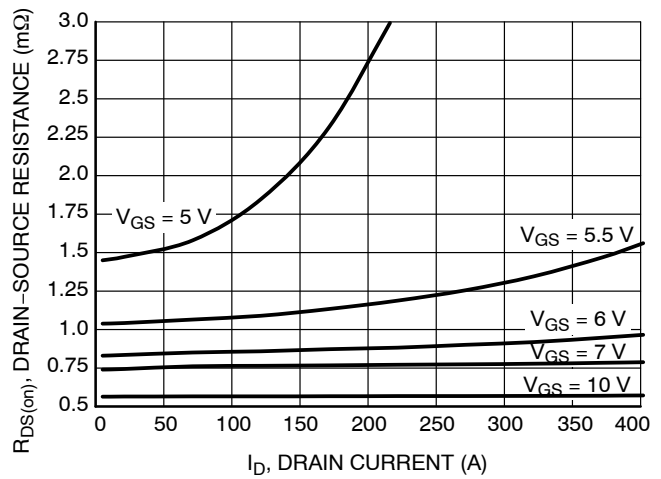


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

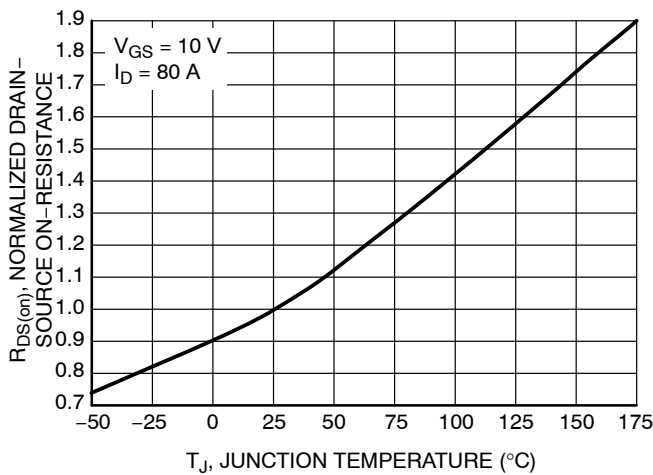


Figure 5. On-Resistance Variation with Temperature

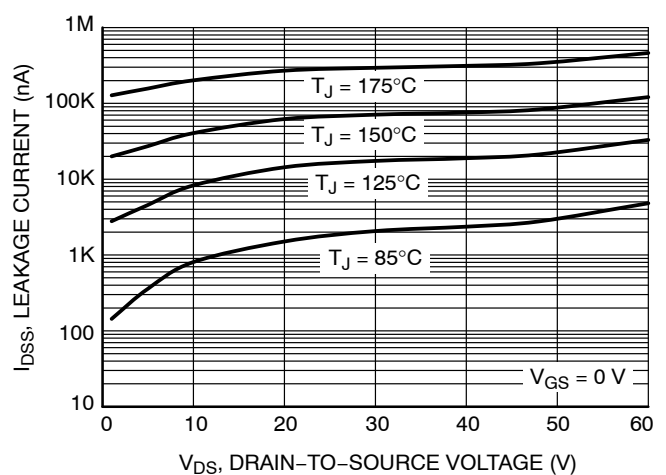


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

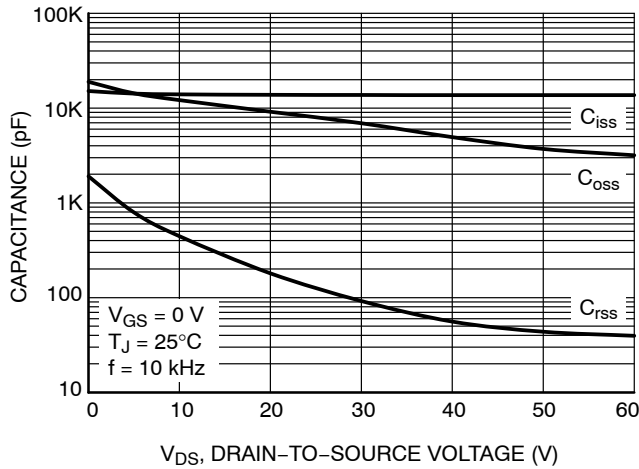


Figure 7. Capacitance Variation

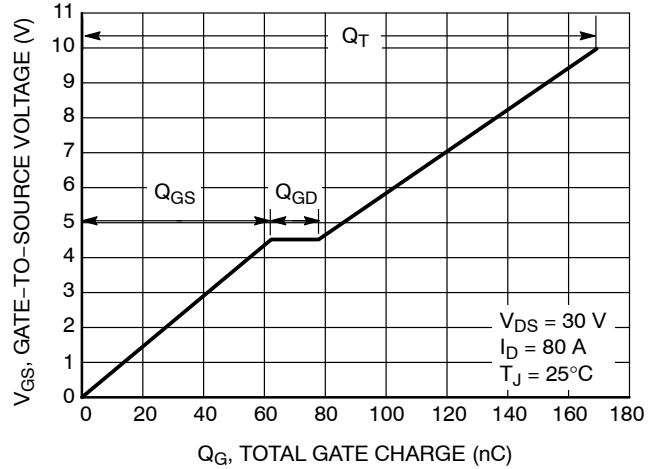


Figure 8. Gate-to-Source Voltage vs. Total Gate Charge

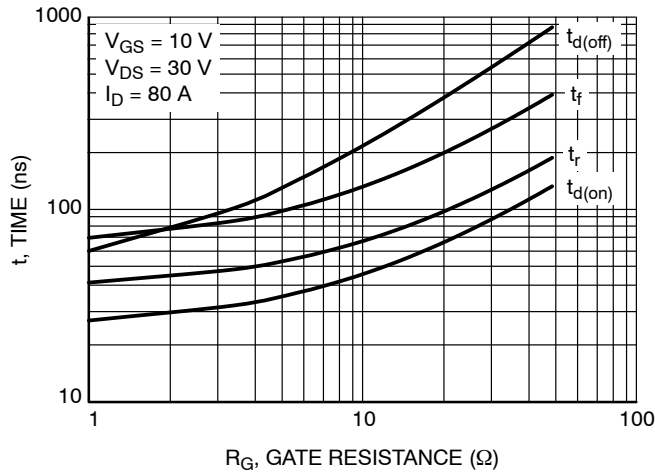


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

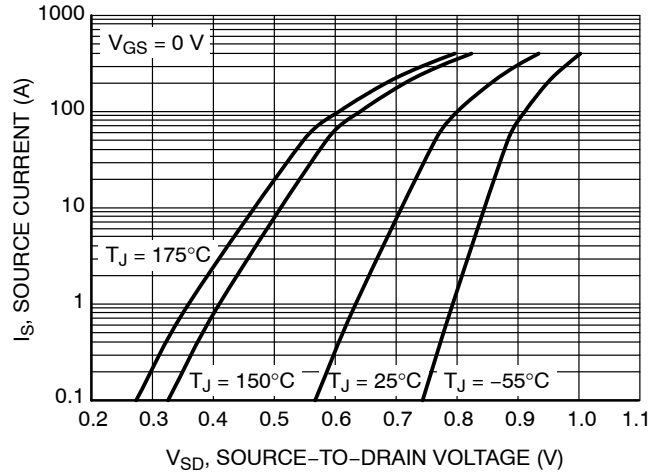


Figure 10. Diode Forward Voltage vs. Current

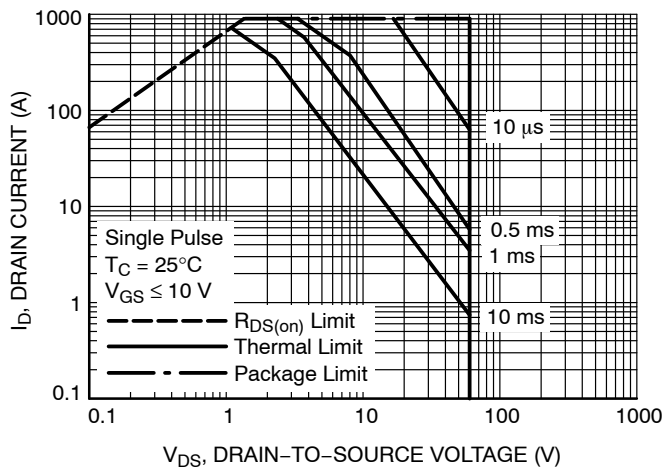


Figure 11. Maximum Rated Forward Biased Safe Operating Area

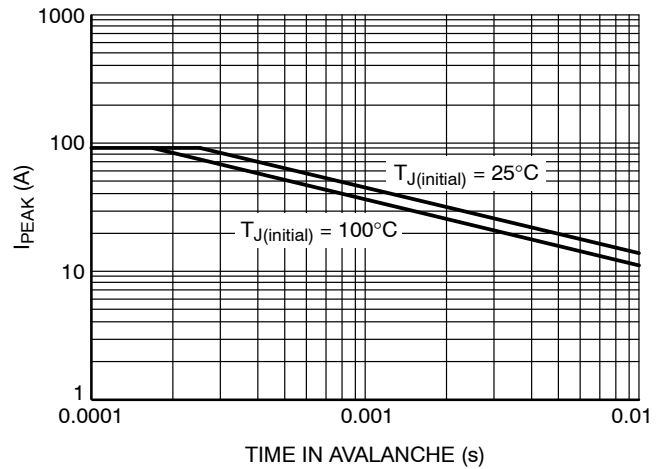


Figure 12.  $I_{PEAK}$  vs. Time in Avalanche

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## TYPICAL CHARACTERISTICS

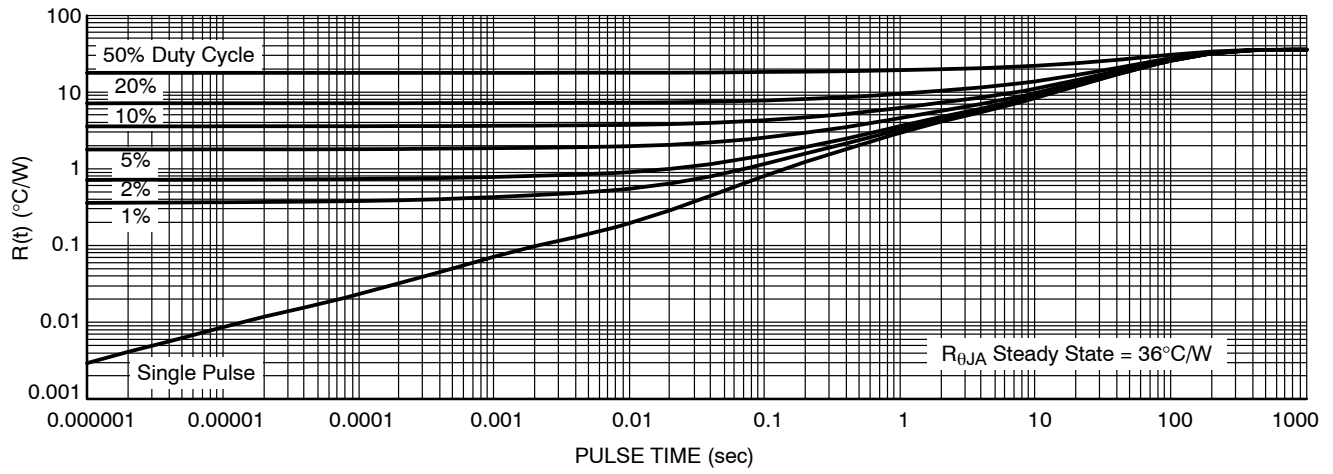


Figure 13. Thermal Characteristics (Junction-to-Ambient)

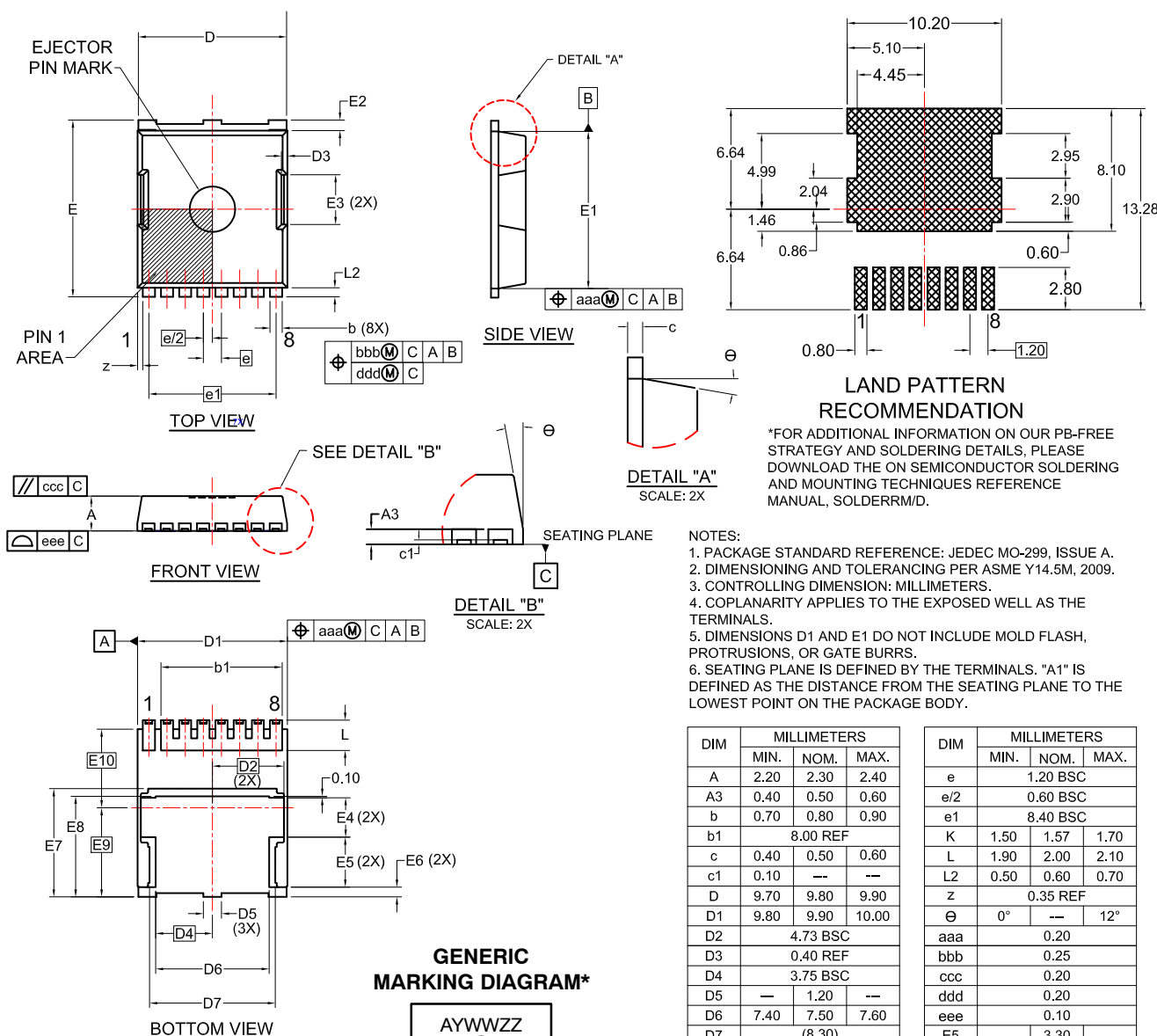
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



## H-PSOF8L 11.68x9.80 CASE 100CU ISSUE A

DATE 06 JAN 2020



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A3	0.40	0.50	0.60
b	0.70	0.80	0.90
b1	8.00 REF		
c	0.40	0.50	0.60
c1	0.10	---	---
D	9.70	9.80	9.90
D1	9.80	9.90	10.00
D2	4.73 BSC		
D3	0.40 REF		
D4	3.75 BSC		
D5	---	1.20	---
D6	7.40	7.50	7.60
D7	(8.30)		
E	11.58	11.68	11.78
E1	10.28	10.38	10.48
E2	0.60	0.70	0.80
E3	3.30 REF		
E4	---	2.60	---

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
e	1.20 BSC		
e/2	0.60 BSC		
e1	8.40 BSC		
K	1.50	1.57	1.70
L	1.90	2.00	2.10
L2	0.50	0.60	0.70
z	0.35 REF		
θ	0°	---	12°
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		
E5	---	3.30	---
E6	---	0.65	---
E7	7.15 REF		
E8	6.55	6.65	6.75
E9	5.89 BSC		
E10	5.19 BSC		

A = Assembly Location  
Y = Year  
WW = Work Week  
ZZ = Assembly Lot Code  
XXXX = Specific Device Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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