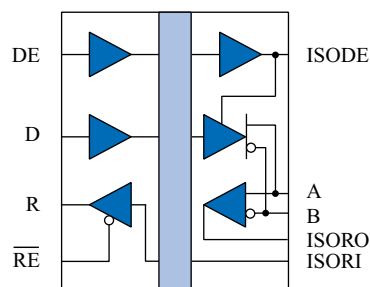
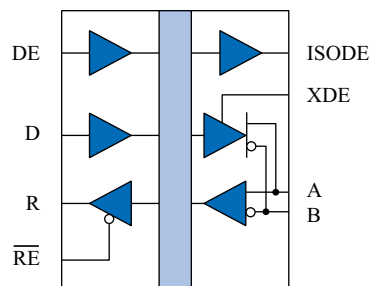


Advanced Isolated RS-485 Transceivers

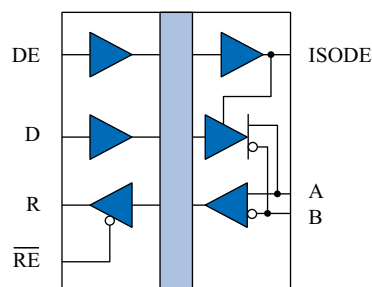
Functional Diagrams



IL3685-1
(QSOP)



IL3685-3
(narrow-body)

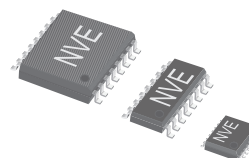


IL3685
(wide-body)

| $V_{ID} (A-B)$ | DE | \overline{RE} | R | D | Mode |
|------------------------|----|-----------------|---|---|---------|
| $\geq 200 \text{ mV}$ | L | L | H | X | Receive |
| $\leq -200 \text{ mV}$ | L | L | L | X | Receive |
| $\geq 1.5 \text{ V}$ | H | L | H | H | Drive |
| $\leq -1.5 \text{ V}$ | H | L | L | L | Drive |
| X | X | H | Z | X | Hi-Z R |
| Open | L | L | H | X | Receive |

Features

- 40 Mbps data rate
- 3 V to 5 V power supplies
- 20 ns propagation delay
- Hot-plug capable
- 50 kV/ μs typ.; 30 kV/ μs min. common mode transient immunity
- 44000 year barrier life
- 15 kV bus ESD protection
- Low EMC footprint
- Thermal shutdown protection
- -40°C to $+85^\circ\text{C}$ temperature range
- Meets or exceeds ANSI RS-485 and ISO 8482:1987(E)
- PROFIBUS compliant
- 6 kV_{RMS} Reinforced Isolation/12.8 kV surge/1 kV_{RMS} WV (V-Series)
- VDE V 0884-11 / IEC 60747-17 certified; UL 1577 recognized
- QSOP, 0.15", or 0.3" 16-pin packages



Applications

- PROFIBUS, PROFIBUS DP, and FMS networks
- Factory automation
- Industrial control networks
- Building environmental controls
- Equipment covered under IEC 61010-1 Edition 3

Description

IL3685-Series are second-generation isolated, high-speed differential bus transceivers. The devices use NVE's patented* IsoLoop spintronic Giant Magnetoresistance (GMR) technology and have advanced features such as hot-plug capability and PROFIBUS compliance.

The wide-body version provides true 8 mm creepage. Narrow-body and QSOP packages offer unprecedented miniaturization.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

The device is compatible with 3 V as well as 5 V input supplies, allowing interface to standard microcontrollers without additional level shifting.

Current limiting and thermal shutdown features protect against output short circuits and bus contention that may cause excessive power dissipation. Receiver inputs feature a "fail-safe if open" design, ensuring a logic high R-output if A/B are floating.



IsoLoop® is a registered trademark of NVE Corporation.
*U.S. Patent number 5,831,426; 6,300,617 and others.

Absolute Maximum Ratings⁽⁷⁾

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|----------------------------------|--------------------|------|------|----------------|-------|-----------------|
| Storage Temperature | T_S | -55 | | 150 | °C | |
| Junction Temperature | T_J | -55 | | 150 | °C | |
| | | | | | | |
| Voltage Range at A or B Bus Pins | | -7 | | 12 | V | |
| Supply Voltage ⁽¹⁾ | V_{DD1}, V_{DD2} | -0.5 | | 7 | V | |
| Digital Input Voltage | | -0.5 | | $V_{DD} + 0.5$ | V | |
| Digital Output Voltage | | -0.5 | | $V_{DD} + 1$ | V | |
| ESD (all bus nodes) | | 15 | | | kV | HBM |

Recommended Operating Conditions

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|--|------------------------|------------|------|------------|-------|--|
| Supply Voltage | V_{DD1} V_{DD2} | 3.0 4.5 | | 5.5 5.5 | V | |
| Ambient Operating Temperature | T_A | -40 | | 85 | °C | |
| Junction Temperature | T_J | -40 | | 100 | °C | |
| High-Level Digital Input Voltage | V_{IH} | 2.4 3.0 | | V_{DD1} | V | $V_{DD1} = 3.3\text{ V}$ $V_{DD1} = 5.0\text{ V}$ |
| Low-Level Digital Input Voltage | V_{IL} | 0 | | 0.8 | V | |
| Differential Input Voltage ⁽²⁾ | V_{ID} | | | +12 / -7 | V | |
| High-Level Output Current (Driver) | I_{OH} | | | 60 | mA | |
| High-Level Digital Output Current (Receiver) | I_{OH} | | | 8 | mA | |
| Low-Level Output Current (Driver) | I_{OL} | -60 | | | mA | |
| Low-Level Digital Output Current (Receiver) | I_{OL} | -8 | | | mA | |
| Digital Input Signal Rise and Fall Times | t_{IR}, t_{IF} | DC Stable | | | | |

Safety and Approvals

VDE V 0884-11 / IEC 60747-17

V-Series (Reinforced Isolation; VDE File Number 5016933-4880-0002)

- Working Voltage (V_{IORM}): 1000 V_{RMS} (1415 V_{PK}) under VDE V 0884-10 reinforced isolation; pollution degree 2
- Working Voltage (V_{IORM}): 500 V_{RMS} (708 V_{PK}) under VDE V 0884-11 reinforced isolation; pollution degree 2
- Isolation voltage (V_{ISO}): 6000 V_{RMS}
- Surge immunity (V_{IOSM}): 12.8 kV $_{PK}$
- Surge rating: 8 kV
- Transient overvoltage (V_{IOTM}): 6000 V_{PK}
- Each part tested at 2387 V_{PK} for 1 second, 5 pC partial discharge limit
- Samples tested at 6000 V_{PK} for 60 sec.; then 2122 V_{PK} for 10 sec. with 5 pC partial discharge limit

VDE V 0884-11 / IEC 60747-17

Standard versions (Basic Isolation; VDE File Number 5016933-4880-0001)

- Isolation voltage (V_{ISO}): 2500 V_{RMS}
- Transient overvoltage (V_{IOTM}): 4000 V_{PK}
- Surge rating: 4000 V
- Each part tested at 1590 V_{PK} for 1 second, 5 pC partial discharge limit.
- Samples tested at 4000 V_{PK} for 60 sec.; then 1358 V_{PK} for 10 sec. with 5 pC partial discharge limit.
- Working Voltage (V_{IORM} ; pollution degree 2):

| Package | Part No. Suffix | Working Voltage |
|------------------------------|-----------------|-----------------|
| QSOP16 | -1 | 500 V_{RMS} |
| Narrow-body SOIC16 | -3 | 400 V_{RMS} |
| Wide-body SOIC16/ True 8™ | None | 500 V_{RMS} |

| Safety-Limiting Values | Symbol | Value | Units |
|--|--------|-------|-------|
| Safety rating ambient temperature | T_S | 180 | °C |
| Safety rating power (180 °C) | P_S | 270 | mW |
| Supply current safety rating (total of supplies) | I_S | 54 | mA |

UL 1577 (Component Recognition Program File Number E207481)

Standard isolation grade

2500 V rating; each part tested at 3000 V_{RMS} (4243 V_{PK}) for 1 second; each lot sample tested at 2500 V_{RMS} (3536 V_{PK}) for 1 minute.

V-Series isolation grade

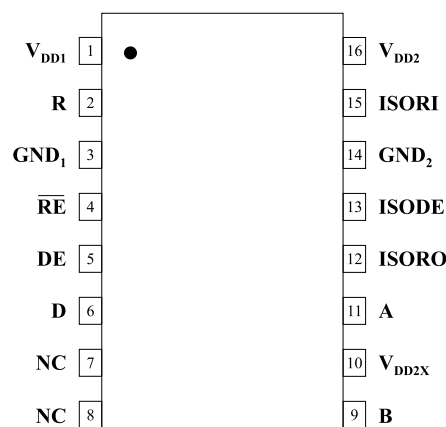
6 kV rating; each part tested at 7.2 kV $_{RMS}$ (10.2 kV $_{PK}$) for 1 second; each lot sample tested at 6 kV $_{RMS}$ (8485 V_{PK}) for 1 minute.

Soldering Profile

Per JEDEC J-STD-020C, MSL 1

IL3685-1 (QSOP Package) Pin Connections

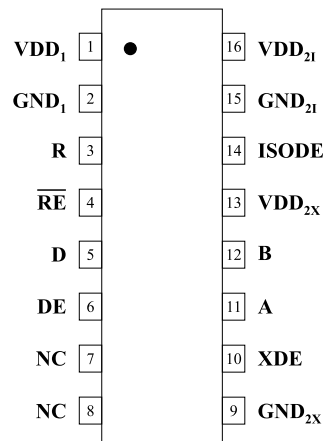
| | | |
|------|------------------------|---|
| 1 | V _{DD1} | Input power supply. |
| 2 | R | Output data from bus. |
| 3 | GND ₁ | Input power supply ground return. |
| 4 | $\overline{\text{RE}}$ | Read data enable (if $\overline{\text{RE}}$ is high, R= high impedance). |
| 5 | DE | Drive enable (HIGH if left unconnected). |
| 6 | D | Data input to bus. |
| 7, 8 | NC | No internal connection. |
| 9 | B | Inverting bus line. |
| 10 | V _{DD2X} | Output transceiver power supply (normally connected to pin 16). |
| 11 | A | Non-inverting bus line. |
| 12 | ISORO | Isolated R output (should be externally connected to pin 15; no other connection should be made). |
| 13 | ISODE | Isolated DE output. |
| 14 | GND ₂ | Output power supply ground return. |
| 15 | ISORI | Isolated R input (should be connected to pin 12; no other connection should be made). |
| 16 | V _{DD2I} | Output isolation power supply (normally connected to pin 10). |



IL3685-1

IL3685-3 (0.15" Narrow-Body SOIC) Pin Connections

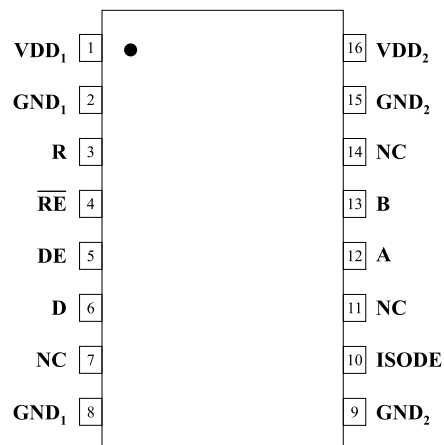
| | | |
|------|------------------------|---|
| 1 | V _{DD1} | Input power supply. |
| 2 | GND ₁ | Input power supply ground return. |
| 3 | R | Output data from bus. |
| 4 | $\overline{\text{RE}}$ | Read data enable (if $\overline{\text{RE}}$ is high, R= high impedance). |
| 5 | D | Data input to bus. |
| 6 | DE | Drive enable (HIGH if left unconnected). |
| 7, 8 | NC | No internal connection. |
| 9 | GND _{2X} | Output transceiver ground return. (normally connected to pin 15). |
| 10 | XDE | Transceiver Device Enable input enables the transceiver from the bus side, or is connected to ISODE to enable the transceiver from the controller-side DE input (this input should not be left unterminated). |
| 11 | A | Non-inverting bus line. |
| 12 | B | Inverting bus line. |
| 13 | V _{DD2X} | Output transceiver power supply (normally connected to pin 16). |
| 14 | ISODE | Isolated DE output (normally connected to pin 10). |
| 15 | GND _{2I} | Output isolation power supply ground return. (normally connected to pin 9). |
| 16 | V _{DD2I} | Output isolation power supply (normally connected to pin 13). |



IL3685-3

IL3685 (0.3" SOIC Wide-Body SOIC) Pin Connections

| | | |
|----|------------------|--|
| 1 | V _{DD1} | Input power supply. |
| 2 | GND ₁ | Input power supply ground return (pin 2 is internally connected to pin 8). |
| 3 | R | Output data from bus. |
| 4 | \overline{RE} | Read data enable (if \overline{RE} is high, R= high impedance). |
| 5 | DE | Drive enable (HIGH if left unconnected). |
| 6 | D | Data input to bus. |
| 7 | NC | No internal connection. |
| 8 | GND ₁ | Input power supply ground return (pin 8 is internally connected to pin 2). |
| 9 | GND ₂ | Output power supply ground return (pin 9 is internally connected to pin 15). |
| 10 | ISODE | Isolated DE output for use in PROFIBUS applications where the state of the isolated drive enable node needs to be monitored. |
| 11 | NC | No internal connection. |
| 12 | A | Non-inverting bus line. |
| 13 | B | Inverting bus line. |
| 14 | NC | No internal connection. |
| 15 | GND ₂ | Output power supply ground return (pin 15 is internally connected to pin 9). |
| 16 | V _{DD2} | Output power supply. |



IL3685

Driver Section

| Electrical Specifications (T_{min} to T_{max} and $V_{DD} = 4.5$ V to 5.5 V unless otherwise stated) | | | | | | |
|---|------------------|------|------|-----------|---------------|---|
| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
| Output voltage | V_O | | | V_{DD} | V | $I_O = 0$ |
| Differential Output Voltage ⁽²⁾ | $ V_{OD1} $ | | | V_{DD} | V | $I_O = 0$ |
| Differential Output Voltage ⁽²⁾ | $ V_{OD2} $ | 2.1 | 3 | 3.5 | V | $R_L = 54 \Omega$ |
| Differential Output Voltage ⁽²⁾ | V_{OD3} | 1.9 | | 3.5 | V | $-7 \text{ V} < V_{CM} < 12 \text{ V}$; $R_L = 60 \Omega$ |
| Change in Magnitude of Differential Output Voltage ⁽⁴⁾ | $\Delta V_{OD} $ | | | ± 0.2 | V | $R_L = 54 \Omega$ or 100Ω |
| Common Mode Output Voltage | V_{OC} | | | 3 | V | $R_L = 54 \Omega$ or 100Ω |
| Change in Magnitude of Common Mode Output Voltage ⁽⁴⁾ | $\Delta V_{OC} $ | | | ± 0.2 | V | $R_L = 54 \Omega$ or 100Ω |
| High Level Input Current | I_{IH} | | | 10 | μA | $V_I = 3.5 \text{ V}$ |
| Low Level Input Current | I_{IL} | | | -10 | μA | $V_I = 0.4 \text{ V}$ |
| Absolute Short-circuit Output Current | I_{OS} | | | 250 | mA | $-7 \text{ V} < V_O < 12 \text{ V}$ |

Receiver Section

| Electrical Specifications (T_{min} to T_{max} and $V_{DD} = 4.5$ V to 5.5 V unless otherwise stated) | | | | | | |
|---|--------------------------------|----------------|----------|---------|---------------|---|
| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
| Positive-going Input Threshold Voltage | V_{IT+} | | | 0.2 | V | $-7 \text{ V} < V_{CM} < 12 \text{ V}$ |
| Negative-going Input Threshold Voltage | V_{IT-} | -0.2 | | | V | $-7 \text{ V} < V_{CM} < 12 \text{ V}$ |
| Hysteresis Voltage ($V_{IT+} - V_{IT-}$) | V_{HYS} | | 28 | | mV | $V_{CM} = 0 \text{ V}$, $T = 25^\circ\text{C}$ |
| Differential Bus Input Capacitance | C_D | | 9 | 12 | pF | |
| High Level Digital Output Voltage | V_{OH} | $V_{DD} - 0.2$ | V_{DD} | | V | $V_{ID} = 200 \text{ mV}$ $I_{OH} = -20 \mu\text{A}$ |
| Low Level Digital Output Voltage | V_{OL} | | | 0.2 | V | $V_{ID} = -200 \text{ mV}$ $I_{OH} = 20 \mu\text{A}$ |
| High-impedance-state output current | I_{OZ} | | | ± 1 | μA | $V_O = 0.4$ to $(V_{DD2} - 0.5) \text{ V}$ |
| Line Input Current | I_I | | | 220 | μA | $V_I = 12 \text{ V}$ |
| | | | | -160 | μA | $V_I = -7 \text{ V}$ |
| Input Resistance | R_I | 54 | | | k Ω | |
| Bus-Side Supply Current | I_{DD2} | | 5 | 16 | mA | |
| Bus-Side Dynamic Supply Current | $\Delta I_{DD2}/\Delta f_{IN}$ | | 1 | | | $R_T = \infty$ |
| | | | 0.8 | | | $R_T = 60 \Omega$ |

Power Consumption

| T_{min} to T_{max} and $V_{DD2} = 5 \text{ V}$ unless otherwise stated | | | | | | |
|--|--------------------------------|------|--------|--------|---------|---|
| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
| Controller-Side Quiescent Current | I_{DD1} | | 3 4 | 4 6 | mA | $V_{DD1} = 3.3 \text{ V}$ $V_{DD1} = 5 \text{ V}$ $f_{IN} = 0 \text{ Hz}$ |
| Bus-Side Quiescent Supply Current | I_{DD2} | | 5 | 16 | mA | Outputs Enabled; $R_T = \infty$; $f_{IN} = 0 \text{ Hz}$; V_{DD2X} connected to V_{DD2I} if applicable |
| Controller-Side Dynamic Supply Current | I_{DD1} | | 0.22 | | mA/Mbps | $V_{DD1} = 3.3 \text{ V}$ |
| Bus-Side Dynamic Supply Current | $\Delta I_{DD2}/\Delta f_{IN}$ | | 1 | | | $R_T = \infty$ |
| | | | 0.8 | | | $R_T = 60 \Omega$ |

Switching Characteristics

| V_{DD1} = 5 V, V_{DD2} = 5 V | | | | | | |
|--|-------------------------------------|------|------|------|-------|--|
| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
| Data Rate | | 40 | | | Mbps | R _L = 54 Ω, C _L = 50 pF |
| Propagation Delay ⁽⁵⁾ | t _{PD} | | 20 | 30 | ns | V _O = -1.5 to 1.5 V, C _L = 15 pF |
| Pulse Skew ⁽⁶⁾ | t _{SK} (P) | | 1 | 5 | ns | V _O = -1.5 to 1.5 V, C _L = 15 pF |
| Skew Limit ⁽³⁾ | t _{SK} (LIM) | | 2 | 10 | ns | R _L = 54 Ω, C _L = 50 pF |
| Output Enable Time To High Level | t _{PZH} | | 15 | 30 | ns | C _L = 15 pF |
| Output Enable Time To Low Level | t _{PZL} | | 15 | 30 | ns | C _L = 15 pF |
| Output Disable Time From High Level | t _{PHZ} | | 15 | 30 | ns | C _L = 15 pF |
| Output Disable Time From Low Level | t _{PLZ} | | 15 | 30 | ns | C _L = 15 pF |
| Common Mode Transient Immunity (Output Logic High to Logic Low) | CM _H , CM _L | 30 | 50 | | kV/μs | V _{CM} = 1500 V _{DC} t _{TRANSIENT} = 25 ns |
| V_{DD1} = 3.3 V, V_{DD2} = 5 V | | | | | | |
| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
| Data Rate | | 40 | | | Mbps | R _L = 54 Ω, C _L = 50 pF |
| Propagation Delay ⁽⁵⁾ | t _{PD} | | 25 | 35 | ns | V _O = -1.5 to 1.5 V, C _L = 15 pF |
| Pulse Skew ⁽⁶⁾ | t _{SK} (P) | | 2 | 5 | ns | V _O = -1.5 to 1.5 V, C _L = 15 pF |
| Skew Limit ⁽³⁾ | t _{SK} (LIM) | | 4 | 10 | ns | R _L = 54 Ω, C _L = 50 pF |
| Output Enable Time To High Level | t _{PZH} | | 17 | 30 | ns | C _L = 15 pF |
| Output Enable Time To Low Level | t _{PZL} | | 17 | 30 | ns | C _L = 15 pF |
| Output Disable Time From High Level | t _{PHZ} | | 17 | 30 | ns | C _L = 15 pF |
| Output Disable Time From Low Level | t _{PLZ} | | 17 | 30 | ns | C _L = 15 pF |
| Common Mode Transient Immunity (Output Logic High to Logic Low) | CM _H , CM _L | 30 | 50 | | kV/μs | V _{CM} = 1500 V _{DC} t _{TRANSIENT} = 25 ns |

Magnetic Field Immunity⁽⁸⁾

| V _{DD1} = 5 V, V _{DD2} = 5 V | | | | | | |
|--|------------------|--|------|--|-----|----------------------|
| Power Frequency Magnetic Immunity | H _{PF} | | 3500 | | A/m | 50Hz/60Hz |
| Pulse Magnetic Field Immunity | H _{PM} | | 4500 | | A/m | t _p = 8μs |
| Damped Oscillatory Magnetic Field | H _{OSC} | | 4500 | | A/m | 0.1Hz – 1MHz |
| Cross-axis Immunity Multiplier ⁽⁹⁾ | K _X | | 2.5 | | | |
| V _{DD1} = 3.3 V, V _{DD2} = 5 V | | | | | | |
| Power Frequency Magnetic Immunity | H _{PF} | | 1500 | | A/m | 50Hz/60Hz |
| Pulse Magnetic Field Immunity | H _{PM} | | 2000 | | A/m | t _p = 8μs |
| Damped Oscillatory Magnetic Field | H _{OSC} | | 2000 | | A/m | 0.1Hz – 1MHz |
| Cross-axis Immunity Multiplier ⁽⁹⁾ | K _X | | 2.5 | | | |

Insulation Specifications

| Parameter | | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|--|-----------------------------------|-------------------|--------------------|-------------------|------|-------------------------------------|---|
| Creepage Distance (external) | IL3685-1E IL3685-3E IL3685E | | 3.2 4.0 8.03 | 8.3 | | mm | Per IEC 60601 |
| Total Barrier Thickness (internal) | | | 0.013 | 0.016 | | mm | |
| Barrier Resistance | | R _{IO} | | >10 ¹⁴ | | Ω | 500 V |
| Barrier Capacitance | | C _{IO} | | 7 | | pF | f = 1 MHz |
| Leakage Current | | | | 0.2 | | μA _{RMS} | 240 V _{RMS} , 60 Hz |
| Comparative Tracking Index | | CTI | ≥600 | | | V _{RMS} | Per IEC 60112 |
| High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life) | AC DC | V _{IO} | 1000 1500 | | | V _{RMS} V _{DC} | At maximum operating temperature |
| Surge Immunity ("V" Version) | | V _{IOSM} | 12.8 | | | kV _{PK} | Per IEC 61000-4-5 |
| Barrier Life | | | | 44000 | | Years | 100°C, 1000 V _{RMS} , 60% CL activation energy |

Thermal Characteristics

| Parameter | | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|--|---------------------------------|-----------------|------|-----------------|--------------------|-------|---------------------------------|
| Junction–Ambient Thermal Resistance | QSOP 0.15" SOIC 0.3" SOIC | θ _{JA} | | 100 82 67 | | °C/W | Double-sided PCB in free air |
| Junction–Case (Top) Thermal Resistance | QSOP 0.15" SOIC 0.3" SOIC | θ _{JC} | | 9 8 12 | | | |
| Junction–Ambient Thermal Resistance | 0.3" SOIC | θ _{JA} | | 46 | | | 2s2p PCB in free air per JESD51 |
| Junction–Case (Top) Thermal Resistance | | θ _{JC} | | 9 | | | |
| Power Dissipation | QSOP 0.15" SOIC 0.3" SOIC | P _D | | | 675 700 1500 | mW | |

Notes:

1. All voltages are with respect to network ground except differential I/O bus voltages.
2. Differential input/output voltage is measured at the noninverting terminal A with respect to the inverting terminal B.
3. Skew limit is the maximum propagation delay difference between any two devices at 25°C.
4. $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from one logic state to the other.
5. Includes 10 ns read enable time. Maximum propagation delay is 25 ns after read assertion.
6. Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel.
7. Absolute Maximum specifications mean the device will not be damaged if operated under these conditions. It does not guarantee performance.
8. The relevant test and measurement methods are given in the Electromagnetic Compatibility section.
9. External magnetic field immunity is improved by this factor if the field direction is “end-to-end” rather than to “pin-to-pin.”

Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

Pinout Differences Between Packages

The QSOP (IL3685-1E) and narrow-body (IL3685-3E) versions are designed for minimum board area in densely-populated PCAs. Both have pin sets that should be connected externally for normal operation, but that can be used for testing, trouble-shooting, or special purposes. The wide-body version (IL3685E) has redundant ground pins for layout flexibility.

The narrow-body version provides a separate isolated DE output (ISODE) and Transceiver Device Enable (XDE) input. ISODE follows the Device Enable input (DE). XDE can be used to enable and disable the transceiver from the bus side, or connected to ISODE to enable and disable the transceiver from the DE controller-side input. The QSOP and narrow-body versions also provide separate bus-side power supply pins— V_{DD2X} for the transceiver module and V_{DD2I} for the isolation module. These should be externally connected for normal operation, but can be used separately for testing or troubleshooting. The QSOP version also has an “ISORI” input that can be used to test the controller-side “R” from the bus side. ISORI should be connected externally to “ISORO” for normal operation. ISORI and ISORO can be used for testing.

The wide-body version has internal connections between the isolated DE output and the Transceiver Device Enable input, and well as between the two bus-side power supplies.

Power Supply Decoupling

V_{DD1} and V_{DD2} should be bypassed with 0.1 μ F typical (47 nF minimum) capacitors as close as possible to the V_{DD} pins.

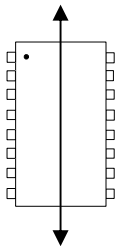
Maintaining Creepage

Creepage distances are often critical in isolated circuits. In addition to meeting JEDEC standards, NVE isolator packages have unique creepage specifications. Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance. Package drawings and recommended pad layouts are included in this datasheet.

Electromagnetic Compatibility

IL3685-Series Transceivers are fully compliant with IEC 61000-6-1 and IEC 61000-6-2 standards for immunity, and IEC 61000-6-3, IEC 61000-6-4, CISPR, and FCC Class A standards for emissions.

The IsoLoop Isolator's Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EM immunity. Immunity to external magnetic fields is even higher if the field direction is “end-to-end” (rather than to “pin-to-pin”) as shown at right.



Application Information

Figures 1a, 1b, and 1c show typical connections to a bus and microcontroller for the three package versions, including external connections required for normal operation. Typical termination resistors, fail-safe resistors, and power supply decoupling capacitors are also included:

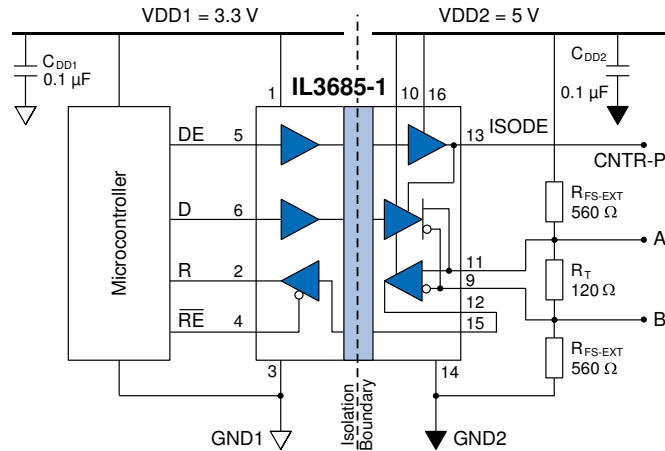


Figure 1a. Typical QSOP transceiver connections.

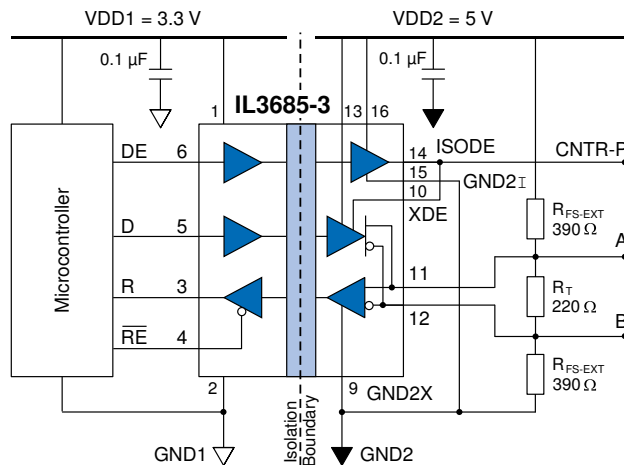


Figure 1b. Typical narrow-body transceiver connections.

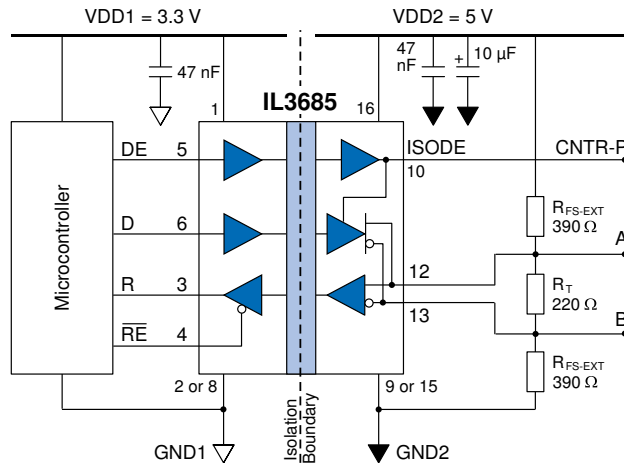


Figure 1c. Typical wide-body transceiver connections.

Transceiver Operation

The transceiver block diagram is shown below:

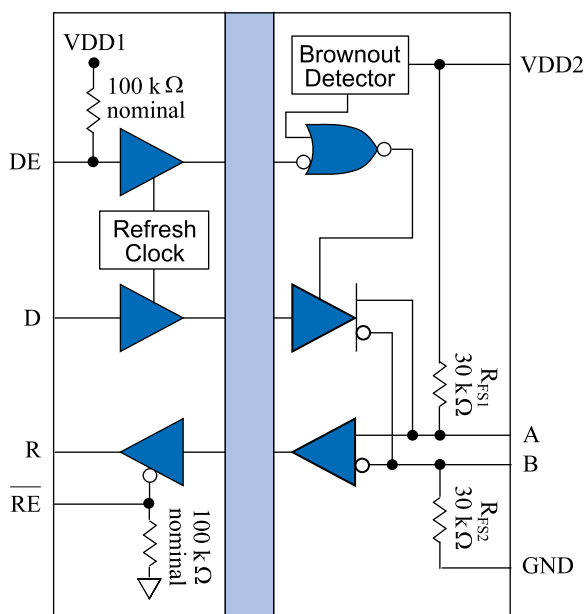


Figure 2. Detailed transceiver block diagram.

Receiver Features

The receiver output “R” has tri-state capability via the active low \overline{RE} input.

Driver Features

The driver features low propagation delay skew to maximize bit width and minimize EMI. Drivers have tri-state capability via the active-high DE input.

Deterministic Power Up and Brownout Detection

IL3685 parts have circuitry to disable the bus driver until the driver-side voltage (VDD2) reaches approximately 3.3 volts on power-up. The transceiver is disabled when the voltage drops below approximately 3.1 volts on power-down. This brownout circuitry ensures the transceiver does not “crash” the bus on power up, power down, or brownout, and eliminates the need for external power supply monitors. In addition, a patented refresh circuit maintains the correct transceiver output state with respect to data input (DC correctness). The refresh circuit ensures the bus outputs will follow the Function Table shown on Page 1 after power up.

Hot Plug Operation

Deterministic power-up allows IL3685 nodes to “hot plug” into the bus, since the bus driver will be in a high-impedance state until the bus supply is enough for the bus driver to operate.

Unpowered Nodes

Unpowered nodes (i.e., either no VDD1 or VDD2 power) result in high impedances on the “A” and “B” bus lines, so the unpowered node will not disturb bus operation.

Internal Fail-Safe Biasing Resistors

Internal “fail-safe biasing” forces a logic high state on “R” with an open-circuit between the bus “A” and “B” lines, or when no drivers are active on the bus.

Rigorous PROFIBUS Compatibility

Unlike most other transceivers, IL3685E transceivers meet stringent PROFIBUS standards for maximum differential output voltage as other PROFIBUS requirements.

Thermal Shutdown

The bus driver is disabled when the driver die temperature exceeds approximately 150 °C, and re-enabled when the die temperature drops below approximately 135 °C. The receiver section continues to operate during thermal shutdown.

Termination and Fail-Safe Biasing

Internal Biasing Resistors

“Fail-safe biasing” forces a logic high state on “R” in response to an open-circuit condition between the bus “A” and “B” lines, or when no drivers are active on the bus. IL3000-Series Isolated Transceivers include internal pull-up and pull-down resistors of approximately 30 k Ω in the receiver section (RFS-INT in Figure 3 below):

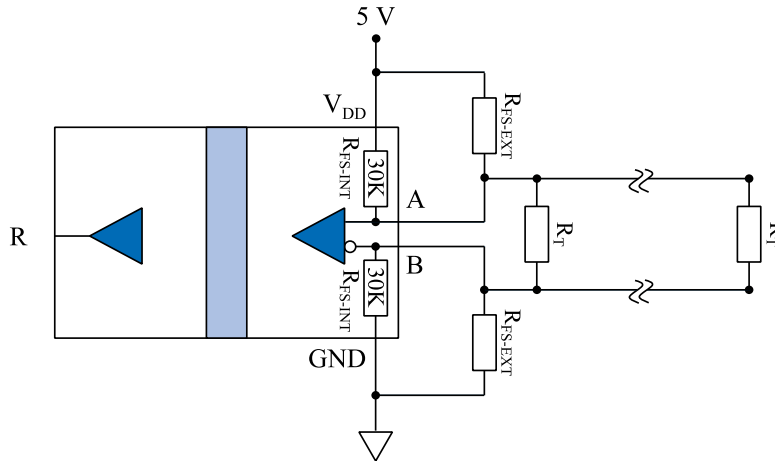


Figure 3. Termination and internal and external fail-safe biasing resistors.

These internal resistors ensure fail-safe operation if there are no termination resistors and up to four RS-485 worst-case Unit Loads of 12 k Ω .

Termination Resistors

Termination resistors should be on both ends of the network to minimize reflections. Values should be selected to match cable impedance; 220 Ω resistors are typical for PROFIBUS.

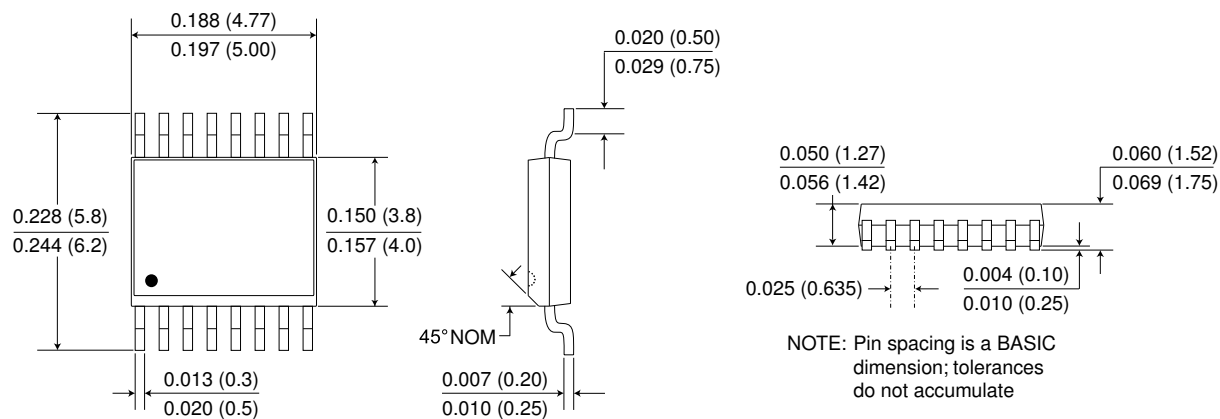
External Fail-Safe Biasing Resistors

Termination resistors bring the differential voltage across the conductor pair close to zero with no active drivers. In this case, the idle bus is indeterminate and susceptible to noise. External fail-safe biasing resistors (labeled RFS-EXT in Figure 3) at one end of the bus ensure fail-safe operation with a terminated bus. Biasing should provide at least 200 mV across the conductor pair to meet the RS-485 input sensitivity specification. Fail-safe resistors of 390 Ω are common for PROFIBUS. They should be on only one node of the network. Using the same value for pull-up and pull-down biasing resistors maintains balance for positive- and negative going transitions.

Package Drawings

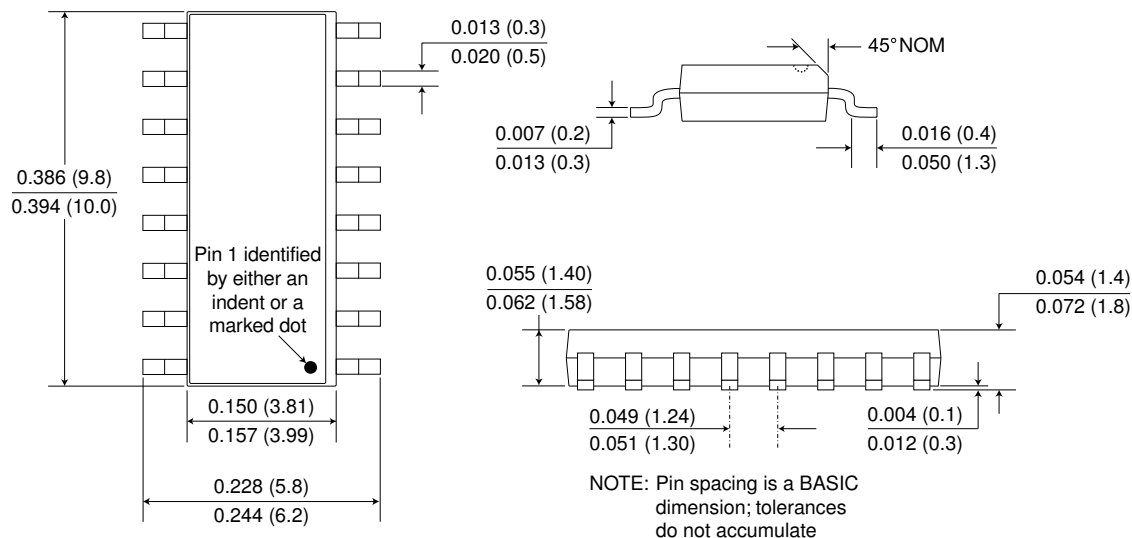
Ultraminiature 16-pin QSOP Package (-1 suffix)

Dimensions in inches (mm); scale = approx. 5X



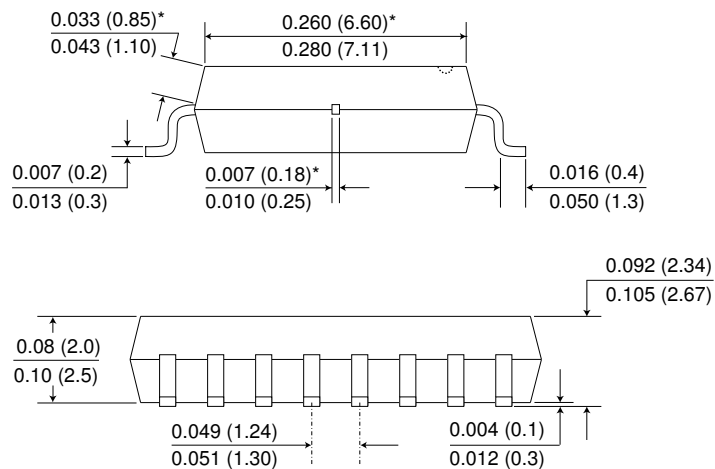
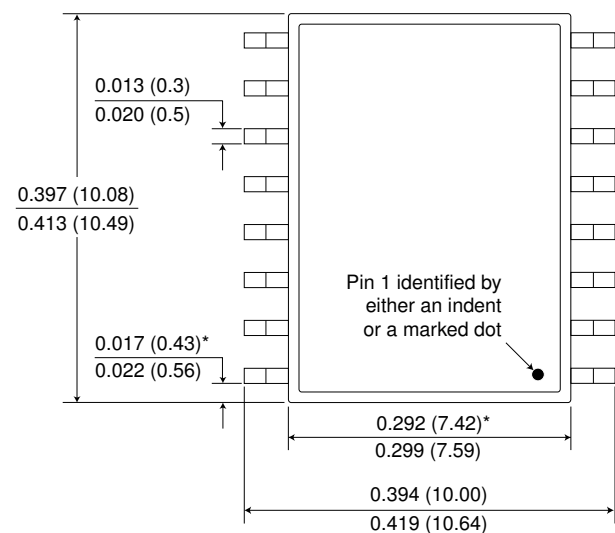
0.15" 16-pin Narrow-Body SOIC Package (-3 suffix)

Dimensions in inches (mm); scale = approx. 5X



0.3" 16-pin Wide-Body SOIC Package (no suffix)

Dimensions in inches (mm); scale = approx. 5X



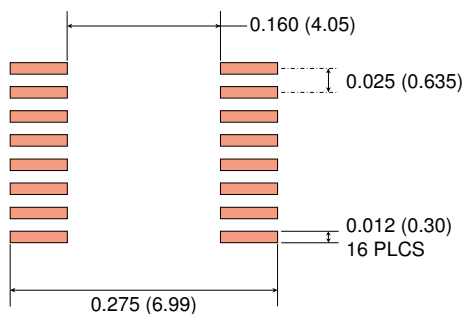
NOTE: Pin spacing is a BASIC dimension; tolerances do not accumulate

*Specified for True 8™ package to guarantee 8 mm creepage per IEC 60601.

Recommended Pad Layouts

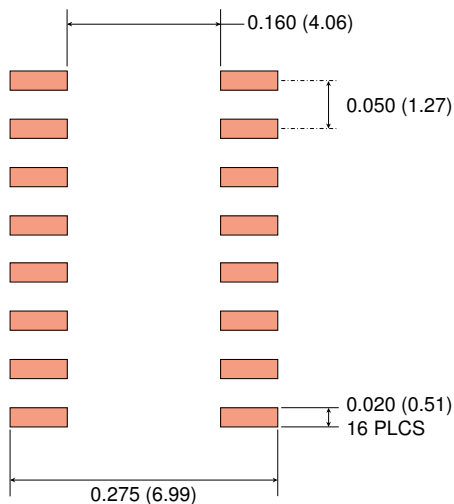
4 mm x 5 mm 16-pin QSOP Pad Layout

Dimensions in inches (mm); scale = approx. 5X



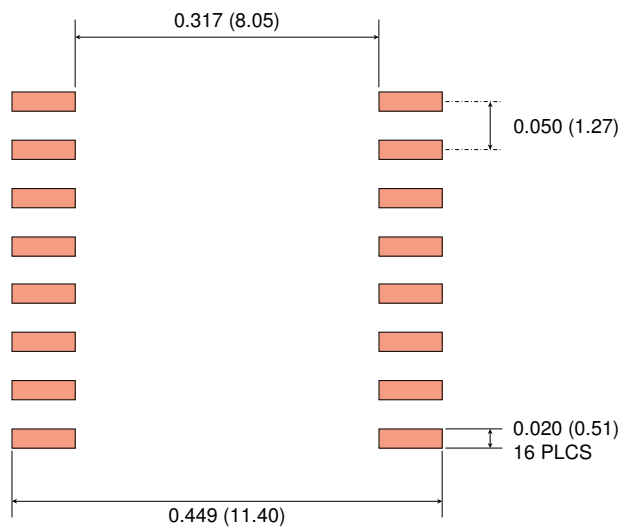
0.15" Narrow-Body 16-pin SOIC Pad Layout

Dimensions in inches (mm); scale = approx. 5X



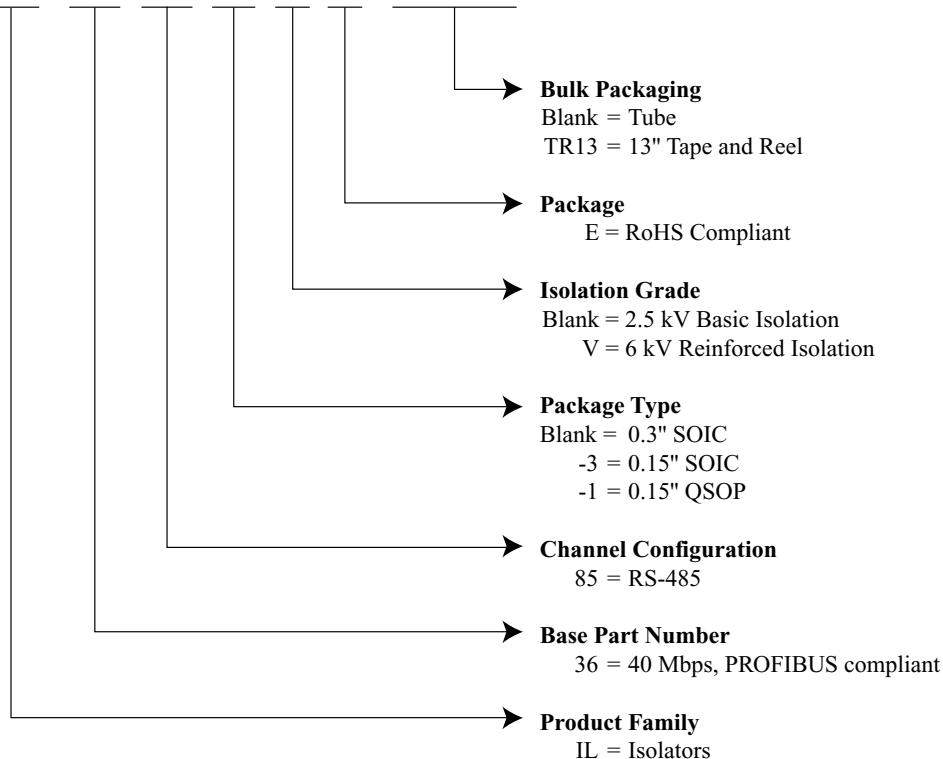
0.3" 16-pin Wide-Body SOIC Pad Layout

Dimensions in inches (mm); scale = approx. 5X



Ordering Information and Valid Part Numbers

IL 36 85 -3 V E TR13



Valid Part Numbers

IL3685E
IL3685E TR13
IL3685-3E
IL3685-3E TR13
IL3685-1E TR7
IL3685-1E TR13

IL3685VE
IL3685VE TR13

RoHS
COMPLIANT

Revision History

ISB-DS-001-IL3685-Y May 2020

Changes

- Upgrade from VDE V 0884-10 to VDE V 0884-11 / IEC 60747-17 (p. 3).
- Separate power consumption specifications section; added dynamic power consumption (p. 6).
- Revised thermal specifications (p. 8).
- More details on power up, hot plug, brownout detection, and unpowered nodes (p. 12).
- Updated EMC standards.

ISB-DS-001-IL3685-X

Change

- Improved thermal specifications based on new test data (p. 2).

ISB-DS-001-IL3685-W

Change

- Dropped 10 μ F tantalum capacitor recommendation (p. 8).

ISB-DS-001-IL3685-V

Change

- Added IL3685VE to the list of available parts (p. 16).

ISB-DS-001-IL3685-U

Changes

- Refined thermal resistance specifications based on additional test data (p. 2).
- Added worst-case operating conditions to max. ambient operating temperature spec.
- Deleted minimum magnetic field immunity specifications (p. 8) since it is not 100% tested.

ISB-DS-001-IL3685-T

Changes

- Added QSOP version (IL3685-1E).
- VDE certification and UL approval for V-Series version (6 kV reinforced isolation).

ISB-DS-001-IL3685-S

Changes

- Eliminated inconsistent Driver Section output current specification.
- Improved Receiver Section Line Input Current and Input Resistance specifications.

ISB-DS-001-IL3685-R

Changes

- Updated VDE certification standard to VDE V 0884-10.
- Upgraded “V” Version Surge Immunity specification to 12.8 kV.
- Upgraded “V” Version VDE 0884-10 rating to reinforced insulation.

ISB-DS-001-IL3685-Q

Changes

- Increased V-Series isolation voltage to 6 kV_{RMS}.
- Increased typ. Total Barrier Thickness specification to 0.016 mm.
- Increased CTI min. specification to ≥ 600 V_{RMS}.

ISB-DS-001-IL3685-P

Changes

- Increase V-Series surge voltage specification to 10 kV.
- Upgraded V-Series safety and approval from IEC 60747-5-5 (VDE 0884) to VDE 0884-10.

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ISB-DS-001-IL3685-Y

May 2020