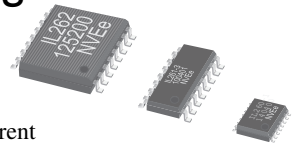
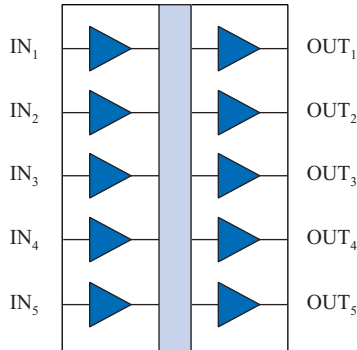


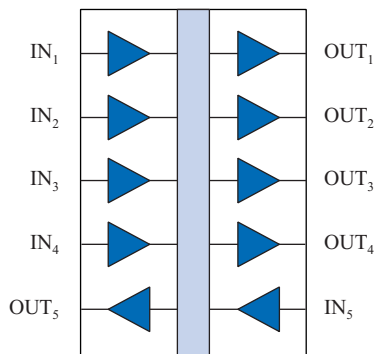
## High Speed Five-Channel Digital Isolators



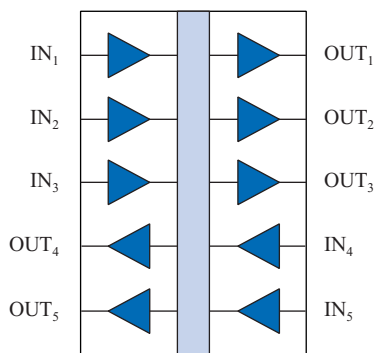
### Functional Diagrams



**IL260**



**IL261**



**IL262**

### Features

- High Speed: 110 Mbps
- 1.2 mA/channel typical quiescent current
- Very high isolation: 6 kV<sub>RMS</sub> Reinforced Isolation (V-Series)
- 50 kV/μs typ.; 30 kV/μs min. common mode transient immunity
- No carrier or clock for low EMI emissions and susceptibility
- -40 °C to 85 °C operating temperature
- 44000 year barrier life
- Excellent magnetic immunity
- 2 ns typical pulse width distortion
- 100 ps pulse jitter
- 4 ns typical propagation delay skew
- 10 ns typical propagation delay
- 2 ns channel-to-channel skew
- VDE certified; UL 1577 recognized
- 0.15" and True 8™ mm 16-pin SOIC; 16-pin QSOP packages

### Applications

- ADCs and DACs
- Multiplexed data transmission
- Board-to-board communication
- Peripheral interfaces
- Equipment covered under IEC 61010-1 Edition 3
- 5 kV<sub>RMS</sub> rated IEC 60601-1 medical applications

### Description

NVE's IL260-Series five-channel high-speed digital isolators are CMOS devices manufactured with NVE's patented\* IsoLoop<sup>®</sup> spintronic Giant Magnetoresistive (GMR) technology.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

All transmit and receive channels operate at 110 Mbps over the full temperature and supply voltage range. The symmetric magnetic coupling barrier provides a typical propagation delay of only 10 ns and a pulse width distortion of 2 ns, achieving the best specifications of any isolator. The unique fifth channel can be used to distribute isolated clocks or handshake signals to multiple delta-sigma A/D converters. High channel density makes these devices ideal for isolating ADCs and DACs, parallel buses and peripheral interfaces.

Typical transient immunity of 50 kV/μs is unsurpassed. Performance is specified over the temperature range of -40 °C to +85 °C without derating.

The five-channel devices provide the highest channel density available. Parts are available in ultraminiature 16-pin QSOPs, as well as 0.15" and 0.3"-wide SOIC packages.

V-Series versions offer extremely high isolation voltage of 6 kV<sub>RMS</sub>, and true 8 mm creepage.

## Absolute Maximum Ratings<sup>(1)</sup>

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Storage Temperature	$T_S$	-55		150	°C	
Junction Temperature	$T_J$	-55		150	°C	
Ambient Operating Temperature	$T_A$	-40		85	°C	
Supply Voltage	$V_{DD1}, V_{DD2}$	-0.5		7	V	
Input Voltage	$V_I$	-0.5		$V_{DD} + 0.5$	V	
Output Voltage	$V_O$	-0.5		$V_{DD} + 0.5$	V	
Output Current Drive	$I_O$	-10		10	mA	
Lead Solder Temperature				260	°C	10 sec.
ESD			2		kV	HBM

## Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Ambient Operating Temperature	$T_A$	-40		85	°C	
Junction Temperature	$T_J$	-40		110	°C	
Supply Voltage	$V_{DD1}, V_{DD2}$	2.5		5.5	V	
Logic High Input Voltage	$V_{IH}$	2.4		$V_{DD}$	V	
Logic Low Input Voltage	$V_{IL}$	0		0.8	V	
Input Signal Rise and Fall Times	$t_{IR}, t_{IF}$			1	μs	

## Safety and Approvals

### VDE V 0884-10 (VDE V 0884-11 pending)

V-Series (Reinforced Isolation; VDE File Number 5016933-4880-0002)

- Working Voltage ( $V_{IORM}$ ) 1000  $V_{RMS}$  (1415  $V_{PK}$ ); reinforced insulation; pollution degree 2
- Isolation voltage ( $V_{ISO}$ ) 6000  $V_{RMS}$
- Surge immunity ( $V_{IOSM}$ ) 12.8 kV $_{PK}$
- Surge rating 8 kV
- Transient overvoltage ( $V_{IOTM}$ ) 6000  $V_{PK}$
- Each part tested at 2387  $V_{PK}$  for 1 second, 5 pC partial discharge limit
- Samples tested at 6000  $V_{PK}$  for 60 sec.; then 2122  $V_{PK}$  for 10 sec. with 5 pC partial discharge limit

Standard versions (Basic Isolation; VDE File Number 5016933-4880-0001)

- Working Voltage ( $V_{IORM}$ ) 600  $V_{RMS}$  (848  $V_{PK}$ ); basic insulation; pollution degree 2
- Isolation voltage ( $V_{ISO}$ ) 2500  $V_{RMS}$
- Transient overvoltage ( $V_{IOTM}$ ) 4000  $V_{PK}$
- Surge rating 4000 V
- Each part tested at 1590  $V_{PK}$  for 1 second, 5 pC partial discharge limit
- Samples tested at 4000  $V_{PK}$  for 60 sec.; then 1358  $V_{PK}$  for 10 sec. with 5 pC partial discharge limit

Safety-Limiting Values	Symbol	Value	Units
Safety rating ambient temperature	$T_S$	180	°C
Safety rating power (180°C)	$P_S$	270	mW
Supply current safety rating (total of supplies)	$I_S$	54	mA

### IEC 61010-1 (Edition 2; TUV Certificate Numbers N1502812; N1502812-101)

Reinforced Insulation; Pollution Degree II; Material Group III

Part No. Suffix	Package	Working Voltage
-1	QSOP	300 $V_{RMS}$
-3	0.15" SOIC	300 $V_{RMS}$
None	0.3" SOIC (standard)	300 $V_{RMS}$
V	0.3" SOIC (high isolation voltage)	1000 $V_{RMS}$

### UL 1577 (Component Recognition Program File Number E207481)

V-Series isolation grade

6 kV rating; tested at 7.2 kV $_{RMS}$  (10.2 kV $_{PK}$ ) for 1 second; each lot sample tested at 6 kV $_{RMS}$  (8485  $V_{PK}$ ) for 1 minute

Standard isolation grade

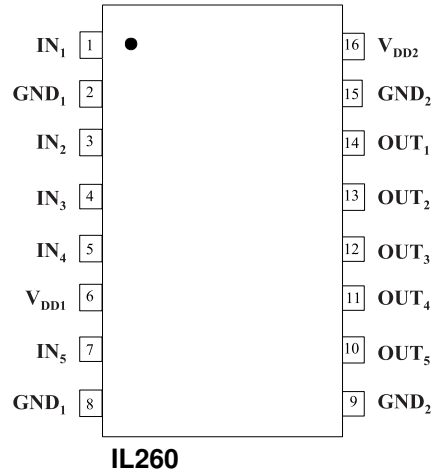
Each part tested at 3000  $V_{RMS}$  (4243  $V_{PK}$ ) for 1 second; each lot sample tested at 2500  $V_{RMS}$  (3536  $V_{PK}$ ) for 1 minute

## Soldering Profile

Per JEDEC J-STD-020C, MSL 1

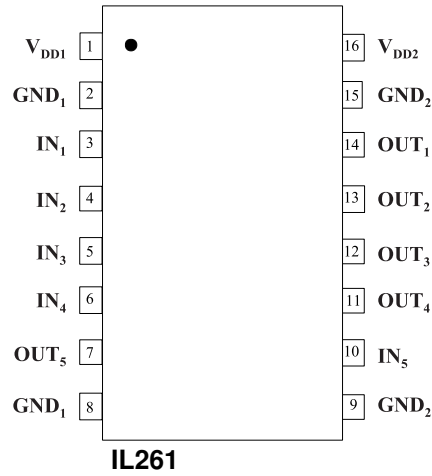
## IL260 Pin Connections

1	IN <sub>1</sub>	Input 1
2	GND <sub>1</sub>	Ground*
3	IN <sub>2</sub>	Input 2
4	IN <sub>3</sub>	Input 3
5	IN <sub>4</sub>	Input 4
6	V <sub>DD1</sub>	Supply Voltage 1
7	IN <sub>5</sub>	Input 5
8	GND <sub>1</sub>	Ground*
9	GND <sub>2</sub>	Ground*
10	OUT <sub>5</sub>	Output 5
11	OUT <sub>4</sub>	Output 4
12	OUT <sub>3</sub>	Output 3
13	OUT <sub>2</sub>	Output 2
14	OUT <sub>1</sub>	Output 1
15	GND <sub>2</sub>	Ground*
16	V <sub>DD2</sub>	Supply Voltage 2



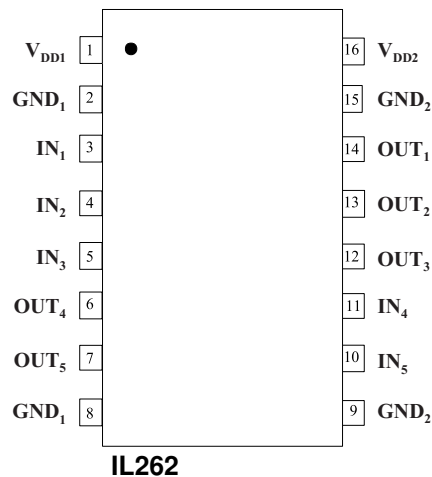
## IL261 Pin Connections

1	V <sub>DD1</sub>	Supply Voltage 1
2	GND <sub>1</sub>	Ground*
3	IN <sub>1</sub>	Input 1
4	IN <sub>2</sub>	Input 2
5	IN <sub>3</sub>	Input 3
6	IN <sub>4</sub>	Input 4
7	OUT <sub>5</sub>	Output 5
8	GND <sub>1</sub>	Ground*
9	GND <sub>2</sub>	Ground*
10	IN <sub>5</sub>	Input 5
11	OUT <sub>4</sub>	Output 4
12	OUT <sub>3</sub>	Output 3
13	OUT <sub>2</sub>	Output 2
14	OUT <sub>1</sub>	Output 1
15	GND <sub>2</sub>	Ground*
16	V <sub>DD2</sub>	Supply Voltage 2



## IL262 Pin Connections

1	V <sub>DD1</sub>	Supply Voltage 1
2	GND <sub>1</sub>	Ground*
3	IN <sub>1</sub>	Input 1
4	IN <sub>2</sub>	Input 2
5	IN <sub>3</sub>	Input 3
6	OUT <sub>4</sub>	Output 4
7	OUT <sub>5</sub>	Output 5
8	GND <sub>1</sub>	Ground*
9	GND <sub>2</sub>	Ground*
10	IN <sub>5</sub>	Input 5
11	IN <sub>4</sub>	Input 4
12	OUT <sub>3</sub>	Output 3
13	OUT <sub>2</sub>	Output 2
14	OUT <sub>1</sub>	Output 1
15	GND <sub>2</sub>	Ground*
16	V <sub>DD2</sub>	Supply Voltage 2



\*NOTE: Pins 2 and 8 are internally connected, as are pins 9 and 15.

3.3 Volt Electrical Specifications (T <sub>min</sub> to T <sub>max</sub> )							
Parameters		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Quiescent Current	IL260	I <sub>DD1</sub>		300	400	μA	
	IL261			1.2	1.75	mA	
	IL262			2.4	3.5	mA	
Output Quiescent Current	IL260	I <sub>DD2</sub>		6	8.75	mA	
	IL261			4.8	7	mA	
	IL262			3.6	5.25	mA	
Logic Input Current		I <sub>i</sub>	-10		10	μA	
Logic High Output Voltage		V <sub>OH</sub>	0.8 x V <sub>DD</sub>	V <sub>DD</sub> -0.1	V <sub>DD</sub>	V	I <sub>O</sub> = -20 μA, V <sub>i</sub> =V <sub>IH</sub>
				0.9 x V <sub>DD</sub>			I <sub>O</sub> = -4 mA, V <sub>i</sub> =V <sub>IH</sub>
Logic Low Output Voltage		V <sub>OL</sub>		0	0.1	V	I <sub>O</sub> = 20 μA, V <sub>i</sub> =V <sub>IL</sub>
				0.5	0.8		I <sub>O</sub> = 4 mA, V <sub>i</sub> =V <sub>IL</sub>

Switching Specifications (2.5 V < V <sub>DD</sub> < 3.6 V)							
Maximum Data Rate			100	110		Mbps	C <sub>L</sub> = 15 pF
Minimum Pulse Width <sup>(7)</sup>		PW	10			ns	50% Points, V <sub>O</sub>
Propagation Delay Input to Output (High to Low)		t <sub>PHL</sub>		12	18	ns	C <sub>L</sub> = 15 pF
Propagation Delay Input to Output (Low to High)		t <sub>PLH</sub>		12	18	ns	C <sub>L</sub> = 15 pF
Pulse Width Distortion  t <sub>PHL</sub> -t <sub>PLH</sub>   <sup>(2)</sup>		PWD		2	3	ns	C <sub>L</sub> = 15 pF
Propagation Delay Skew <sup>(3)</sup>		t <sub>PSK</sub>		4	6	ns	C <sub>L</sub> = 15 pF
Output Rise Time (10%-90%)		t <sub>R</sub>		2	4	ns	C <sub>L</sub> = 15 pF
Output Fall Time (10%-90%)		t <sub>F</sub>		2	4	ns	C <sub>L</sub> = 15 pF
Common Mode Transient Immunity (Output Logic High to Logic Low) <sup>(4)</sup>		CM <sub>H</sub>  ,  CM <sub>L</sub>	30	50		kV/μs	V <sub>CM</sub> = 1500 V <sub>DC</sub> t <sub>TRANSIENT</sub> = 25 ns
Channel-to-Channel Skew				2	3	ns	C <sub>L</sub> = 15 pF
Dynamic Power Consumption <sup>(6)</sup>				140	240	μA/Mbps	per channel

Magnetic Field Immunity <sup>(8)</sup> (V <sub>DD2</sub> = 3 V, 3 V < V <sub>DD1</sub> < 5.5 V)							
Power Frequency Magnetic Immunity		H <sub>PF</sub>		1500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity		H <sub>PM</sub>		2000		A/m	t <sub>p</sub> = 8μs
Damped Oscillatory Magnetic Field		H <sub>OSC</sub>		2000		A/m	0.1Hz - 1MHz
Cross-axis Immunity Multiplier <sup>(9)</sup>		K <sub>X</sub>		2.5			

5 Volt Electrical Specifications (T <sub>min</sub> to T <sub>max</sub> )							
Parameters		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Quiescent Current	IL260	I <sub>DD1</sub>		350	500	μA	
	IL261			1.8	2.5	mA	
	IL262			3.6	5	mA	
Output Quiescent Current	IL260	I <sub>DD2</sub>		9	12.5	mA	
	IL261			7.2	10	mA	
	IL262			5.4	7.5	mA	
Logic Input Current		I <sub>i</sub>	-10		10	μA	
Logic High Output Voltage		V <sub>OH</sub>	V <sub>DD</sub> -0.1	V <sub>DD</sub>		V	I <sub>O</sub> = -20 μA, V <sub>i</sub> = V <sub>IH</sub>
			0.8 x V <sub>DD</sub>	0.9 x V <sub>DD</sub>			I <sub>O</sub> = -4 mA, V <sub>i</sub> = V <sub>IH</sub>
Logic Low Output Voltage		V <sub>OL</sub>		0	0.1	V	I <sub>O</sub> = 20 μA, V <sub>i</sub> = V <sub>IL</sub>
				0.5	0.8		I <sub>O</sub> = 4 mA, V <sub>i</sub> = V <sub>IL</sub>

Switching Specifications (V <sub>DD</sub> = 5 V)							
Maximum Data Rate			100	110		Mbps	C <sub>L</sub> = 15 pF
Minimum Pulse Width <sup>(7)</sup>		PW	10			ns	50% Points, V <sub>O</sub>
Propagation Delay Input to Output (High to Low)		t <sub>PHL</sub>		10	15	ns	C <sub>L</sub> = 15 pF
Propagation Delay Input to Output (Low to High)		t <sub>PLH</sub>		10	15	ns	C <sub>L</sub> = 15 pF
Pulse Width Distortion  t <sub>PHL</sub> - t <sub>PLH</sub>   <sup>(2)</sup>		PWD		2	3	ns	C <sub>L</sub> = 15 pF
Pulse Jitter <sup>(10)</sup>		t <sub>J</sub>		100		ps	C <sub>L</sub> = 15 pF
Propagation Delay Skew <sup>(3)</sup>		t <sub>PSK</sub>		4	6	ns	C <sub>L</sub> = 15 pF
Output Rise Time (10%-90%)		t <sub>R</sub>		1	3	ns	C <sub>L</sub> = 15 pF
Output Fall Time (10%-90%)		t <sub>F</sub>		1	3	ns	C <sub>L</sub> = 15 pF
Common Mode Transient Immunity (Output Logic High to Logic Low) <sup>(4)</sup>		CM <sub>H</sub>  ,  CM <sub>L</sub>	30	50		kV/μs	V <sub>CM</sub> = 1500 V <sub>DC</sub> t <sub>TRANSIENT</sub> = 25 ns
Channel-to-Channel Skew				2	3	ns	C <sub>L</sub> = 15 pF
Dynamic Power Consumption <sup>(6)</sup>				200	340	μA/Mbps	per channel

Magnetic Field Immunity <sup>(8)</sup> (V <sub>DD2</sub> = 5 V, 3 V < V <sub>DD1</sub> < 5.5V)							
Power Frequency Magnetic Immunity		H <sub>PF</sub>		3500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity		H <sub>PM</sub>		4500		A/m	t <sub>p</sub> = 8μs
Damped Oscillatory Magnetic Field		H <sub>OSC</sub>		4500		A/m	0.1Hz - 1MHz
Cross-axis Immunity Multiplier <sup>(9)</sup>		K <sub>X</sub>		2.5			

Insulation Specifications							
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	
Creepage Distance (external)	QSOP	4.03			mm	Per IEC 60601	
	0.15" SOIC	4.03					
	0.3" SOIC	8.03	8.3				
Total Barrier Thickness (internal)		0.012	0.016		mm		
Leakage Current <sup>(5)</sup>			0.2		$\mu\text{A}_{\text{RMS}}$	240 V <sub>RMS</sub>	
Barrier Resistance <sup>(5)</sup>	R <sub>IO</sub>		>10 <sup>14</sup>		$\Omega$	500 V	
Barrier Capacitance <sup>(5)</sup>	C <sub>IO</sub>		5		pF	f = 1 MHz	
Comparative Tracking Index	CTI	≥600			V <sub>RMS</sub>	Per IEC 60112	
High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life)	AC	V <sub>IO</sub>	1000		V <sub>RMS</sub>	At maximum operating temperature	
	DC		1500		V <sub>DC</sub>		
Surge Immunity ("V" Versions)	V <sub>IOSM</sub>	12.8			kV <sub>PK</sub>	Per IEC 61000-4-5	
Barrier Life			44000		Years	100°C, 1000 V <sub>RMS</sub> , 60% CL activation energy	

Thermal Characteristics							
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	
Junction–Ambient Thermal Resistance	QSOP	$\theta_{JA}$	100			Double-sided PCB in free air	
	0.15" SOIC16		82				
	0.3" SOIC16		67				
Junction–Case (Top) Thermal Resistance	QSOP	$\theta_{JC}$	9		°C/W	2s2p PCB in free air per JESD51	
	0.15" SOIC16		8				
	0.3" SOIC16		12				
Junction–Ambient Thermal Resistance	0.3" SOIC	$\theta_{JA}$	46				
Junction–Case (Top) Thermal Resistance		$\theta_{JC}$	9				
Power Dissipation	QSOP 0.15" SOIC16 0.3" SOIC16	P <sub>D</sub>		675 675 1500	mW		

### Notes:

1. Absolute maximum means the device will not be damaged if operated under these conditions. It does not guarantee performance.
2. PWD is defined as  $t_{\text{PHL}} - t_{\text{PLH}}$ . %PWD is equal to PWD divided by pulse width.
3.  $t_{\text{PSK}}$  is the magnitude of the worst-case difference in  $t_{\text{PHL}}$  and/or  $t_{\text{PLH}}$  between devices at 25°C.
4.  $\text{CM}_H$  is the maximum common mode voltage slew rate that can be sustained while maintaining  $V_o > 0.8 V_{\text{DD2}}$ .  $\text{CM}_L$  is the maximum common mode input voltage that can be sustained while maintaining  $V_o < 0.8 V$ . The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
5. Device is considered a two terminal device: pins 1–8 shorted and pins 9–16 shorted.
6. Dynamic power consumption numbers are calculated per channel and are supplied by the channel's input side power supply.
7. Minimum pulse width is the minimum value at which specified PWD is guaranteed.
8. The relevant test and measurement methods are given in the Electromagnetic Compatibility section on p. 8.
9. External magnetic field immunity is improved by this factor if the field direction is "end-to-end" rather than to "pin-to-pin" (see diagram on p. 8).
10. 66,535-bit pseudo-random binary signal (PRBS) NRZ bit pattern with no more than five consecutive 1s or 0s; 800 ps transition time.

**Application Information**

**Electrostatic Discharge Sensitivity**

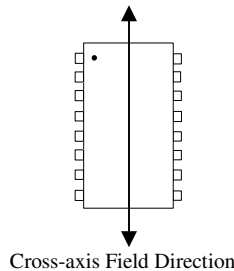
This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

**Electromagnetic Compatibility**

IsoLoop Isolators have the lowest EMC footprint of any isolation technology. There are no internal clocks or carriers. IsoLoop Isolators' Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards.

These isolators are fully compliant with IEC 61000-6-1 and IEC 61000-6-2 standards for immunity, and IEC 61000-6-3, IEC 61000-6-4, CISPR, and FCC Class A standards for emissions.

Immunity to external magnetic fields is even higher if the field direction is "end-to-end" rather than to "pin-to-pin" as shown in the diagram below:



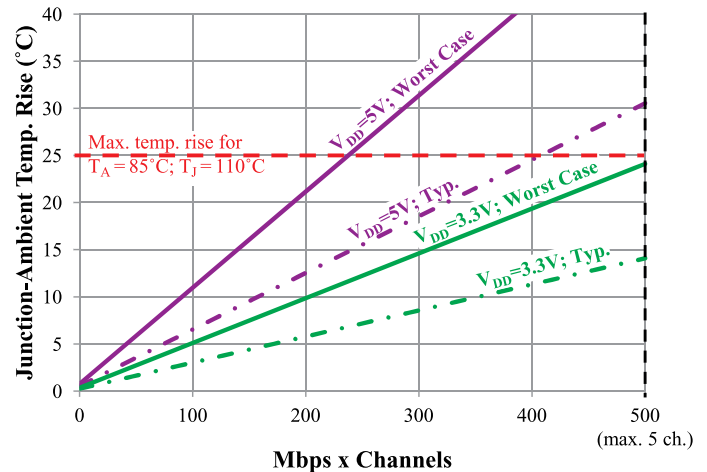
**Dynamic Power Consumption**

IsoLoop Isolators achieve their low power consumption from the way they transmit data across the isolation barrier. By detecting the edge transitions of the input logic signal and converting these to narrow current pulses, a magnetic field is created around the GMR Wheatstone bridge. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. Since the current pulses are narrow, about 2.5 ns, the power consumption is independent of mark-to-space ratio and solely dependent on frequency. This has obvious advantages over optocouplers, which have power consumption heavily dependent on mark-to-space ratio.

**Thermal Management**

IsoLoop Isolators are designed for low power dissipation and thermal performance, providing unmatched channel density for high-performance isolators. Nevertheless, package temperature rise should be considered when running multiple channels at high speed. Power consumption is higher at 5 volt operation than at 3.3 volts, and dynamic supply current is higher on the input side of the isolators than the output side, so thermal management is more important with five-volt input-side power supplies.

IL260/IL261/IL262 parts have a maximum junction temperature of 110°C. Based on the specifications contained in this datasheet, the derating curve at typical operating conditions is as follows:



**Power Supply Decoupling**

Both power supplies should be bypassed with 0.1 μF typical (0.047 μF minimum) capacitors as close as possible to the V<sub>DD</sub> pins. Ground planes for both GND<sub>1</sub> and GND<sub>2</sub> are highly recommended for data rates above 10 Mbps.

**Maintaining Creepage**

Creepage distances are often critical in isolated circuits. In addition to meeting JEDEC standards, NVE isolator packages have unique creepage specifications. Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance. Package drawings and recommended pad layouts are included in this datasheet.

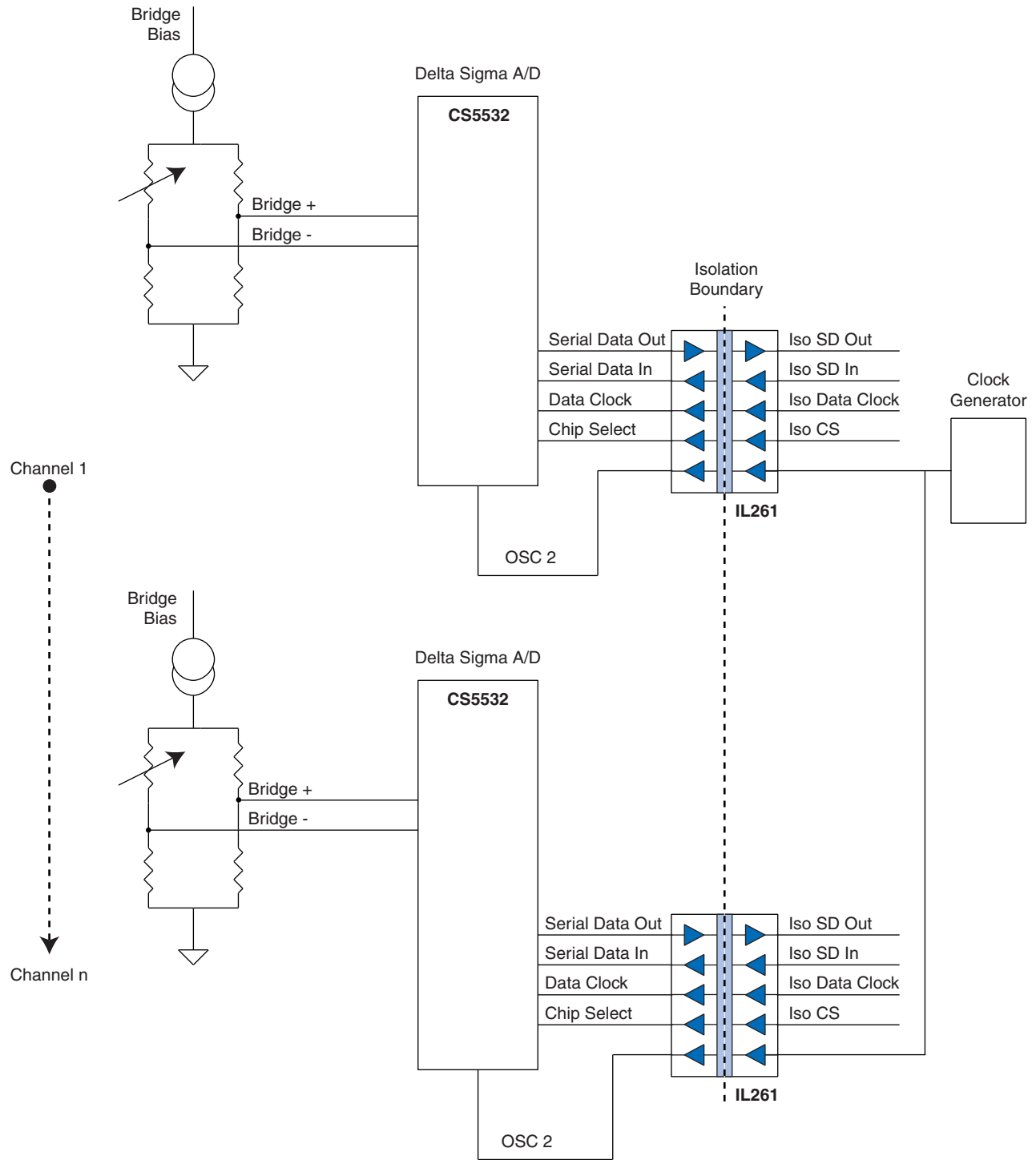
**Signal Status on Start-up and Shut Down**

To minimize power dissipation, input signals are differentiated and then latched on the output side of the isolation barrier to reconstruct the signal. This could result in an ambiguous output state depending on power up, shutdown and power loss sequencing. Therefore, the designer should consider including an initialization signal in the start-up circuit. Initialization consists of toggling the input either high then low, or low then high.



**Application Diagram—Multi-Channel Delta-Sigma A/D Converter**

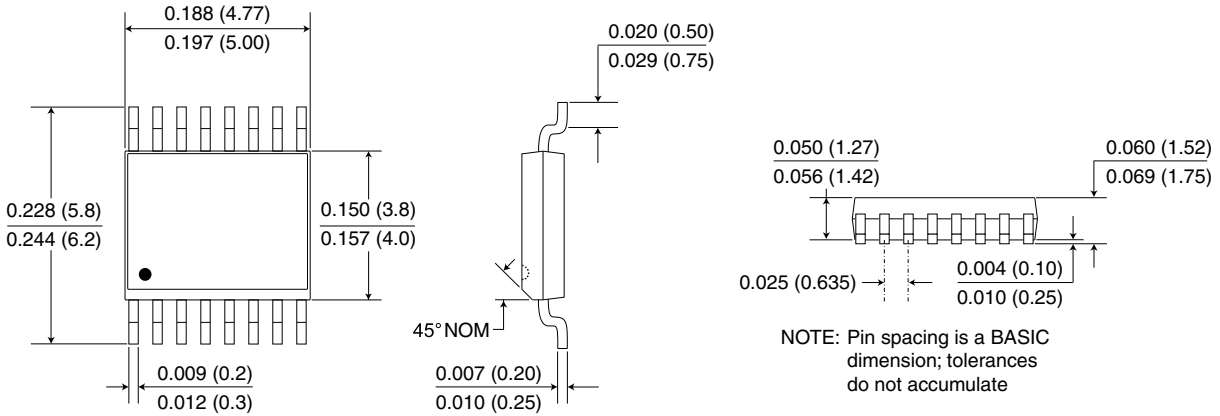
In a typical single-channel delta-sigma ADC, the system clock is located on the isolated side of the system and only four channels of isolation are required. With multiple ADCs configured in a channel-to-channel isolation configuration, however, clock jitter and edge placement accuracy of the system clock must be matched between ADCs. The best solution is to use a single clock on the system side and distribute the clock to each ADC. The five-channel IL261 is ideal, with the fifth channel used to distribute a single, isolated clock to multiple ADCs as shown below:



**Package Drawings**

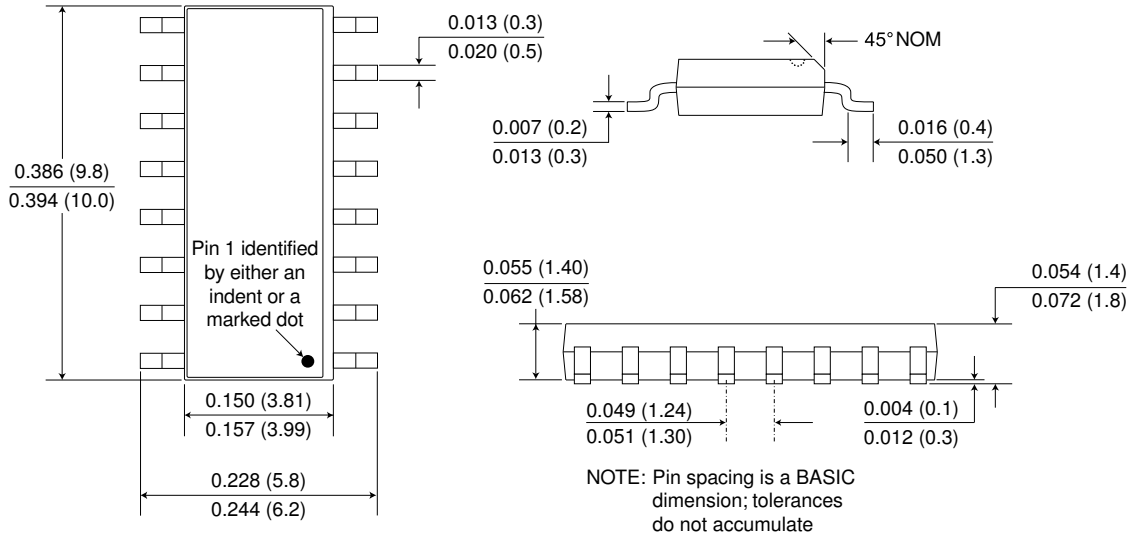
**Ultraminiature 16-pin QSOP Package (-1 suffix)**

Dimensions in inches (mm); scale = approx. 5X



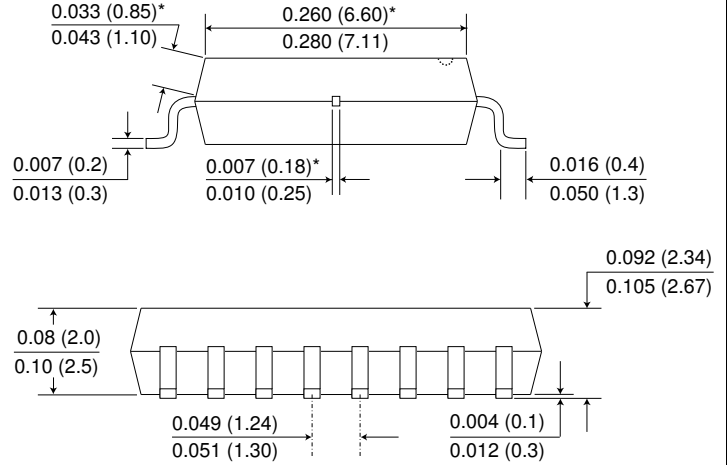
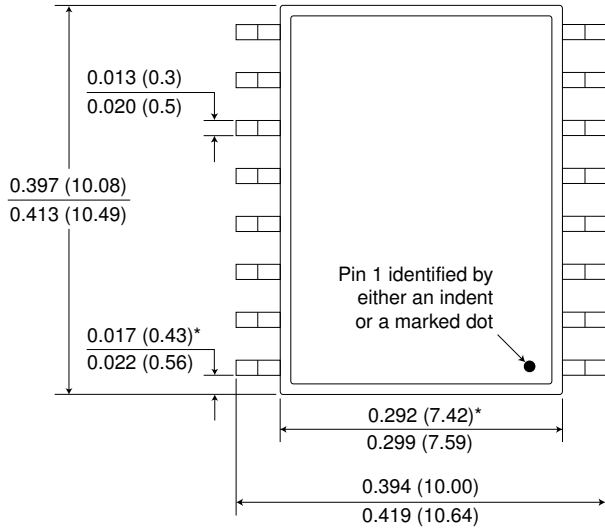
**0.15" 16-pin SOIC Package (-3 suffix)**

Dimensions in inches (mm); scale = approx. 5X



**0.3" 16-pin SOIC Package (no suffix)**

Dimensions in inches (mm); scale = approx. 5X



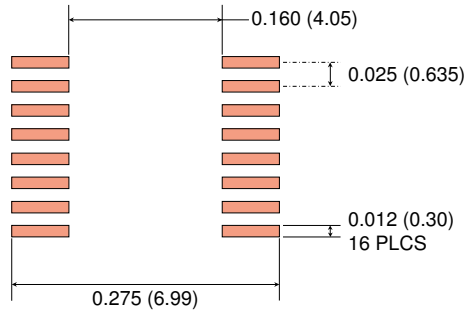
NOTE: Pin spacing is a BASIC dimension; tolerances do not accumulate

\*Specified for True 8™ package to guarantee 8 mm creepage per IEC 60601.

**Recommended Pad Layouts**

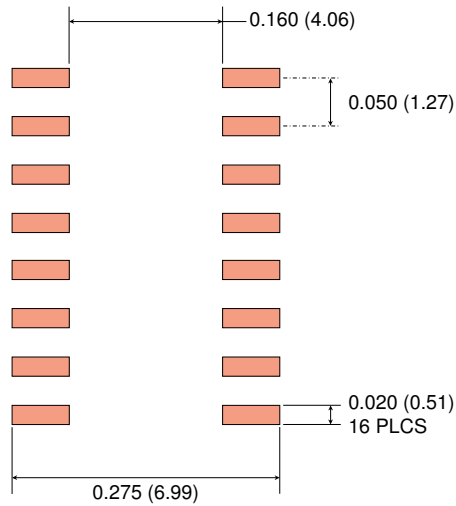
**4 mm x 5 mm 16-pin QSOP Pad Layout**

Dimensions in inches (mm); scale = approx. 5X



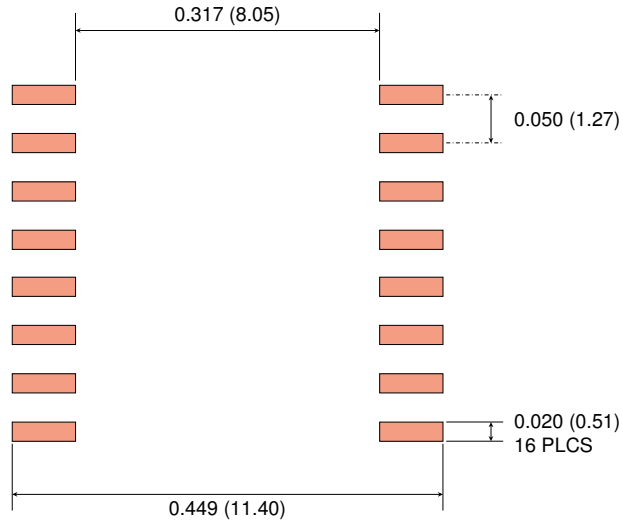
**0.15" 16-pin SOIC Pad Layout**

Dimensions in inches (mm); scale = approx. 5X



**0.3" 16-pin SOIC Pad Layout**

Dimensions in inches (mm); scale = approx. 5X



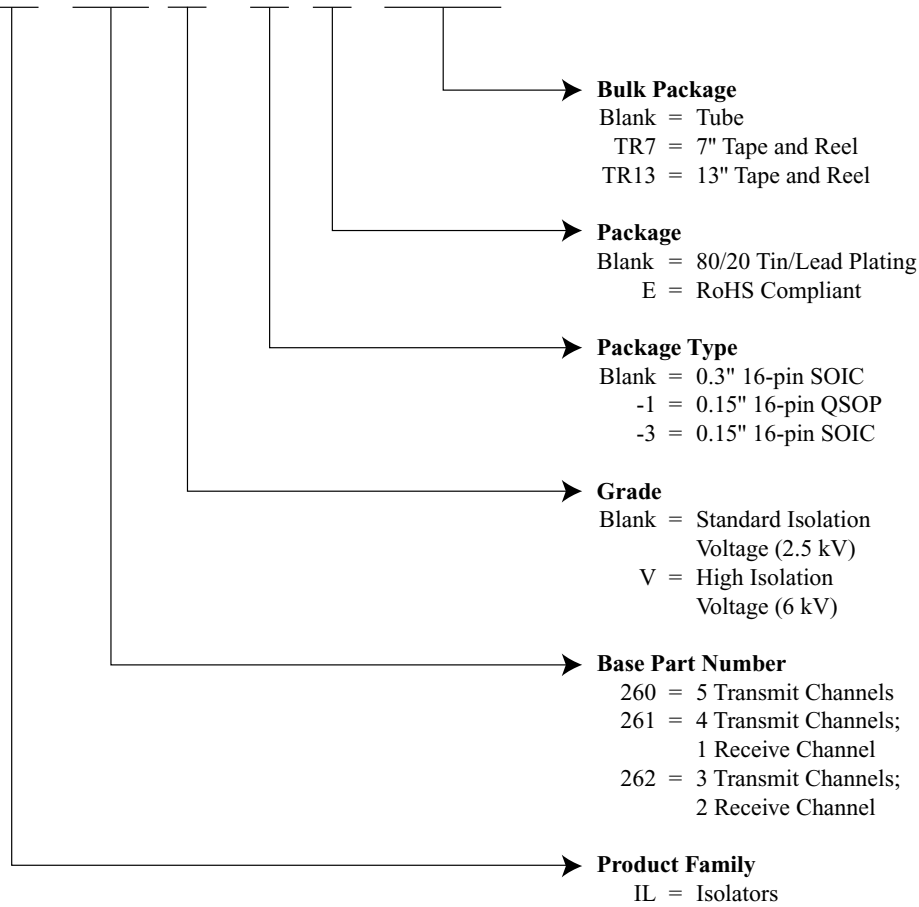
## Available Parts

Available Parts	Transmit Channels	Receive Channels	Isolation Voltage (RMS)	Package
IL260-1E	5	0	2.5 kV	QSOP
IL260-3E	5	0	2.5 kV	Narrow SOIC
IL260E	5	0	2.5 kV	Wide SOIC
IL260VE	5	0	6 kV	Wide SOIC
IL261-1E	4	1	2.5 kV	QSOP
IL261-3E	4	1	2.5 kV	Narrow SOIC
IL261E	4	1	2.5 kV	Wide SOIC
IL261VE	4	1	6 kV	Wide SOIC
IL262-3E	3	2	2.5 kV	Narrow SOIC
IL262E	3	2	2.5 kV	Wide SOIC
IL262VE	3	2	6 kV	Wide SOIC

All part types are available on tape and reel.

## Ordering Information

### IL 260 V - 3 E TR13



### Valid Part Numbers

IL260  
IL260E  
IL260VE  
IL260-1E  
IL260-3  
IL260-3E  
IL261  
IL261E  
IL261VE  
IL261-1E  
IL261-3  
IL261-3E  
IL262  
IL262E  
IL262VE  
IL262-3  
IL262-3E

All IL260-Series part types are available on tape and reel.



## Revision History

**ISB-DS-001-IL260/1/2-W**  
January 2020

### Changes

- Reduced minimum supply voltage to 2.5 V (p. 2).
- Updated EMC standards.
- Deleted minimum magnetic field immunity specifications (not 100% tested).
- Updated thermal specifications (p. 7).

**ISB-DS-001-IL260/1/2-V**

### Change

- VDE certification and UL approval for V-Series versions (6 kV reinforced isolation).

**ISB-DS-001-IL260/1/2-U**

### Changes

- Updated VDE certification standard to VDE V 0884-10.
- Upgraded “VE” Version Surge Immunity specification to 12.8 kV.
- Upgraded “VE” Version VDE 0884-10 rating to reinforced insulation.
- Corrected QSOP pin width dimension (p. 10).

**ISB-DS-001-IL260/1/2-T**

### Changes

- Increased V-Series isolation voltage to 6 kVrms.
- Increased typ. Total Barrier Thickness specification to 0.016 mm.
- Increased CTI min. specification to  $\geq 600 V_{RMS}$ .

**ISB-DS-001-IL260/1/2-S**

### Changes

- Added V-Series 5 kV isolation voltage versions.
- More detailed “Available Parts” table.

**ISB-DS-001-IL260/1/2-R**

### Changes

- Added QSOP packages (-1 suffix).
- Revised and added details to thermal characteristic specifications (p. 2).
- Added VDE 0884 Safety-Limiting Values (p. 3).
- Added “Thermal Management” paragraph in Applications section.

**ISB-DS-001-IL260/1/2-Q**

### Change

- IEC 60747-5-5 (VDE 0884) certification.

**ISB-DS-001-IL260/1/2-P**

### Changes

- Tighter quiescent current specifications.
- Upgraded from MSL 2 to MSL 1.

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*January 2020*