

# ESD7002, SZESD7002

## ESD Protection Diode

### Low Capacitance ESD Protection Diode for High Speed Data Line

The ESD7002 surge protection device is designed to protect high speed data lines from ESD. Ultra-low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines. The flow-through style package allows for easy PCB layout and matched trace lengths necessary to maintain consistent impedance between high speed differential lines such as USB 3.0 and HDMI.

#### Features

- Low Capacitance (0.3 pF Typical, I/O to GND)
- Diode capacitance matching
- Protection for the Following IEC Standards:
- IEC 61000-4-2 (Level 4)
- Low ESD Clamping Voltage
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

#### Typical Applications

- USB2.0/3.0
- LVDS
- HDMI
- High Speed Differential Pairs

#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

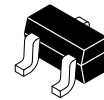
Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T <sub>J</sub>	-55 to +125	°C
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C
Lead Solder Temperature – Maximum (10 Seconds)	T <sub>L</sub>	260	°C
IEC 61000-4-2 Contact (ESD)	ESD	±8	kV
IEC 61000-4-2 Air (ESD)	ESD	±15	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



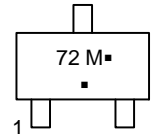
ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)



SC-70  
CASE 419  
STYLE 4

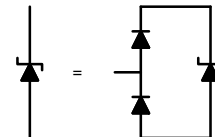
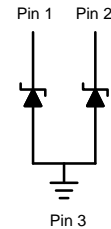
#### MARKING DIAGRAM



72 = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

#### PIN CONFIGURATION AND SCHEMATIC



#### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

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## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	$V_{RWM}$	I/O Pin to GND			16	V
Breakdown Voltage	$V_{BR}$	$I_T = 1\text{ mA}$ , I/O Pin to GND	16.5	23		V
Reverse Leakage Current	$I_R$	$V_{RWM} = 5\text{ V}$ , I/O Pin to GND			1	$\mu\text{A}$
Clamping Voltage (Note 1)	$V_C$	IEC61000-4-2, $\pm 8\text{ kV}$ Contact	See Figures 3 and 4			
Clamping Voltage TLP (Note 2)	$V_C$	$I_{PP} = 8\text{ A}$ $I_{PP} = 16\text{ A}$ $I_{PP} = -8\text{ A}$ $I_{PP} = -16\text{ A}$		31.2 33.9 -5.5 -10.8		V
Junction Capacitance Match	$\Delta C_J$	$V_R = 0\text{ V}$ , $f = 1\text{ MHz}$ between I/O1 to GND and I/O 2 to GND		5	10	%
Junction Capacitance	$C_J$	$V_R = 0\text{ V}$ , $f = 1\text{ MHz}$ between I/O Pins		0.2	0.4	$\mu\text{F}$
Junction Capacitance	$C_J$	$V_R = 0\text{ V}$ , $f = 1\text{ MHz}$ between I/O Pins and GND		0.3	0.5	$\mu\text{F}$
3dB Bandwidth	$f_{BW}$	$R_L = 50\ \Omega$		5		GHz

- For test procedure see Figures 5 and 6 and application note AND8307/D.
- ANSI/ESD STM5.5.1 – Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.  
TLP conditions:  $Z_0 = 50\ \Omega$ ,  $t_p = 100\text{ ns}$ ,  $t_r = 4\text{ ns}$ , averaging window;  $t_1 = 30\text{ ns}$  to  $t_2 = 60\text{ ns}$ .

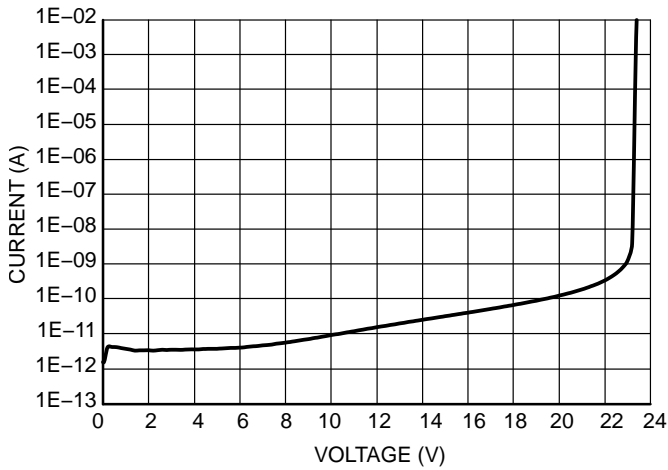


Figure 1. Typical IV Characteristic Curve

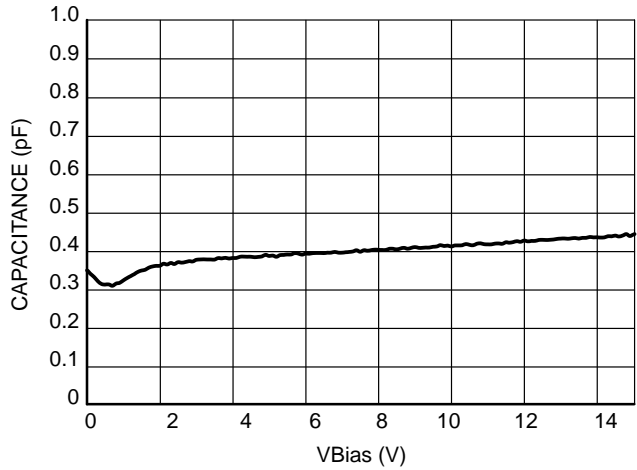


Figure 2. Typical CV Characteristic Curve

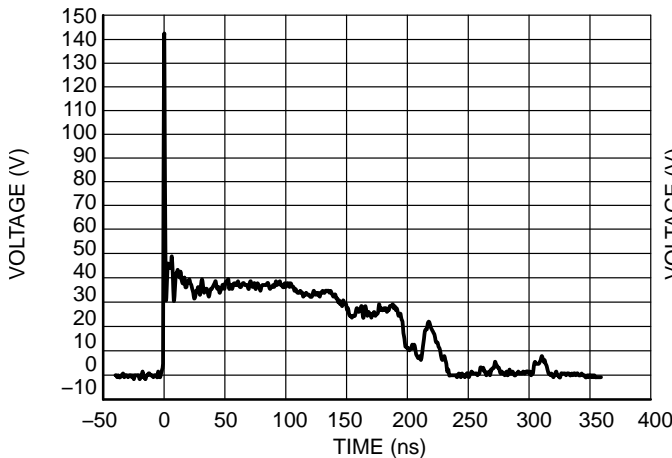


Figure 3. IEC61000-4-2 +8 kV Contact ESD Clamping Voltage

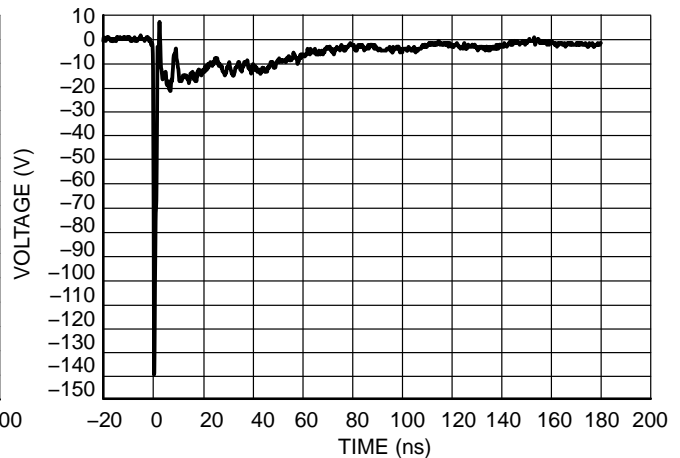


Figure 4. IEC61000-4-2 -8 kV Contact ESD Clamping Voltage

## ESD7002, SZESD7002

### IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

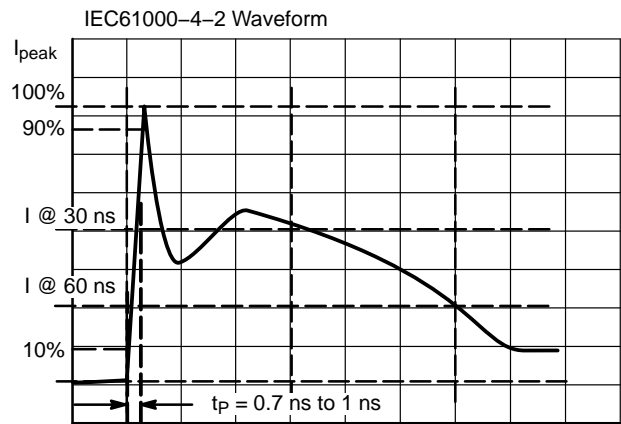


Figure 5. IEC61000-4-2 Spec

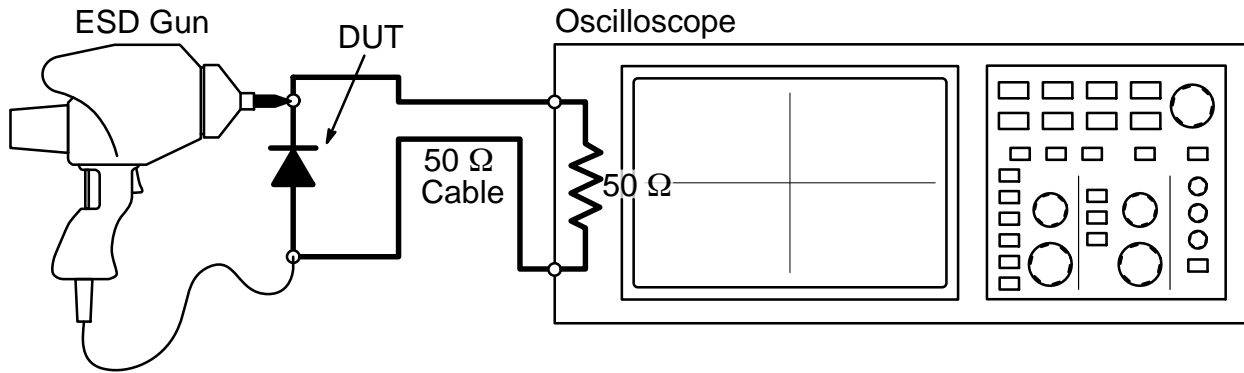


Figure 6. Diagram of ESD Clamping Voltage Test Setup

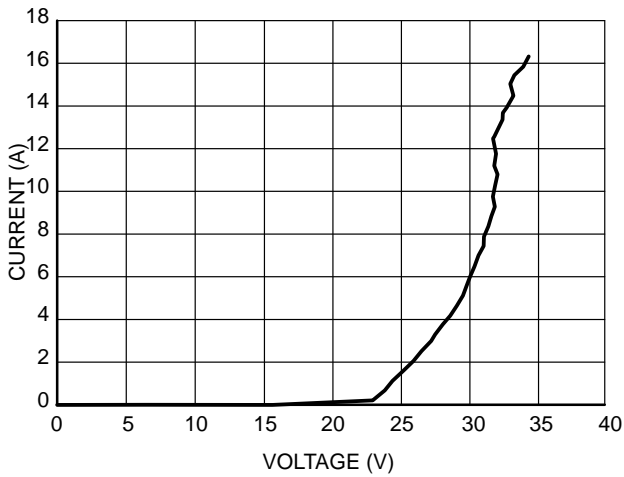
The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

### ESD Voltage Clamping

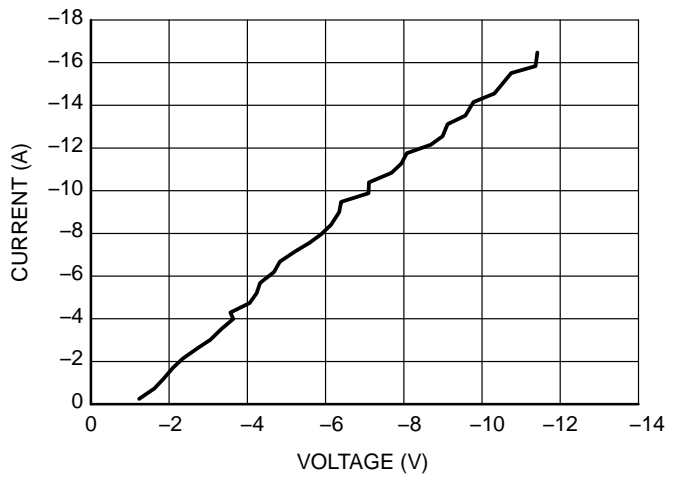
For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

## ESD7002, SZESD7002



**Figure 7. Positive TLP IV Curve**

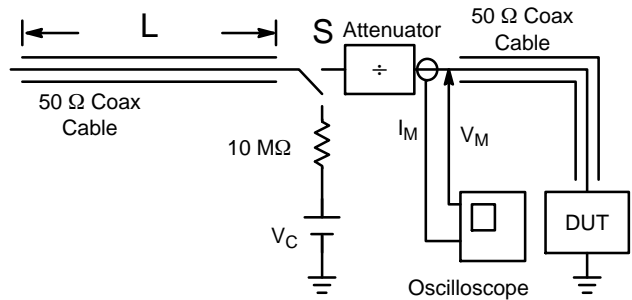


**Figure 8. Negative TLP IV Curve**

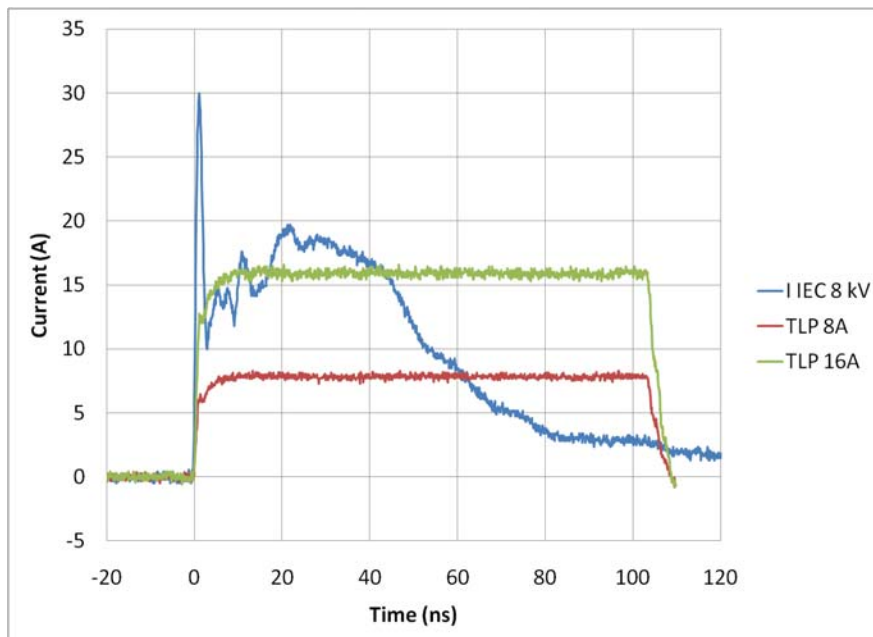
NOTE: TLP parameter:  $Z_0 = 50 \Omega$ ,  $t_p = 100 \text{ ns}$ ,  $t_r = 300 \text{ ps}$ , averaging window:  $t_1 = 30 \text{ ns}$  to  $t_2 = 60 \text{ ns}$ .

### Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I-V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 9. TLP I-V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 10 where an 8 kV IEC 61000-4-2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I-V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.



**Figure 9. Simplified Schematic of a Typical TLP System**



**Figure 10. Comparison Between 8 kV IEC 61000-4-2 and 8 A and 16 A TLP Waveforms**

# ESD7002, SZESD7002

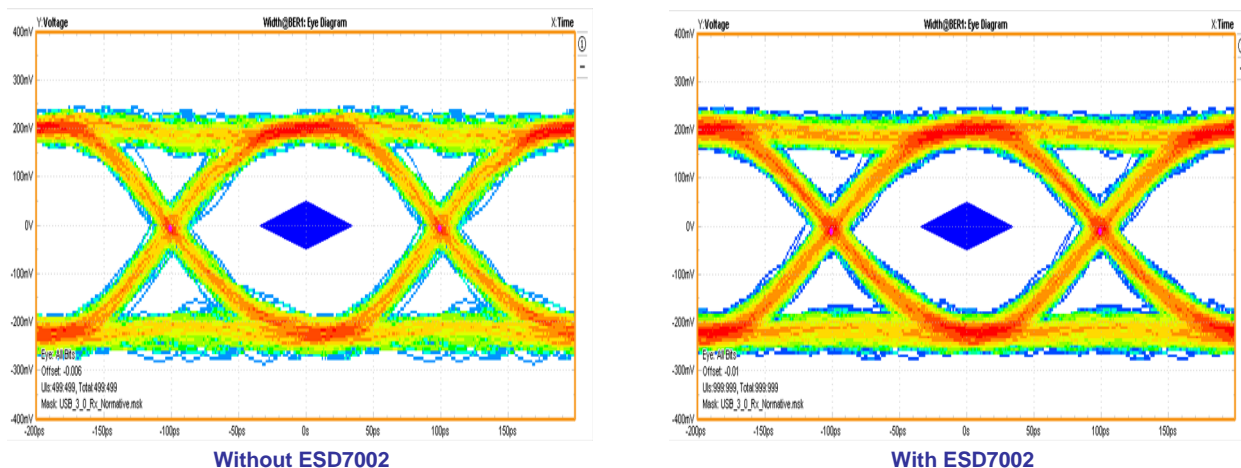


Figure 11. USB3.0 Eye Diagram with and without ESD7002 at 5 Gb/s

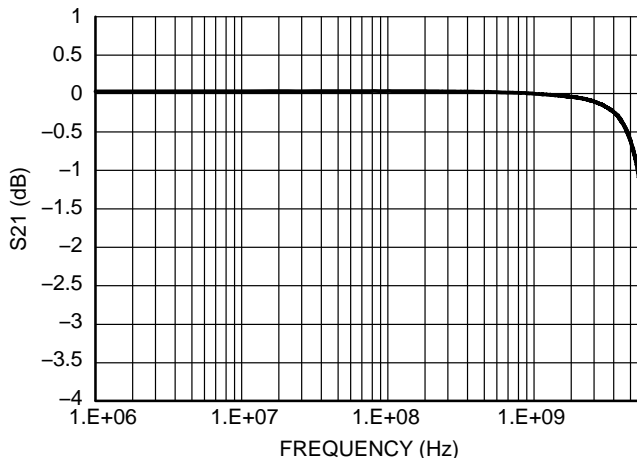


Figure 12. Typical Insertion Loss

## ORDERING INFORMATION

Device	Package	Shipping†
ESD7002WTT1G	SC-70 (Pb-Free)	3000 / Tape & Reel
SZESD7002WTT1G*	SC-70 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



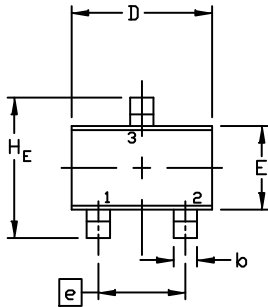
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SC-70 (SOT-323)  
CASE 419  
ISSUE P

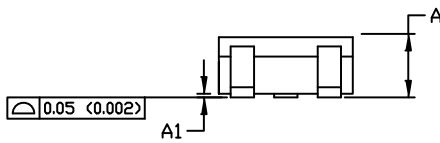
DATE 07 OCT 2021

NOTES:

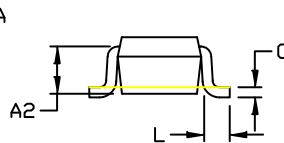
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH



TOP VIEW



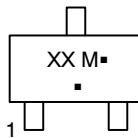
SIDE VIEW



END VIEW

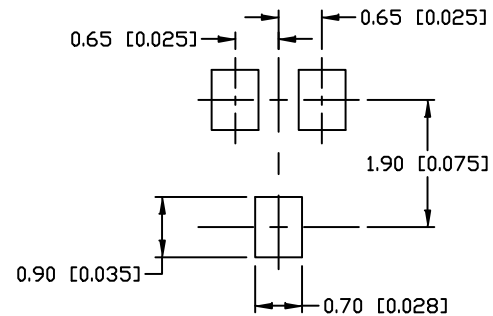
DIM	MILLIMETERS			INCHES		
	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.
A	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2	0.70 REF			0.028 BSC		
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.10	2.20	0.071	0.083	0.087
E	1.15	1.24	1.35	0.045	0.049	0.053
e	1.20	1.30	1.40	0.047	0.051	0.055
e1	0.65 BSC			0.026 BSC		
L	0.20	0.38	0.56	0.008	0.015	0.022
H <sub>E</sub>	2.00	2.10	2.40	0.079	0.083	0.095

GENERIC  
MARKING DIAGRAM



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



\* For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOLDERING FOOTPRINT

STYLE 1:  
CANCELLED

STYLE 2:  
PIN 1. ANODE  
2. N.C.  
3. CATHODE

STYLE 3:  
PIN 1. BASE  
2. EMITTER  
3. COLLECTOR

STYLE 4:  
PIN 1. CATHODE  
2. CATHODE  
3. ANODE

STYLE 5:  
PIN 1. ANODE  
2. ANODE  
3. CATHODE

STYLE 6:  
PIN 1. EMITTER  
2. BASE  
3. COLLECTOR

STYLE 7:  
PIN 1. BASE  
2. EMITTER  
3. COLLECTOR

STYLE 8:  
PIN 1. GATE  
2. SOURCE  
3. DRAIN

STYLE 9:  
PIN 1. ANODE  
2. CATHODE  
3. CATHODE-ANODE

STYLE 10:  
PIN 1. CATHODE  
2. ANODE  
3. ANODE-CATHODE

STYLE 11:  
PIN 1. CATHODE  
2. CATHODE  
3. CATHODE

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