

74LVC2G86

Dual 2-input EXCLUSIVE-OR gate

Rev. 13 — 3 July 2017

Product data sheet

1 General description

The 74LVC2G86 provides a dual 2-input EXCLUSIVE-OR gate.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2 Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant inputs for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114F exceeds 2 000 V
 - MM JESD22-A115-A exceeds 200 V
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low-power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C

3 Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC2G86DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC2G86DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVC2G86GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm	SOT833-1
74LVC2G86GF	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 x 1 x 0.5 mm	SOT1089
74LVC2G86GM	-40 °C to +125 °C	XQFN8	plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 x 1.6 x 0.5 mm	SOT902-2
74LVC2G86GN	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.2 x 1.0 x 0.35 mm	SOT1116
74LVC2G86GS	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 x 1.0 x 0.35 mm	SOT1203
74LVC2G86GX	-40 °C to +125 °C	X2SON8	plastic thermal enhanced extremely thin small outline package; no leads; 8 terminals; body 1.35 x 0.8 x 0.35 mm	SOT1233

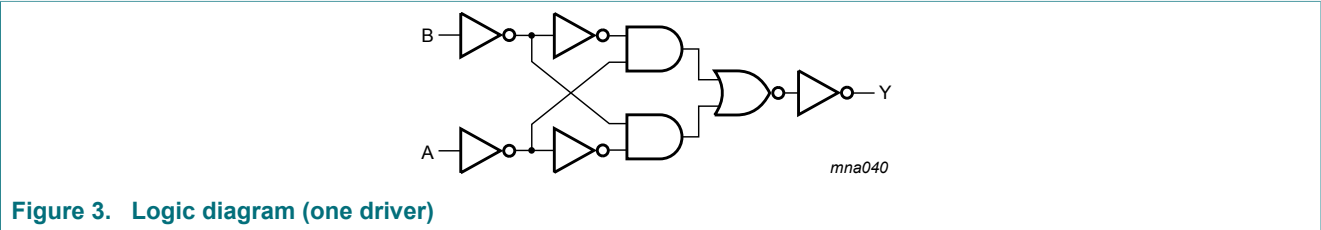
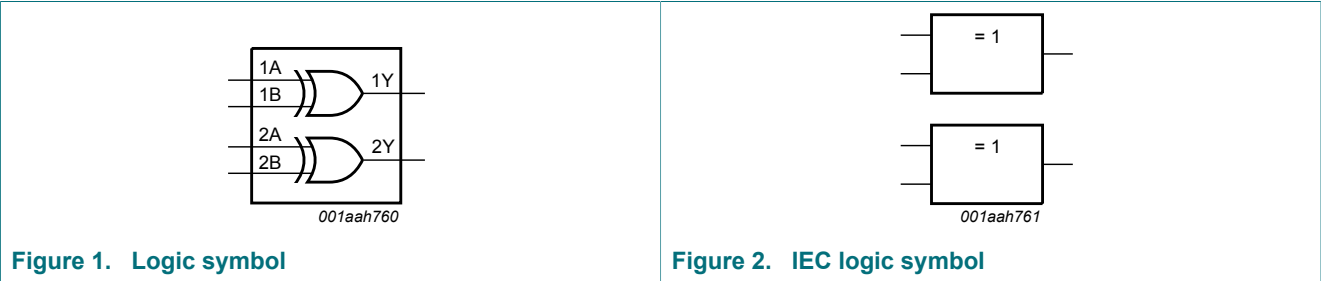
4 Marking

Table 2. Marking codes

Type number	Marking code ^[1]
74LVC2G86DP	V86
74LVC2G86DC	V86
74LVC2G86GT	V86
74LVC2G86GF	VH
74LVC2G86GM	V86
74LVC2G86GN	VH
74LVC2G86GS	VH
74LVC2G86GX	VH

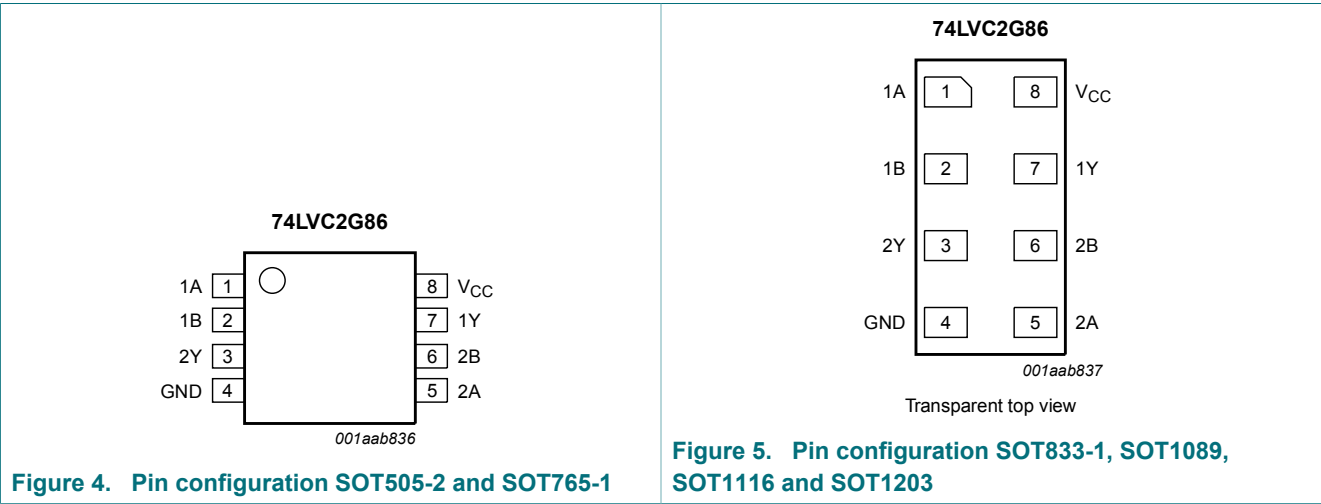
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

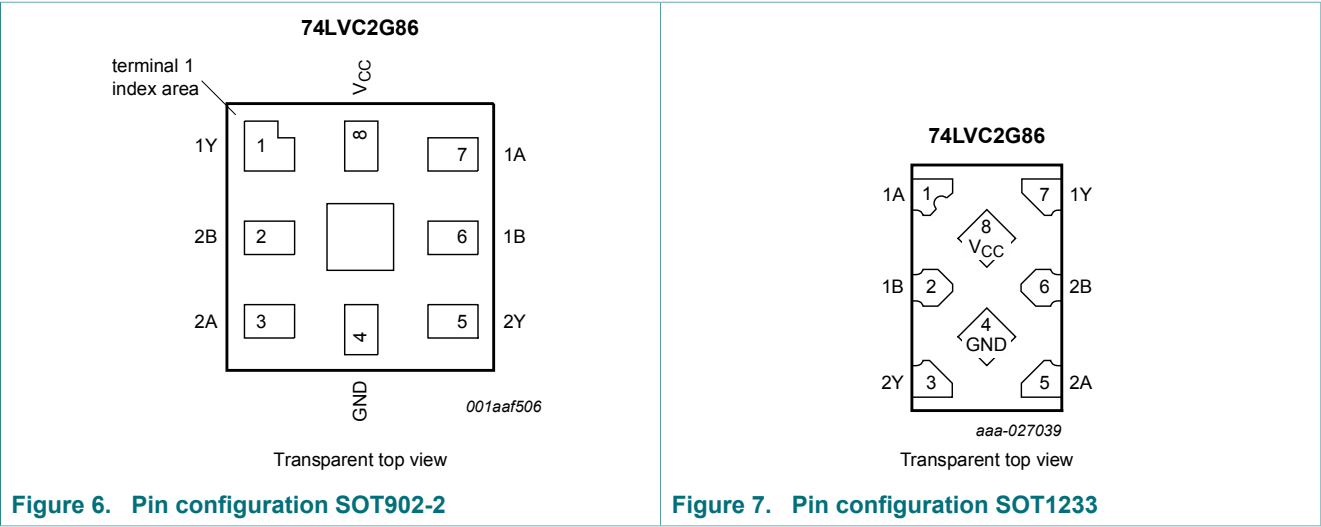
5 Functional diagram



6 Pinnig information

6.1 Pinning





6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT505-2, SOT765-1, SOT833-1, SOT1089, SOT1116, SOT1203 and SOT1233	SOT902-2	
1A, 2A	1, 5	7, 3	data input
1B, 2B	2, 6	6, 2	data input
GND	4	4	ground (0 V)
1Y, 2Y	7, 3	1, 5	data output
V _{CC}	8	8	supply voltage

7 Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level

Input		Output
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	L

8 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage	[1]	-0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	± 50	mA
V_O	output voltage	Active mode [1] [2]	-0.5	$V_{CC} + 0.5$	V
		Power-down mode [1] [2]	-0.5	+6.5	V
I_O	output current	$V_O = 0$ to V_{CC}	-	± 50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to $+125$ °C [3]	-	300	mW
T_{stg}	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When $V_{CC} = 0$ V (Power-down mode), the output voltage can be 5.5 V in normal operation.

[3] For TSSOP8 packages: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.

For VSSOP8 packages: above 110 °C the value of P_{tot} derates linearly with 8.0 mW/K.

For XSON8 and XQFN8 packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

For X2SON8 package: above 118 °C the value of P_{tot} derates linearly with 7.7 mW/K.

9 Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	Active mode	0	V_{CC}	V
		$V_{CC} = 0$ V; Power-down mode	0	5.5	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	-	20	ns/V
		$V_{CC} = 2.7$ V to 5.5 V	-	10	ns/V

10 Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
$T_{amb} = -40\text{ }^{\circ}\text{C to } +85\text{ }^{\circ}\text{C}$						
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65\text{ V to } 1.95\text{ V}$	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$	1.7	-	-	V
		$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$	2.0	-	-	V
		$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$	$0.7 \times V_{CC}$	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65\text{ V to } 1.95\text{ V}$	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$	-	-	0.7	V
		$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$	-	-	0.8	V
		$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$	-	-	$0.3 \times V_{CC}$	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$				
		$I_O = 100\text{ }\mu\text{A}; V_{CC} = 1.65\text{ V to } 5.5\text{ V}$	-	-	0.1	V
		$I_O = 4\text{ mA}; V_{CC} = 1.65\text{ V}$	-	0.07	0.45	V
		$I_O = 8\text{ mA}; V_{CC} = 2.3\text{ V}$	-	0.12	0.3	V
		$I_O = 12\text{ mA}; V_{CC} = 2.7\text{ V}$	-	0.17	0.4	V
		$I_O = 24\text{ mA}; V_{CC} = 3.0\text{ V}$	-	0.33	0.55	V
		$I_O = 32\text{ mA}; V_{CC} = 4.5\text{ V}$	-	0.39	0.55	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$				
		$I_O = -100\text{ }\mu\text{A}; V_{CC} = 1.65\text{ V to } 5.5\text{ V}$	$V_{CC} - 0.1$	-	-	V
		$I_O = -4\text{ mA}; V_{CC} = 1.65\text{ V}$	1.2	1.54	-	V
		$I_O = -8\text{ mA}; V_{CC} = 2.3\text{ V}$	1.9	2.15	-	V
		$I_O = -12\text{ mA}; V_{CC} = 2.7\text{ V}$	2.2	2.50	-	V
		$I_O = -24\text{ mA}; V_{CC} = 3.0\text{ V}$	2.3	2.62	-	V
		$I_O = -32\text{ mA}; V_{CC} = 4.5\text{ V}$	3.8	4.11	-	V
I_I	input leakage current	$V_I = 5.5\text{ V or GND}; V_{CC} = 0\text{ V to } 5.5\text{ V}$	-	± 0.1	± 1	μA
I_{OFF}	power-off leakage current	$V_I \text{ or } V_O = 5.5\text{ V}; V_{CC} = 0\text{ V}$	-	± 0.1	± 2	μA
I_{CC}	supply current	$V_I = 5.5\text{ V or GND};$ $V_{CC} = 1.65\text{ V to } 5.5\text{ V}; I_O = 0\text{ A}$	-	0.1	4	μA
ΔI_{CC}	additional supply current	per pin; $V_I = V_{CC} - 0.6\text{ V};$ $V_{CC} = 2.3\text{ V to } 5.5\text{ V}; I_O = 0\text{ A};$	-	5	500	μA
C_I	input capacitance		-	2.5	-	pF

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
$T_{amb} = -40\text{ }^{\circ}\text{C to } +125\text{ }^{\circ}\text{C}$						
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65\text{ V to } 1.95\text{ V}$	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$	1.7	-	-	V
		$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$	2.0	-	-	V
		$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$	$0.7 \times V_{CC}$	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65\text{ V to } 1.95\text{ V}$	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$	-	-	0.7	V
		$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$	-	-	0.8	V
		$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$	-	-	$0.3 \times V_{CC}$	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$				
		$I_O = 100\text{ }\mu\text{A}; V_{CC} = 1.65\text{ V to } 5.5\text{ V}$	-	-	0.1	V
		$I_O = 4\text{ mA}; V_{CC} = 1.65\text{ V}$	-	-	0.70	V
		$I_O = 8\text{ mA}; V_{CC} = 2.3\text{ V}$	-	-	0.45	V
		$I_O = 12\text{ mA}; V_{CC} = 2.7\text{ V}$	-	-	0.60	V
		$I_O = 24\text{ mA}; V_{CC} = 3.0\text{ V}$	-	-	0.80	V
		$I_O = 32\text{ mA}; V_{CC} = 4.5\text{ V}$	-	-	0.80	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$				
		$I_O = -100\text{ }\mu\text{A}; V_{CC} = 1.65\text{ V to } 5.5\text{ V}$	$V_{CC} - 0.1$	-	-	V
		$I_O = -4\text{ mA}; V_{CC} = 1.65\text{ V}$	0.95	-	-	V
		$I_O = -8\text{ mA}; V_{CC} = 2.3\text{ V}$	1.7	-	-	V
		$I_O = -12\text{ mA}; V_{CC} = 2.7\text{ V}$	1.9	-	-	V
		$I_O = -24\text{ mA}; V_{CC} = 3.0\text{ V}$	2.0	-	-	V
		$I_O = -32\text{ mA}; V_{CC} = 4.5\text{ V}$	3.4	-	-	V
I_I	input leakage current	$V_I = 5.5\text{ V or GND}; V_{CC} = 0\text{ V to } 5.5\text{ V}$	-	-	± 1	μA
I_{OFF}	power-off leakage current	$V_I \text{ or } V_O = 5.5\text{ V}; V_{CC} = 0\text{ V}$	-	-	± 2	μA
I_{CC}	supply current	$V_I = 5.5\text{ V or GND};$ $V_{CC} = 1.65\text{ V to } 5.5\text{ V}; I_O = 0\text{ A}$	-	-	4	μA
ΔI_{CC}	additional supply current	per pin; $V_I = V_{CC} - 0.6\text{ V};$ $V_{CC} = 2.3\text{ V to } 5.5\text{ V}; I_O = 0\text{ A};$	-	-	500	μA

[1] All typical values are measured at $V_{CC} = 3.3\text{ V}$ and $T_{amb} = 25\text{ }^{\circ}\text{C}$.

11 Dynamic characteristics

Table 8. Dynamic characteristics
Voltages are referenced to GND (ground 0 V); for test circuit see Figure 9.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	nA, nB to nY; see Figure 8 ^[2]						
		V _{CC} = 1.65 V to 1.95 V	1.4	3.8	9.9	1.4	12.4	ns
		V _{CC} = 2.3 V to 2.7 V	0.8	2.5	5.7	0.8	7.2	ns
		V _{CC} = 2.7 V	0.8	3.0	5.7	0.8	7.2	ns
		V _{CC} = 3.0 V to 3.6 V	0.8	2.3	4.7	0.8	5.9	ns
		V _{CC} = 4.5 V to 5.5 V	0.6	1.9	3.6	0.6	4.5	ns
C _{PD}	power dissipation capacitance	per gate; V _I = GND to V _{CC} ; ^[3] V _{CC} = 3.3 V	-	15.8	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
Σ(C_L × V_{CC}² × f_o) = sum of outputs.

11.1 Waveforms and test circuit

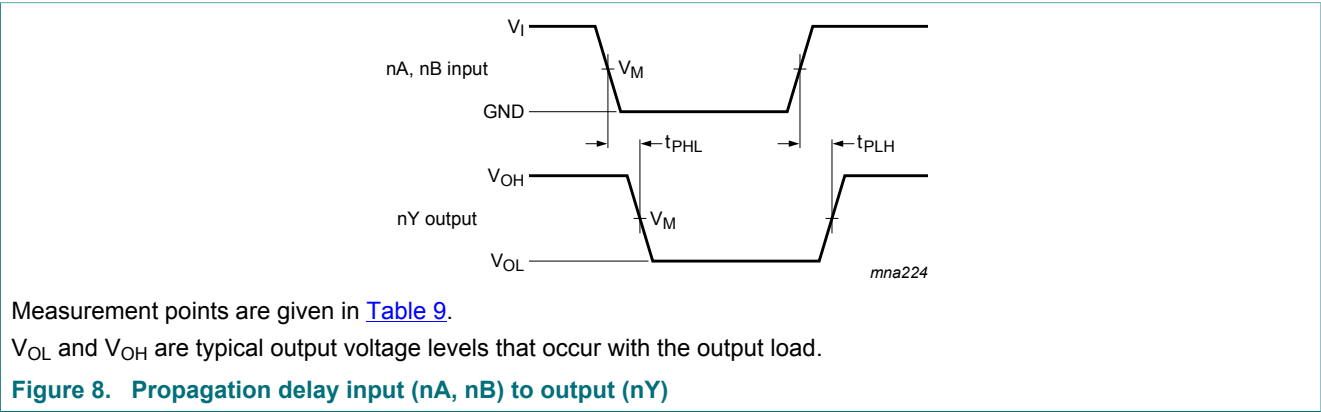
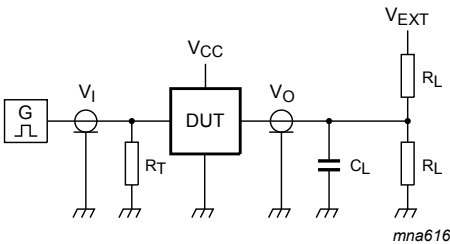


Table 9. Measurement points

Supply voltage	Input	Output
V _{CC}	V _M	V _M
1.65 V to 1.95 V	0.5 x V _{CC}	0.5 x V _{CC}
2.3 V to 2.7 V	0.5 x V _{CC}	0.5 x V _{CC}
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	0.5 x V _{CC}	0.5 x V _{CC}



Test data is given in [Table 10](#).
Definitions for test circuit:
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.
 V_{EXT} = External voltage for measuring switching times.

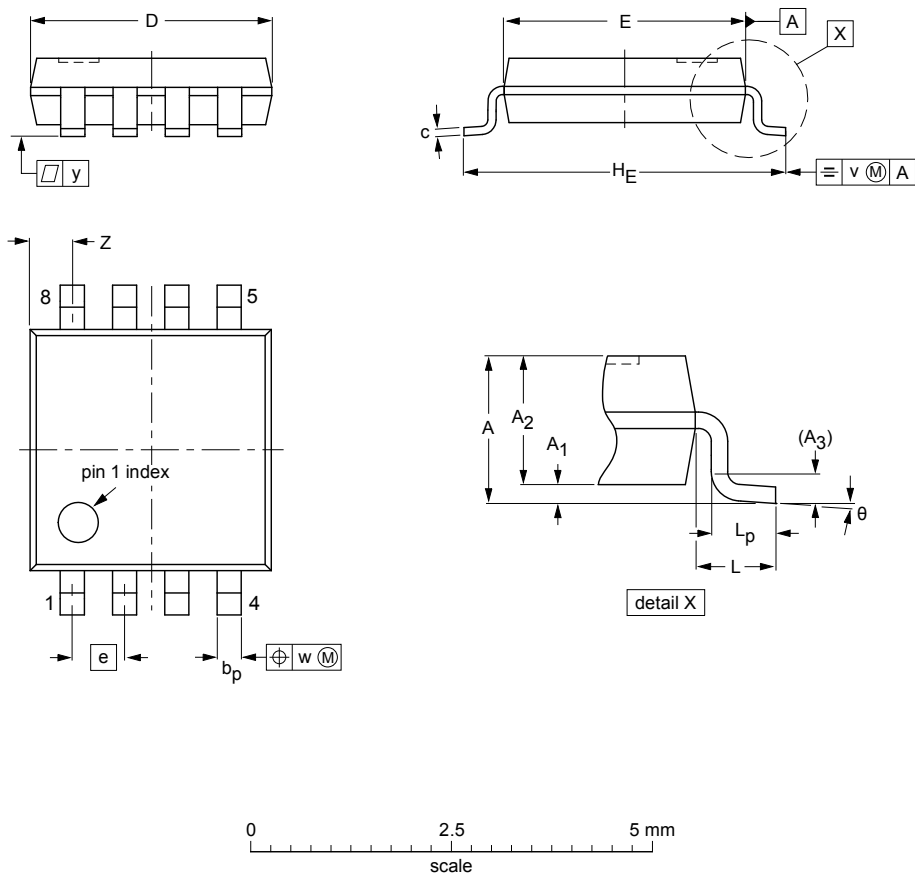
Figure 9. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input	Load			V _{EXT}
V _{CC}	V _I	t _r , t _f	C _L	R _L	t _{PLH} , t _{PHL}
1.65 V to 1.95 V	V _{CC}	≤ 2.0 ns	30 pF	1 kΩ	open
2.3 V to 2.7 V	V _{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
4.5 V to 5.5 V	V _{CC}	≤ 2.5 ns	50 pF	500 Ω	open

12 Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		---				02-01-16

Figure 10. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

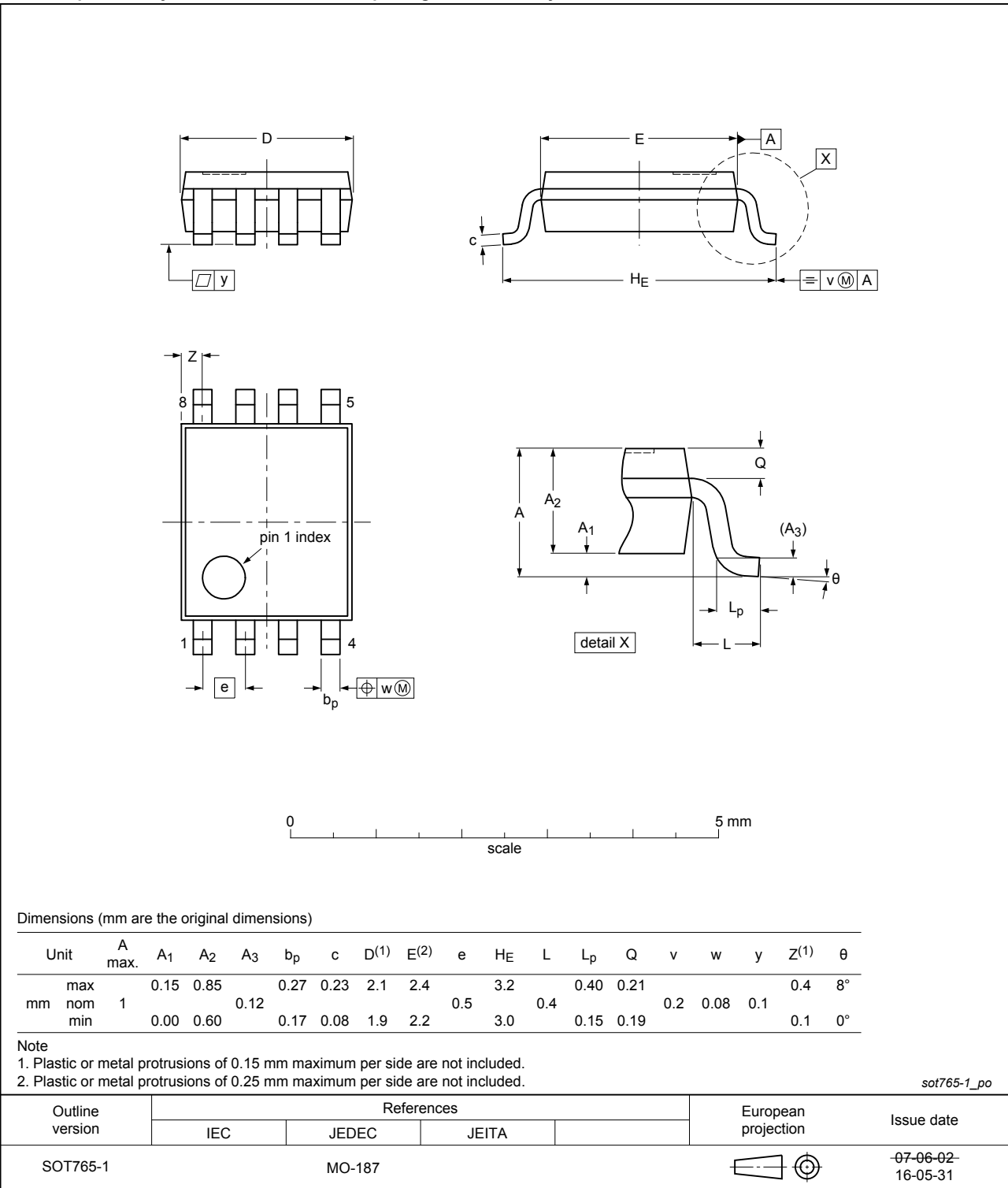
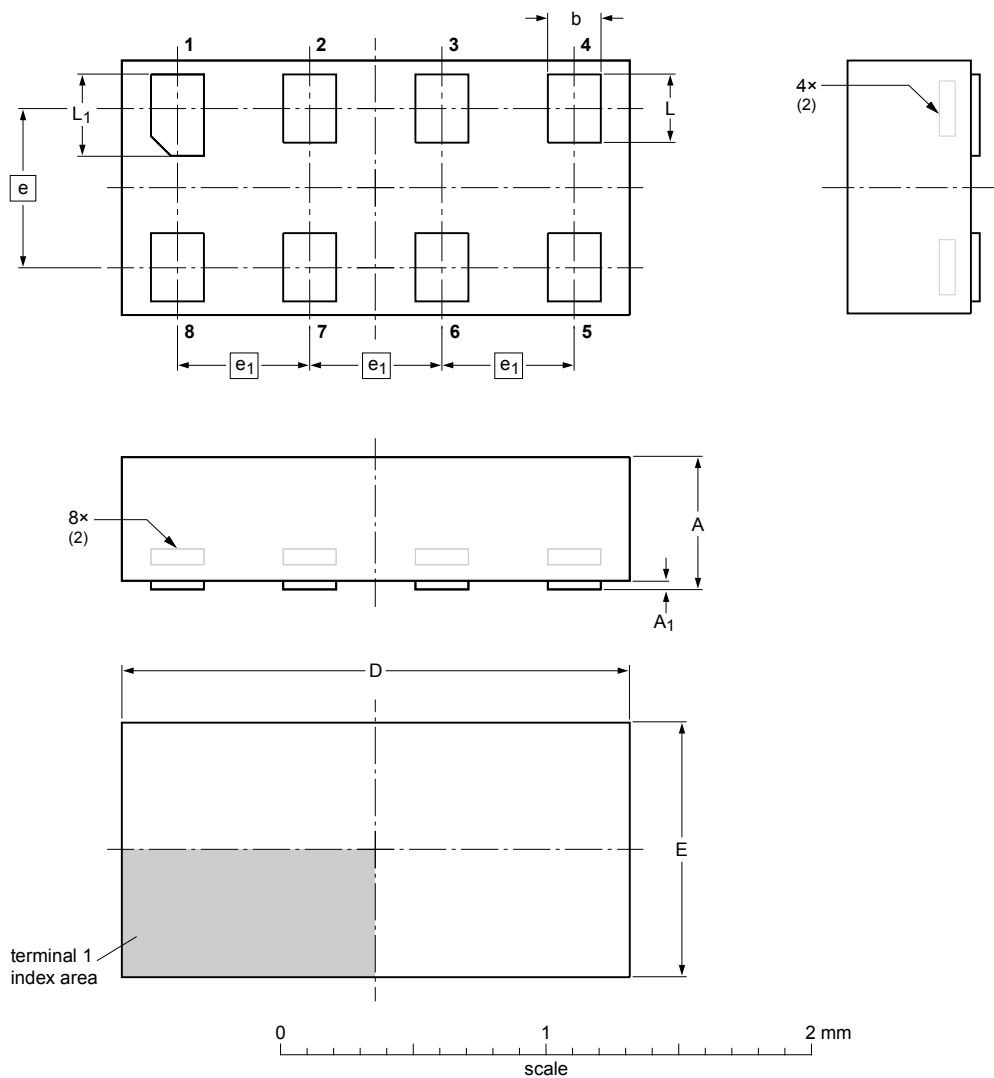


Figure 11. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm SOT833-1



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾ max	A ₁ max	b	D	E	e	e ₁	L	L ₁
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

- Notes
- 1. Including plating thickness.
 - 2. Can be visible in some manufacturing processes.

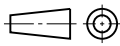
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT833-1	---	MO-252	---			07-11-14 07-12-07

Figure 12. Package outline SOT833-1 (XSON8)

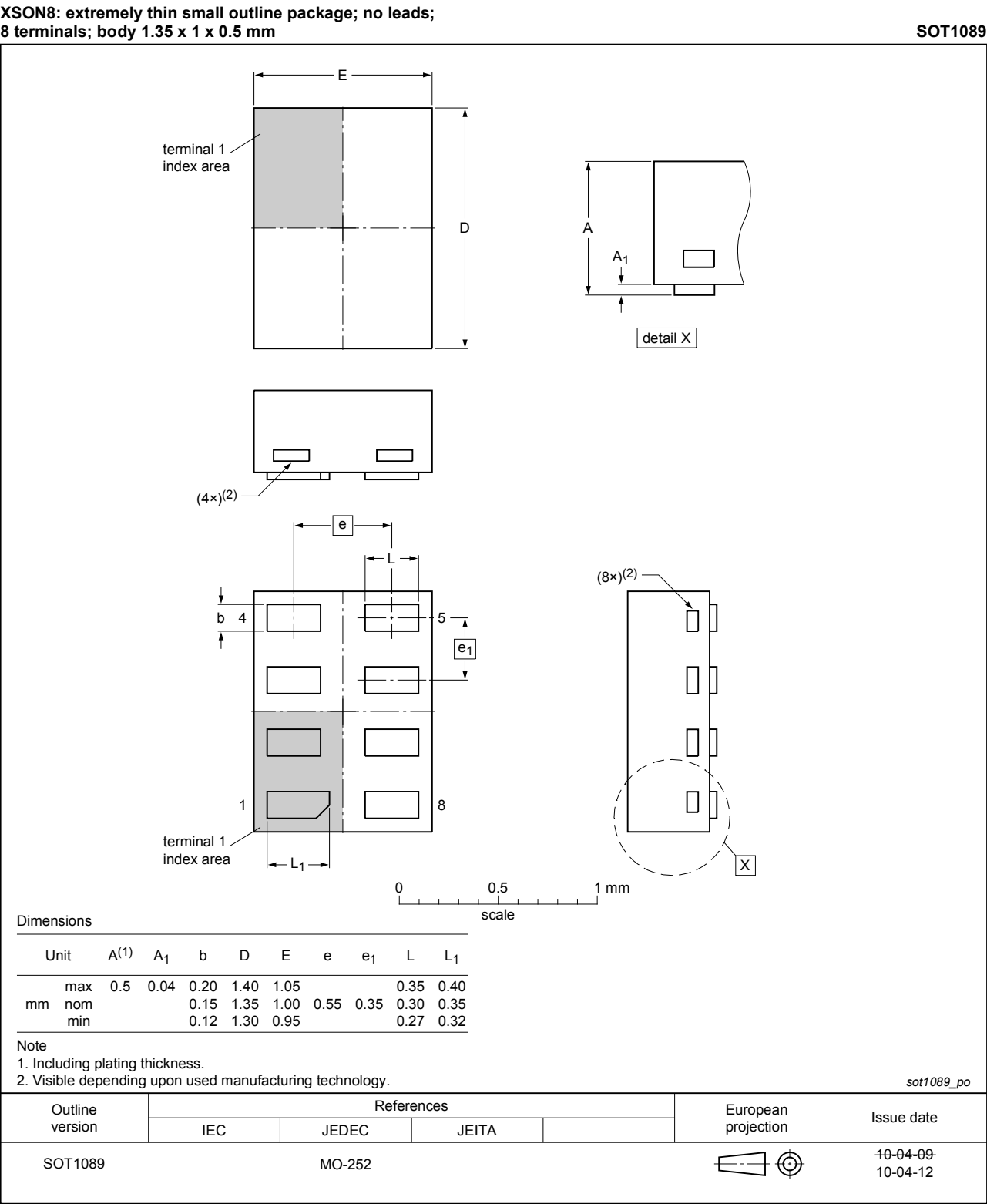


Figure 13. Package outline SOT1089 (XSON8)

XQFN8: plastic, extremely thin quad flat package; no leads;
8 terminals; body 1.6 x 1.6 x 0.5 mm

SOT902-2

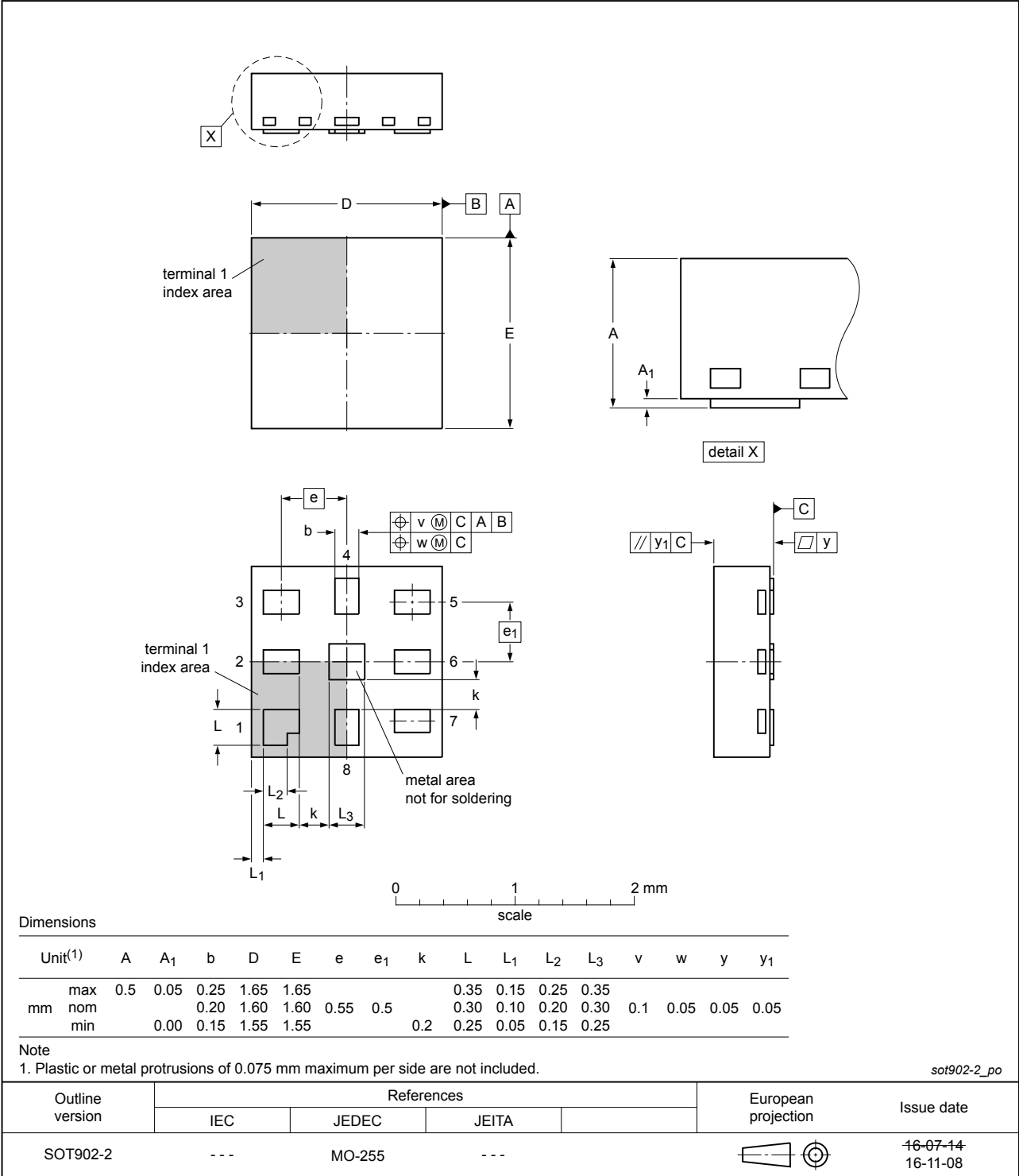
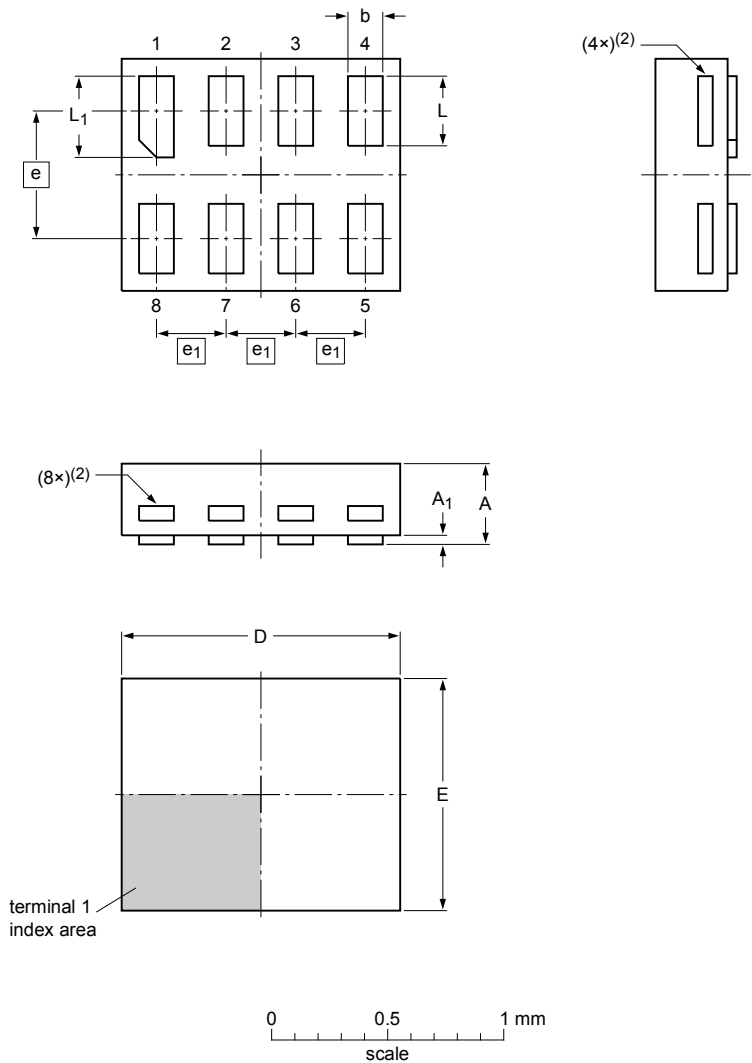


Figure 14. Package outline SOT902-2 (XQFN8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.2 x 1.0 x 0.35 mm

SOT1116



Dimensions

Unit	A ⁽¹⁾	A ₁	b	D	E	e	e ₁	L	L ₁
mm	max	0.35	0.04	0.20	1.25	1.05		0.35	0.40
	nom			0.15	1.20	1.00	0.55	0.30	0.35
	min			0.12	1.15	0.95		0.27	0.32

Note

- 1. Including plating thickness.
- 2. Visible depending upon used manufacturing technology.

sot1116_po

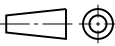
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1116						10-04-02- 10-04-07

Figure 15. Package outline SOT1116 (XSON8)

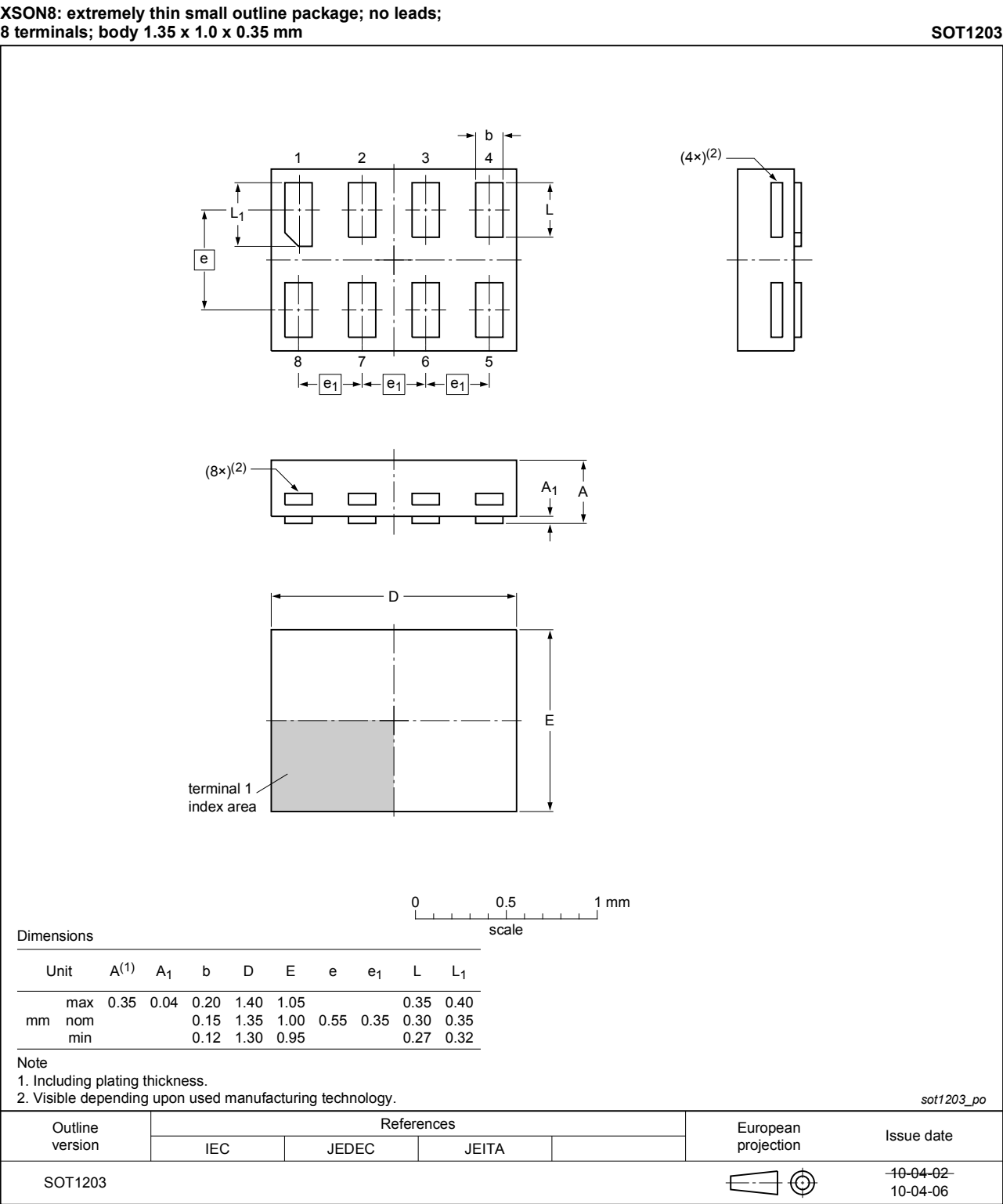


Figure 16. Package outline SOT1203 (XSON8)

X2SON8: plastic thermal enhanced extremely thin small outline package; no leads;
8 terminals; body 1.35 x 0.8 x 0.35 mm

SOT1233

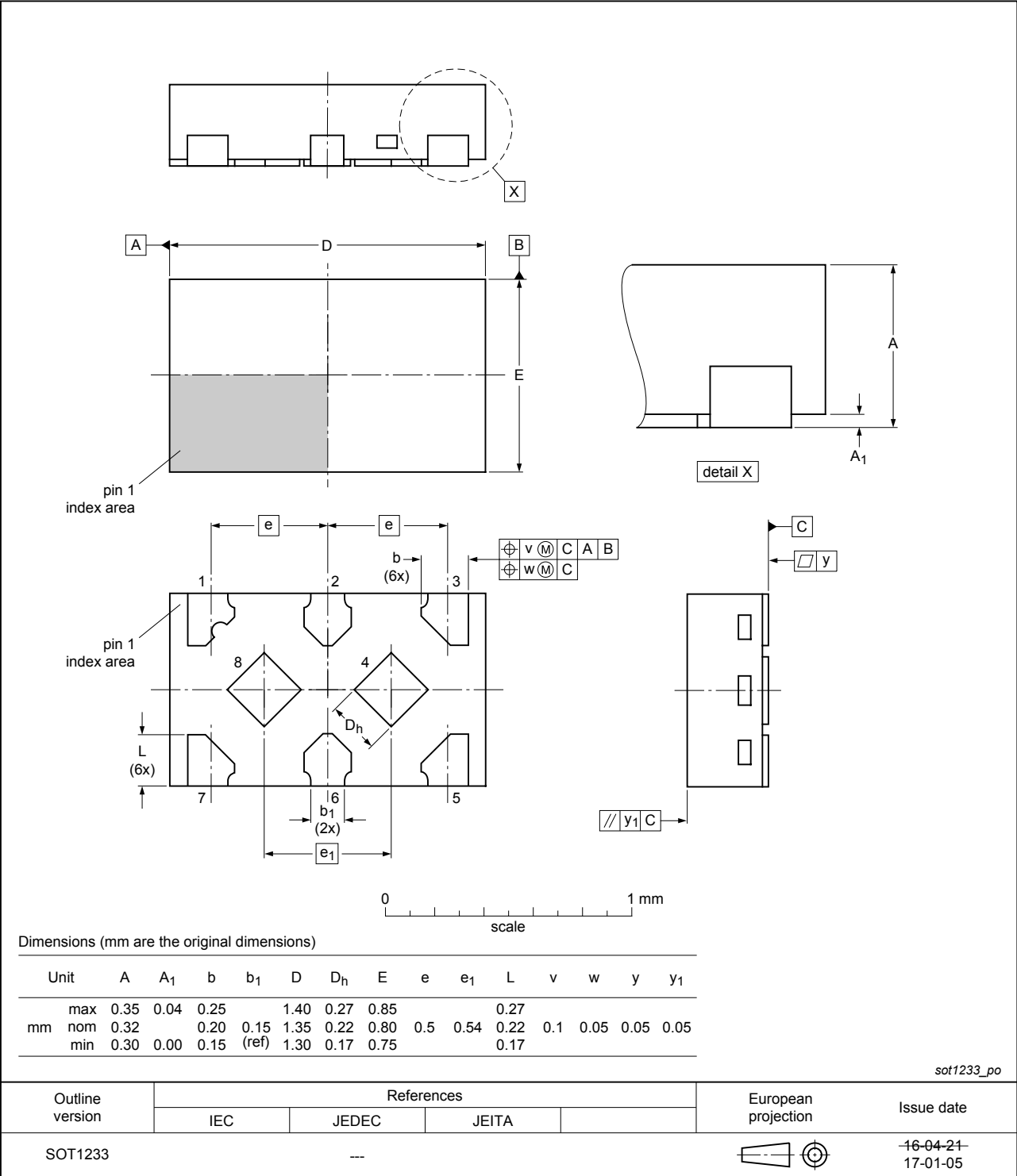


Figure 17. Package outline SOT1233 (X2SON8)

13 Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14 Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC2G86 v.13	20170703	Product data sheet	-	74LVC2G86 v.12
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate. - Added type number 74LVC2G86GX (SOT1233 / X2SON8). - Type number 74LVC2G86GD removed.			
74LVC2G86 v.12	20161215	Product data sheet	-	74LVC2G86 v.11
Modifications:	Table 7: The maximum limits for leakage current and supply current have changed.			
74LVC2G86 v.11	20130408	Product data sheet	-	74LVC2G86 v.10
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74LVC2G86 v.10	20120521	Product data sheet	-	74LVC2G86 v.9
Modifications:	For type number 74LVC2G86GM the sot code has changed to SOT902-2.			
74LVC2G86 v.9	20111125	Product data sheet	-	74LVC2G86 v.8
Modifications:	Legal pages updated.			
74LVC2G86 v.8	20101019	Product data sheet	-	74LVC2G86 v.7
74LVC2G86 v.7	20080613	Product data sheet	-	74LVC2G86 v.6
74LVC2G86 v.6	20080222	Product data sheet	-	74LVC2G86 v.5
74LVC2G86 v.5	20070907	Product data sheet	-	74LVC2G86 v.4
74LVC2G86 v.4	20061013	Product data sheet	-	74LVC2G86 v.3
74LVC2G86 v.3	20050207	Product data sheet	-	74LVC2G86 v.2
74LVC2G86 v.2	20041018	Product specification	-	74LVC2G86 v.1
74LVC2G86 v.1	20030825	Product specification	-	-

15 Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.