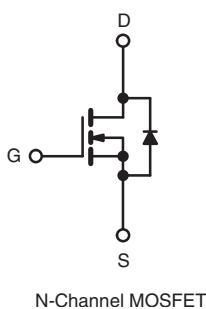
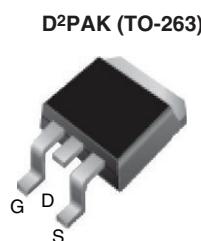


Power MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	100
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V 0.27
Q_g (Max.) (nC)	16
Q_{gs} (nC)	4.4
Q_{gd} (nC)	7.7
Configuration	Single



FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Surface Mount
- Available in Tape and Reel
- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- 175 °C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK (TO-263) is a surface mount power package capable of accommodating die size up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

ORDERING INFORMATION	
Package	D ² PAK (TO-263)
Lead (Pb)-free and Halogen-free	SiHF520S-GE3 SiHF520STRR-GE3 SiHF520STR-GE3
Lead (Pb)-free	IRF520SPbF

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	V_{GS} at 10 V	I_D	9.2 6.5	A
	$T_C = 25$ °C $T_C = 100$ °C			
Pulsed Drain Current ^a		I_{DM}	37	W/°C
Linear Derating Factor			0.40	
Linear Derating Factor (PCB Mount) ^e			0.025	
Single Pulse Avalanche Energy ^b		E_{AS}	200	mJ
Avalanche Current ^a		I_{AR}	9.2	A
Repetitive Avalanche Energy ^a		E_{AR}	6.0	mJ
Maximum Power Dissipation	$T_C = 25$ °C	P_D	60	W
Maximum Power Dissipation (PCB Mount) ^e	$T_A = 25$ °C		3.7	
Peak Diode Recovery dV/dt ^c		dV/dt	5.5	V/ns
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)	For 10 s		300 ^d	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. $V_{DD} = 25$ V, starting $T_J = 25$ °C, $L = 3.5$ mH, $R_g = 25$ Ω , $I_{AS} = 9.2$ A (see fig. 12).

c. $I_{SD} \leq 9.2$ A, $dI/dt \leq 110$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 175$ °C.

d. 1.6 mm from case.

e. When mounted on 1" square PCB (FR-4 or G-10 material).

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	$^{\circ}\text{C/W}$
Maximum Junction-to-Ambient (PCB Mount) ^a	R_{thJA}	-	40	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	2.5	

Note

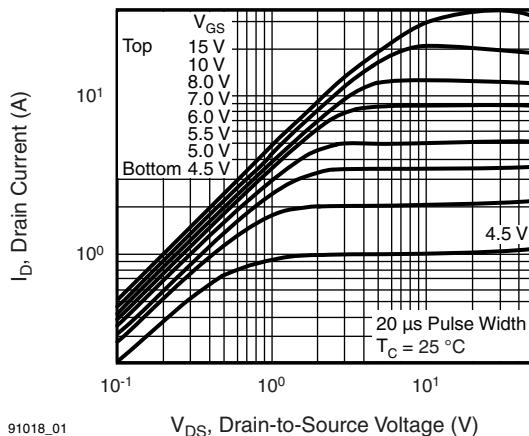
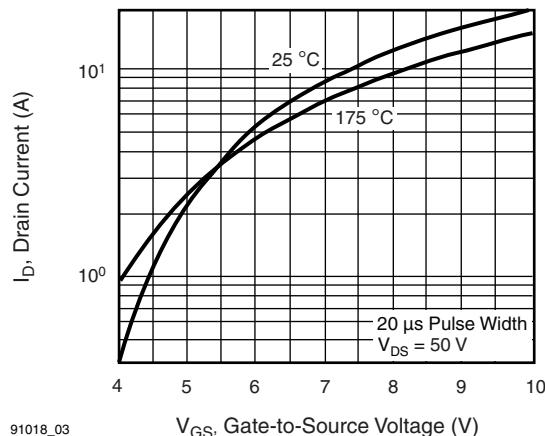
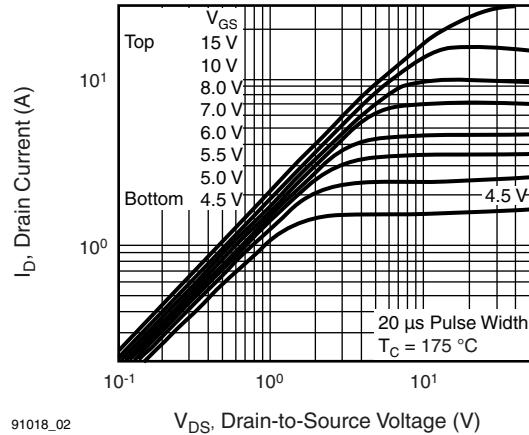
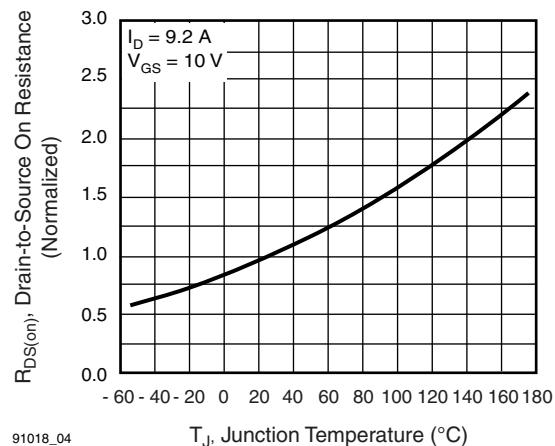
a. When mounted on 1" square PCB (FR-4 or G-10 material).

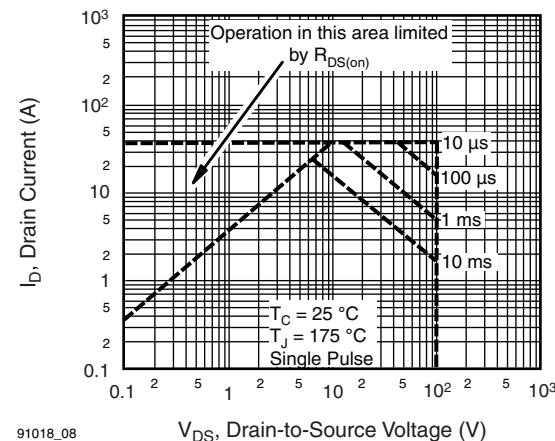
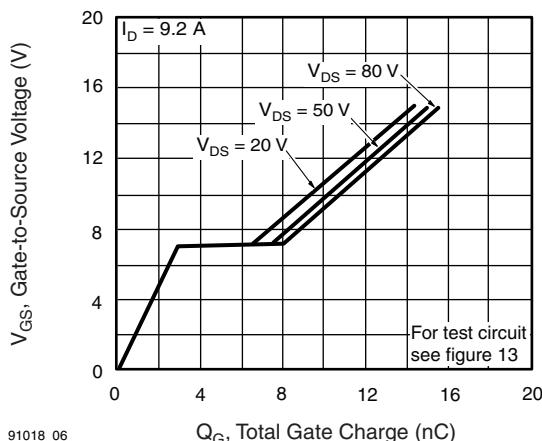
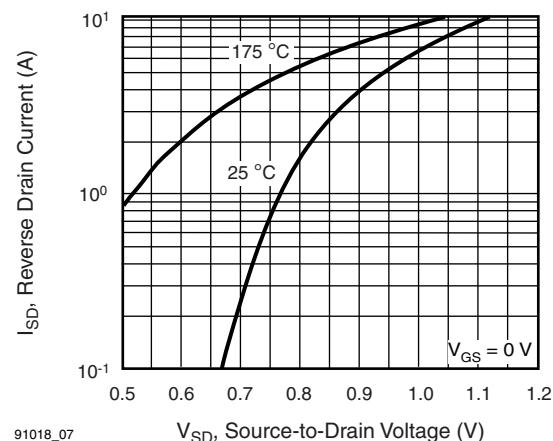
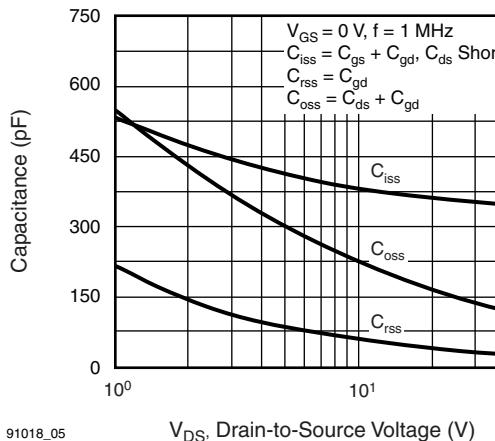
SPECIFICATIONS ($T_J = 25 \text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$, $I_D = 250 \mu\text{A}$		100	-	-	V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25 \text{ }^{\circ}\text{C}$, $I_D = 1 \text{ mA}$		-	0.13	-	$\text{V}/^{\circ}\text{C}$	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$		2.0	-	4.0	V	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100 \text{ V}$, $V_{GS} = 0 \text{ V}$		-	-	25	μA	
		$V_{DS} = 80 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 150 \text{ }^{\circ}\text{C}$		-	-	250		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$	$I_D = 5.5 \text{ A}^b$	-	-	0.27	Ω	
Forward Transconductance	g_{fs}	$V_{DS} = 50 \text{ V}$, $I_D = 5.5 \text{ A}^b$		2.7	-	-	S	
Dynamic								
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}$, $V_{DS} = 25 \text{ V}$, $f = 1.0 \text{ MHz}$, see fig. 5		-	360	-	pF	
Output Capacitance	C_{oss}			-	150	-		
Reverse Transfer Capacitance	C_{rss}			-	34	-		
Total Gate Charge	Q_g	$V_{GS} = 10 \text{ V}$	$I_D = 9.2 \text{ A}$, $V_{DS} = 80 \text{ V}$, see fig. 6 and 13 ^b	-	-	16	nC	
Gate-Source Charge	Q_{gs}			-	-	4.4		
Gate-Drain Charge	Q_{gd}			-	-	7.7		
Turn-On Delay Time	$t_{d(on)}$			-	8.8	-		
Rise Time	t_r	$V_{DD} = 50 \text{ V}$, $I_D = 9.2 \text{ A}$, $R_g = 18 \Omega$, $R_D = 5.2 \Omega$, see fig. 10 ^b		-	30	-	ns	
Turn-Off Delay Time	$t_{d(off)}$			-	19	-		
Fall Time	t_f			-	20	-		
Internal Drain Inductance	L_D			-	4.5	-	nH	
Internal Source Inductance	L_S	Between lead, 6 mm (0.25") from package and center of die contact		-	7.5	-		
Drain-Source Body Diode Characteristics								
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	9.2	A	
Pulsed Diode Forward Current ^a	I_{SM}			-	-	37		
Body Diode Voltage	V_{SD}	$T_J = 25 \text{ }^{\circ}\text{C}$, $I_S = 9.2 \text{ A}$, $V_{GS} = 0 \text{ V}^b$		-	-	1.8	V	
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25 \text{ }^{\circ}\text{C}$, $I_F = 9.2 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}^b$		-	110	260	ns	
Body Diode Reverse Recovery Charge	Q_{rr}			-	0.53	1.3	μC	
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)						

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300 \mu\text{s}$; duty cycle $\leq 2 \%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics, $T_C = 25 \text{ }^\circ\text{C}$

Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Output Characteristics, $T_C = 175 \text{ }^\circ\text{C}$

Fig. 4 - Normalized On-Resistance vs. Temperature



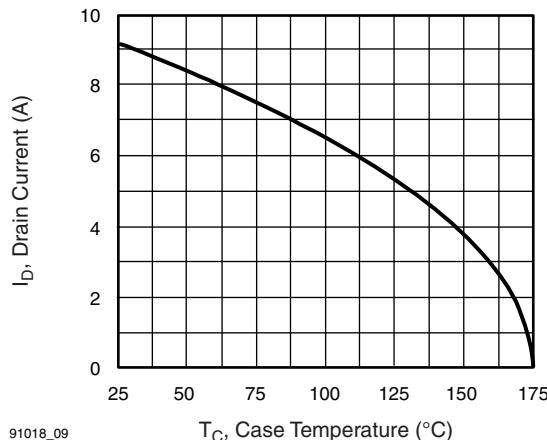


Fig. 9 - Maximum Drain Current vs. Case Temperature

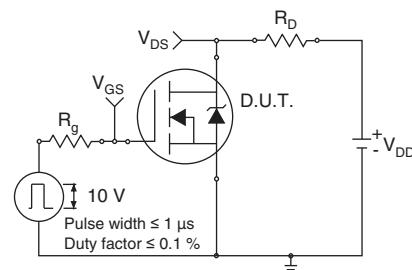


Fig. 10a - Switching Time Test Circuit

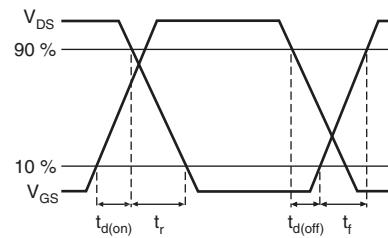


Fig. 10b - Switching Time Waveforms

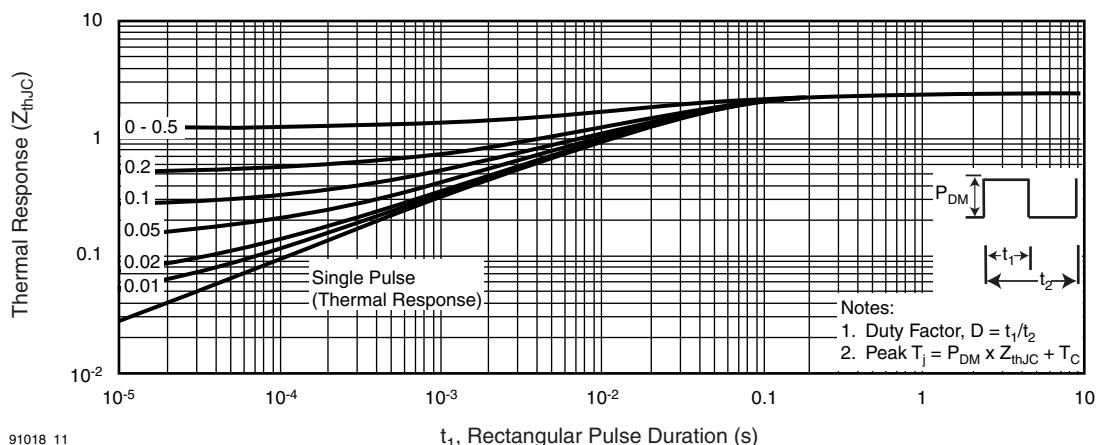


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

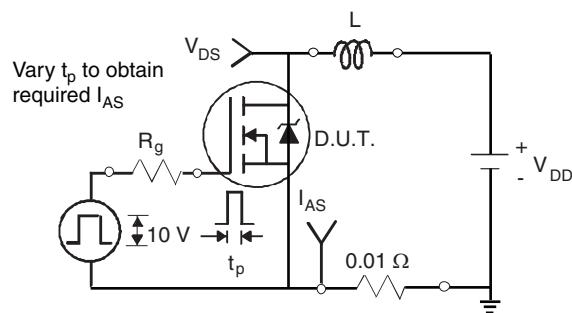


Fig. 12a - Unclamped Inductive Test Circuit

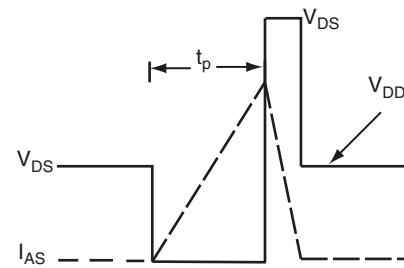


Fig. 12b - Unclamped Inductive Waveforms

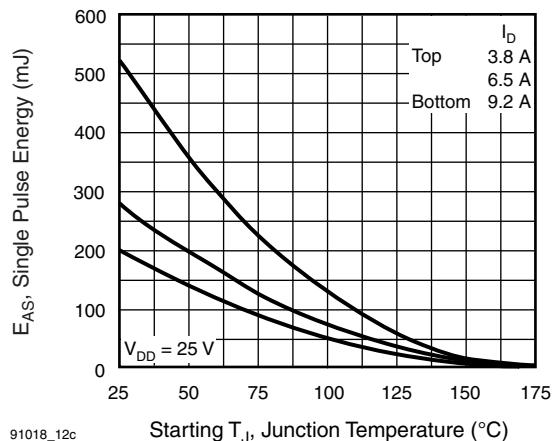


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

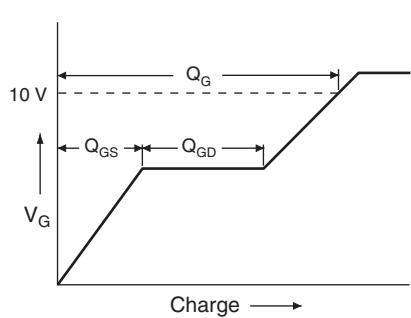


Fig. 13a - Basic Gate Charge Waveform

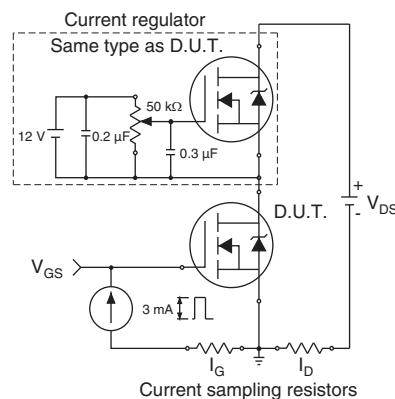
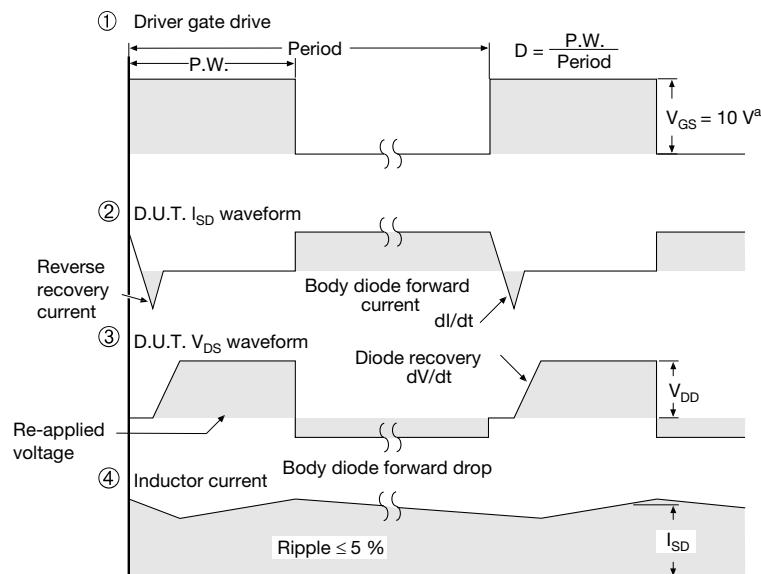
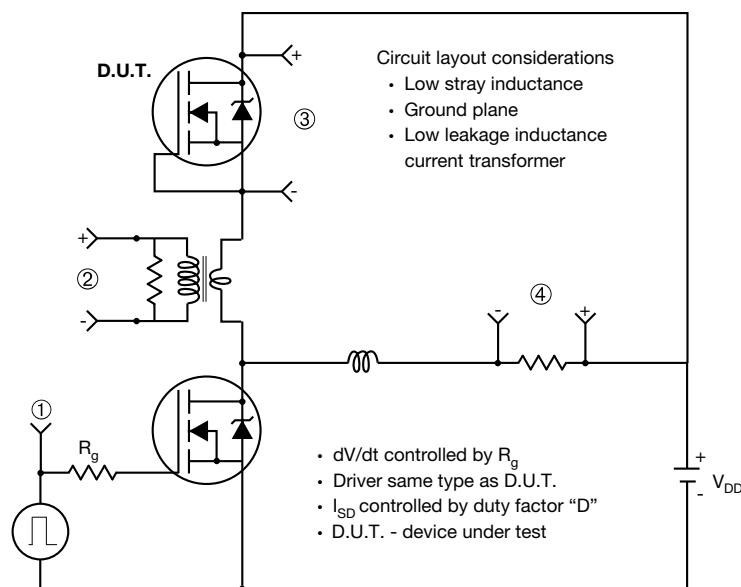


Fig. 13b - Gate Charge Test Circuit

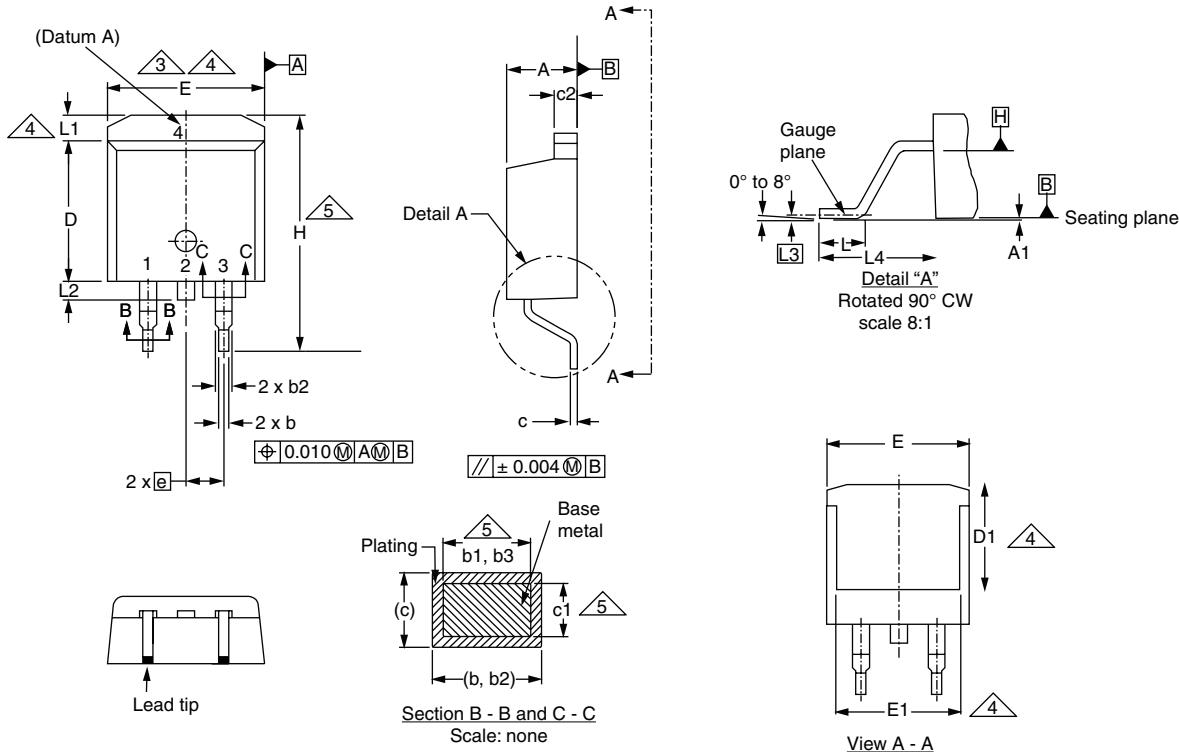
Peak Diode Recovery dV/dt Test Circuit

Note

a. $V_{GS} = 5 \text{ V}$ for logic level devices

Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91018.

TO-263AB (HIGH VOLTAGE)

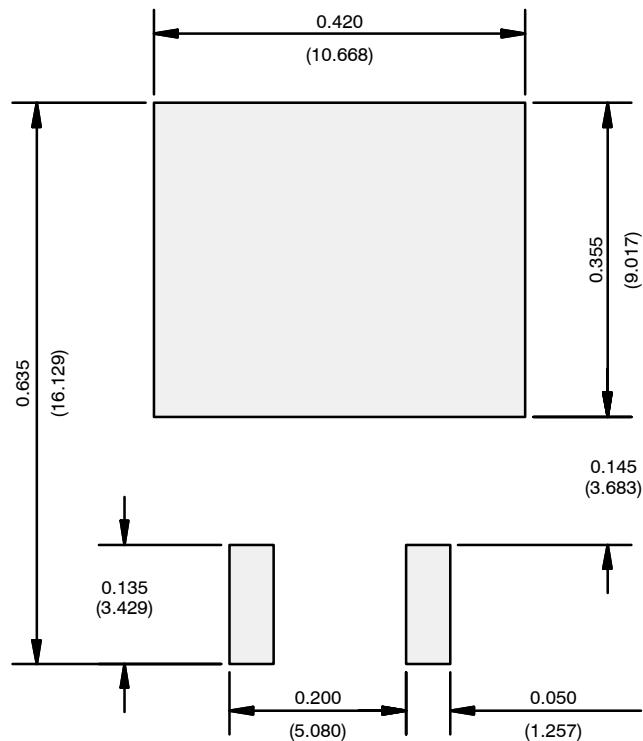


	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead

Recommended Minimum Pads
Dimensions in Inches/(mm)

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