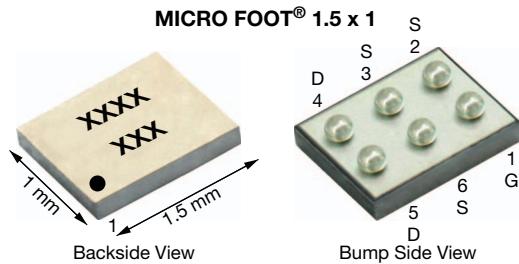


N-Channel 8 V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	R_{DS(on)} (Ω) MAX.	I_D (A) ^d	Q_g (TYP.)
8	0.023 at V _{GS} = 4.5 V	16	17 nC
	0.025 at V _{GS} = 2.5 V	16	
	0.030 at V _{GS} = 1.8 V	16	
	0.040 at V _{GS} = 1.5 V	15	
	0.095 at V _{GS} = 1.2 V	3	


Marking Code: xxxx = 8416

xxx = Date / lot traceability code

Ordering Information:

Si8416DB-T2-E1 (Lead (Pb)-free and halogen-free)

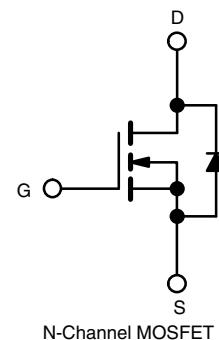
FEATURES

- TrenchFET® power MOSFET
- Ultra-small 1.5 mm x 1 mm maximum outline
- Ultra-thin 0.59 mm maximum height
- Material categorization:
for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Low on-resistance load switch for portable devices
 - Low power consumption, low voltage drop
 - Increased battery life
 - Space Saving on PCB


ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	8	V
Gate-Source Voltage	V _{GS}	± 5	
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	16 ^e	A
	T _C = 70 °C	16 ^e	
	T _A = 25 °C	9.3 ^{a, b}	
	T _A = 70 °C	7.4 ^{a, b}	
Pulsed Drain Current (t = 300 μs)	I _{DM}	20	
Continuous Source-Drain Diode Current	T _C = 25 °C	11	
	T _A = 25 °C	2.3 ^{a, b}	
Maximum Power Dissipation	T _C = 25 °C	13	W
	T _C = 70 °C	8.4	
	T _A = 25 °C	2.77 ^{a, b}	
	T _A = 70 °C	1.77 ^{a, b}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C
Package Reflow Conditions ^c	IR/Convection	260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum Junction-to-Ambient ^{a, f}	R _{thJA}	37	45	°C/W
Maximum Junction-to-Case (Drain) ^g	Steady State	R _{thJC}	7	

Notes

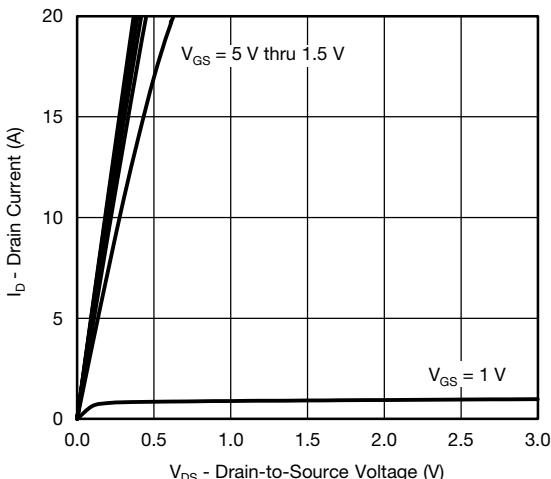
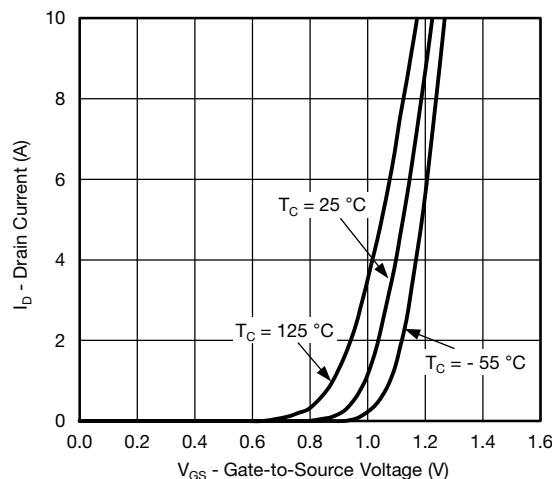
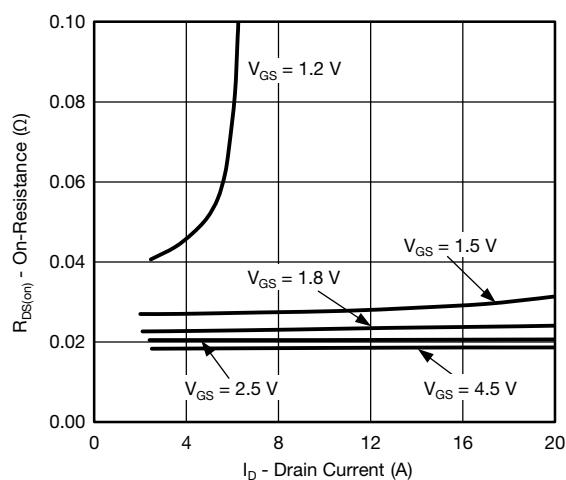
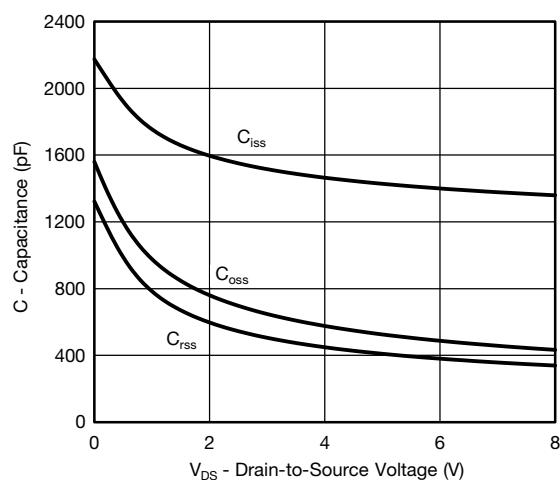
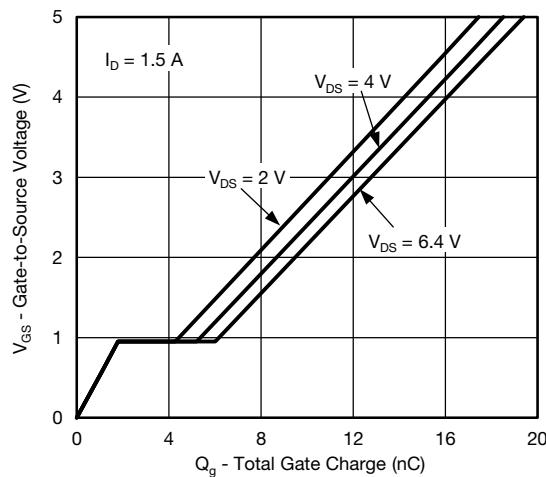
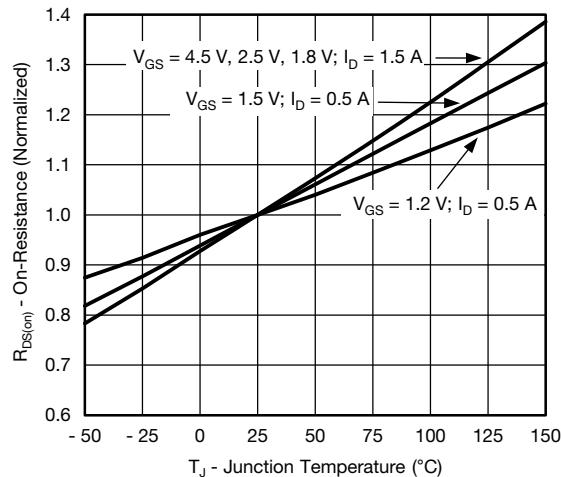
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- Refer to IPC/JEDEC® (J-STD-020), no manual or hand soldering.
- Case is defined as the top surface of the package.
- T_C = 25 °C package limited.
- Maximum under steady state conditions is 85 °C/W.
- Case is defined as top surface of the package.

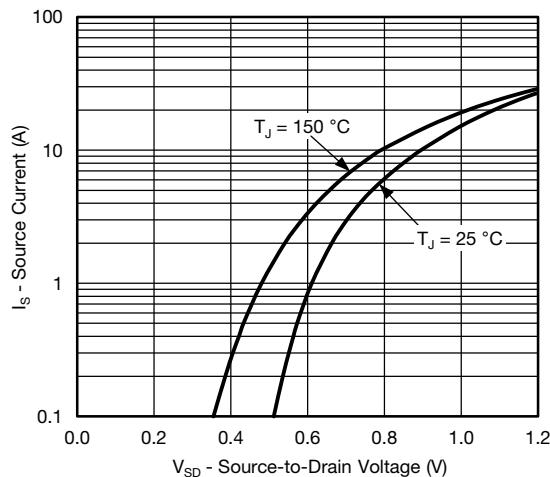
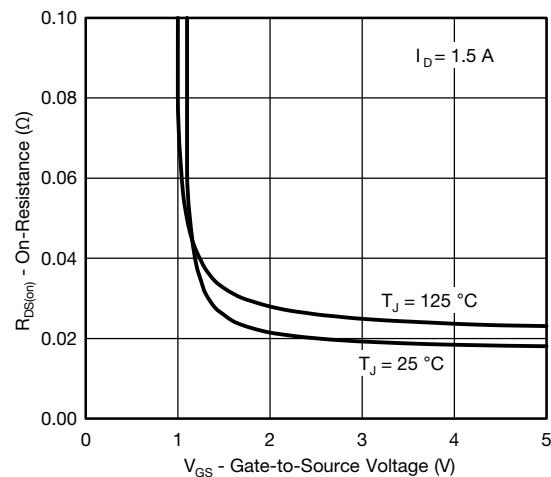
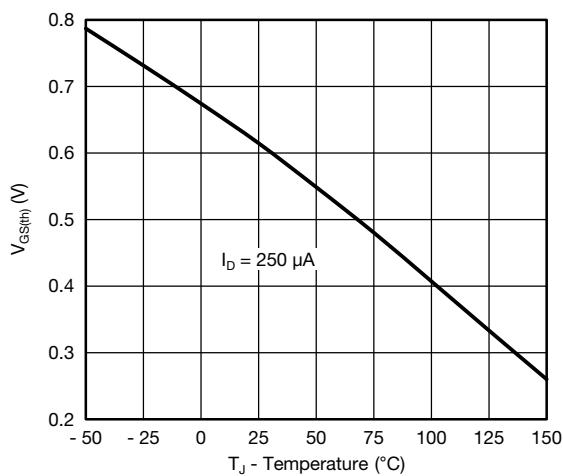
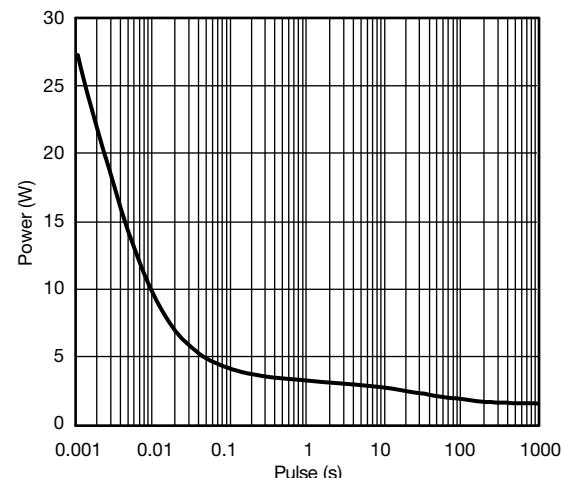
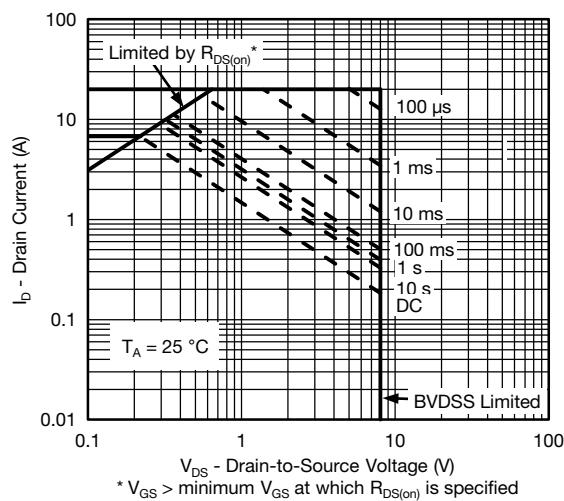
SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$, $I_D = 250 \mu\text{A}$	8	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250 \mu\text{A}$	-	2.2	-	mV/°C
$V_{GS(\text{th})}$ Temperature Coefficient	$\Delta V_{GS(\text{th})}/T_J$		-	-2.7	-	
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	0.35	-	0.80	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 5 \text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 8 \text{ V}$, $V_{GS} = 0 \text{ V}$	-	-	1	μA
		$V_{DS} = 8 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 70^\circ\text{C}$	-	-	10	
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{DS} \geq 5 \text{ V}$, $V_{GS} = 4.5 \text{ V}$	5	-	-	A
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 4.5 \text{ V}$, $I_D = 1.5 \text{ A}$	-	0.019	0.023	Ω
		$V_{GS} = 2.5 \text{ V}$, $I_D = 1 \text{ A}$	-	0.021	0.025	
		$V_{GS} = 1.8 \text{ V}$, $I_D = 1 \text{ A}$	-	0.023	0.030	
		$V_{GS} = 1.5 \text{ V}$, $I_D = 0.5 \text{ A}$	-	0.027	0.040	
		$V_{GS} = 1.2 \text{ V}$, $I_D = 0.5 \text{ A}$	-	0.040	0.095	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 4 \text{ V}$, $I_D = 1.5 \text{ A}$	-	22	-	S
Dynamic ^b						
Input Capacitance	C_{iss}	$V_{DS} = 4 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$	-	1470	-	pF
Output Capacitance	C_{oss}		-	580	-	
Reverse Transfer Capacitance	C_{rss}		-	450	-	
Total Gate Charge	Q_g	$V_{DS} = 4 \text{ V}$, $V_{GS} = 4.5 \text{ V}$, $I_D = 1.5 \text{ A}$	-	17	26	nC
Gate-Source Charge	Q_{gs}		-	1.8	-	
Gate-Drain Charge	Q_{gd}		-	3.4	-	
Gate Resistance	R_g	$V_{GS} = 0.1 \text{ V}$, $f = 1 \text{ MHz}$	-	2.5	-	Ω
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = 4 \text{ V}$, $R_L = 2.7 \Omega$ $I_D \equiv 1.5 \text{ A}$, $V_{GEN} = 4.5 \text{ V}$, $R_g = 1 \Omega$	-	13	25	ns
Rise Time	t_r		-	15	30	
Turn-Off Delay Time	$t_{d(\text{off})}$		-	40	80	
Fall Time	t_f		-	10	20	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$	-	-	20	A
Pulse Diode Forward Current	I_{SM}		-	-	20	
Body Diode Voltage	V_{SD}	$I_S = 1.5 \text{ A}$, $V_{GS} = 0$	-	0.7	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 1.5 \text{ A}$, $dl/dt = 100 \text{ A}/\mu\text{s}$, $T_J = 25^\circ\text{C}$	-	35	70	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	18	35	
Reverse Recovery Fall Time	t_a		-	13	-	ns
Reverse Recovery Rise Time	t_b		-	22	-	

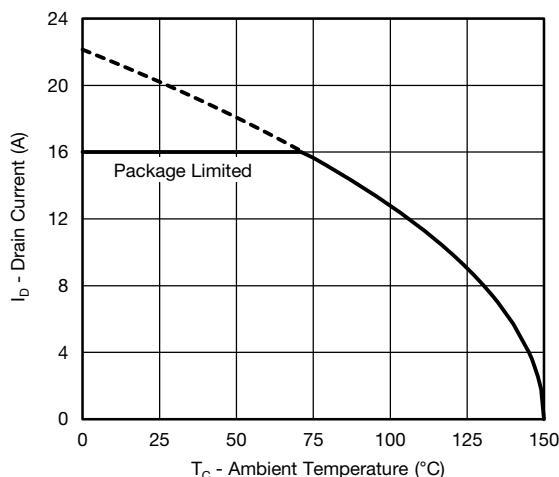
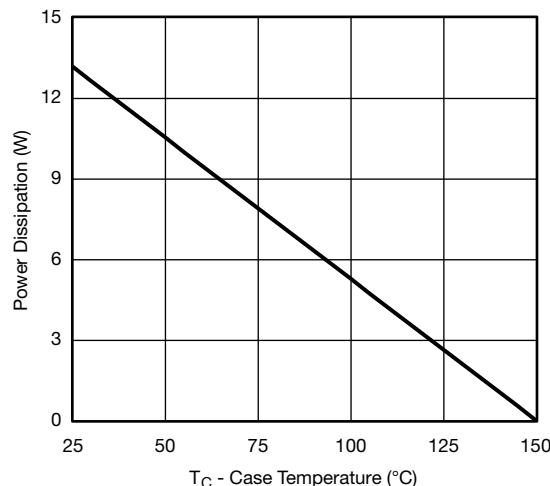
Notes

a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

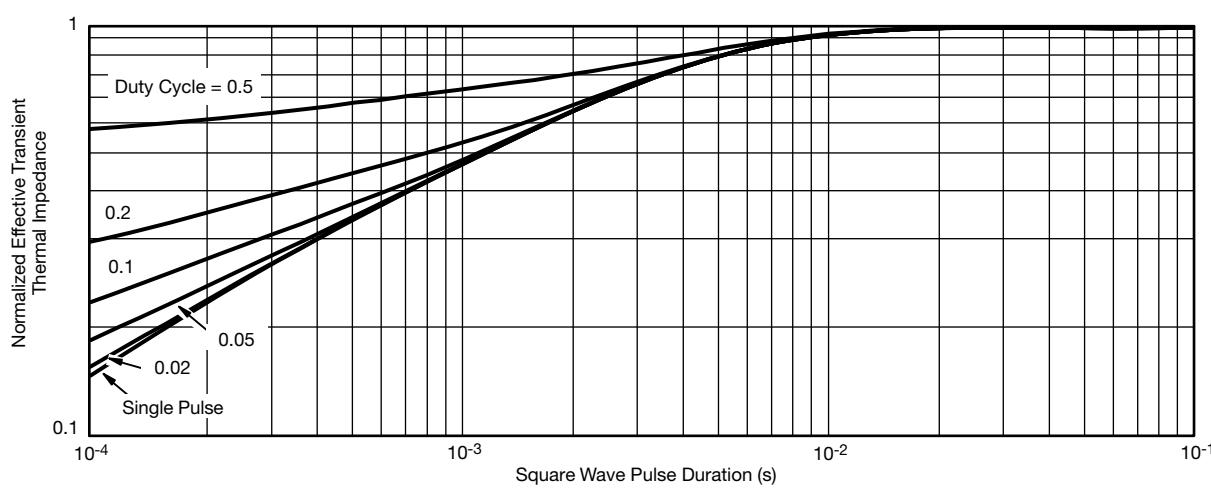
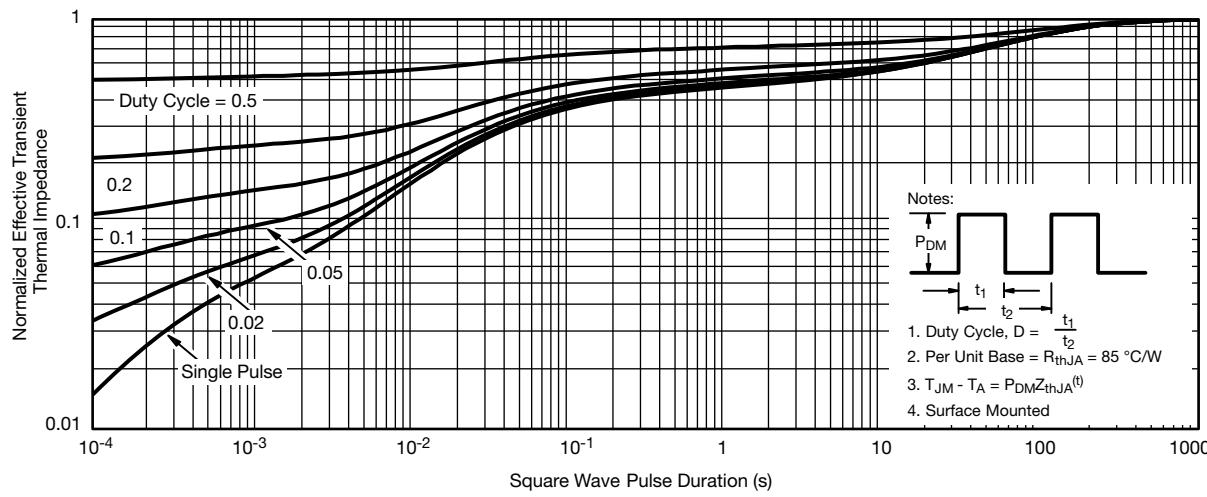
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Single Pulse Power, Junction-to-Ambient

Safe Operating Area, Junction-to-Ambient

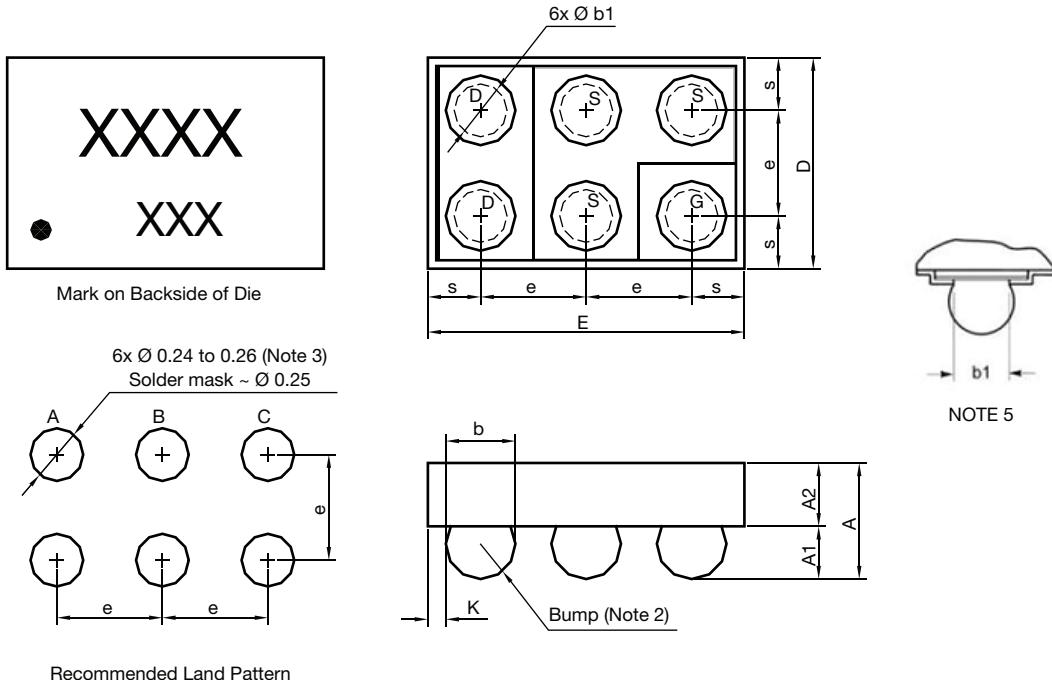
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating*

Power Derating

* The power dissipation P_D is based on T_J (max.) = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63716.

MICRO FOOT®: 6-Bump (1.5 mm x 1 mm, 0.5 mm Pitch, 0.250 mm Bump Height)


Notes

(unless otherwise specified)

1. Six (6) solder bumps are 95.5/3.8/0.7 Sn/Ag/Cu.
2. Backside surface is coated with a Ti/Ni/Ag layer.
3. Non-solder mask defined copper landing pad.
4. Laser marks on the silicon die back.
5. "b1" is the diameter of the solderable substrate surface, defined by an opening in the solder resist layer solder mask defined.
6. • is the location of pin 1

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.510	0.575	0.590	0.0201	0.0226	0.0232
A ₁	0.220	0.250	0.280	0.0087	0.0098	0.0110
A ₂	0.290	0.300	0.310	0.0114	0.0118	0.0122
b	0.297	0.330	0.363	0.0116	0.0129	0.0143
b1	0.250			0.0098		
e	0.500			0.0197		
s	0.210	0.230	0.250	0.0082	0.0090	0.0098
D	0.920	0.960	1.000	0.0362	0.0378	0.0394
E	1.420	1.460	1.500	0.0559	0.0575	0.0591
K	0.028	0.065	0.102	0.0011	0.0025	0.0040

Note

- Use millimeters as the primary measurement.

ECN: T15-0140-Rev. A, 20-Apr-15

DWG: 6035

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