iW1710

Digital PWM Current-Mode Controller for Quasi-Resonant Operation

1.0 Features

- Primary-side feedback eliminates opto-isolators and simplifies design
- Quasi-resonant operation for highest overall efficiency
- ***EZ-EMI*** ® design to easily meet global EMI standards
- Up to 130 kHz switching frequency enables small adapter size
- Very tight output voltage regulation
- No external compensation components required
- Complies with CEC/EPA no-load power consumption and average efficiency regulations
- Built-in output constant-current control with primary-side feedback
- Low start-up current (10 µA typical)
- Built-in soft start
- Built-in short circuit protection and output overvoltage protection
- Optional AC line under/overvoltage protection
- PFM operation at light load
- Current sense resistor short protection
- Overtemperature Protection

2.0 Description

The iW1710 is a high performance AC/DC power supply controller which uses digital control technology to build peak current mode PWM flyback power supplies. The device operates in quasi-resonant mode at heavy load to provide high efficiency along with a number of key built-in protection features while minimizing the external component count, simplifying EMI design and lowering the total bill of material cost. The iW1710 removes the need for secondary feedback circuitry while achieving excellent line and load regulation. It also eliminates the need for loop compensation components while maintaining stability over all operating conditions. Pulse-by-pulse waveform analysis allows for a loop response that is much faster than traditional solutions, resulting in improved dynamic load response. The built-in current limit function enables optimized transformer design in universal off-line applications over a wide input voltage range.

The ultra-low operating current at light load ensures that the iW1710 is ideal for applications targeting the newest regulatory standards for average efficiency and standby power.

3.0 Applications

- Cable/DSL modems, WLAN access points and VOIP gateways.

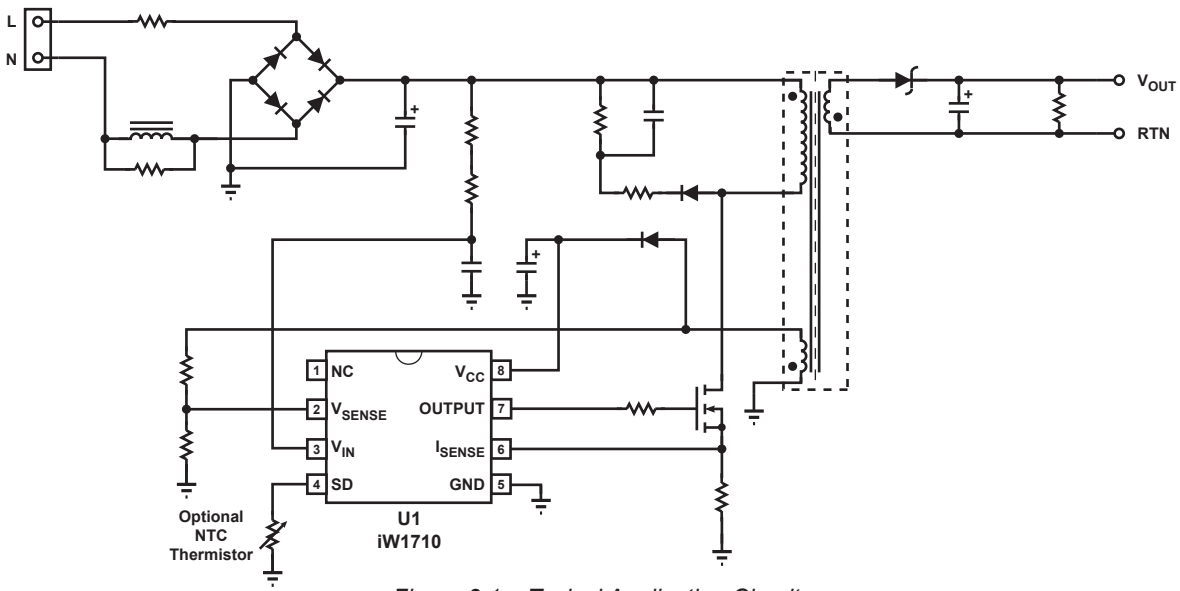
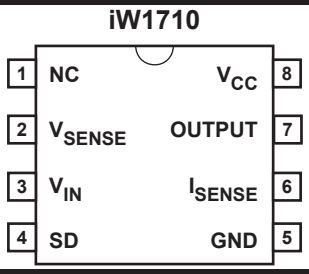


Figure 3.1 : Typical Application Circuit

4.0 Pinout Description



Pin #	Name	Type	Pin Description
1	NC	-	No connection.
2	V_{SENSE}	Analog Input	Auxiliary voltage sense (used for primary side regulation).
3	V_{IN}	Analog Input	Rectified AC line average voltage sense.
4	SD	Analog Input	External shutdown control. Connect to ground through a resistor if not used. (see section 10.16)
5	GND	Ground	Ground.
6	I_{SENSE}	Analog Input	Primary current sense (used for cycle-by-cycle peak current control and limit).
7	OUTPUT	Output	Gate drive for external MOSFET switch.
8	V_{CC}	Power Input	Power supply for control logic and voltage sense for power-on reset circuitry.

5.0 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage if exceeded. For maximum safe operating conditions, refer to Electrical Characteristics in Section 6.0.

Parameter	Symbol	Value	Units
DC supply voltage range (pin 8, I_{CC} = 20mA max)	V_{CC}	-0.3 to 18	V
DC supply current at V_{CC} pin	I_{CC}	20	mA
Output (pin 7)		-0.3 to 18	V
V_{SENSE} input (pin 2, I_{Vsense} ≤ 10 mA)		-0.7 to 4.0	V
V_{IN} input (pin 3)		-0.3 to 18	V
I_{SENSE} input (pin 6)		-0.3 to 4.0	V
SD input (pin 4)		-0.3 to 18	V
Power dissipation at T_A ≤ 25°C	P_D	526	mW
Maximum junction temperature	$T_{J\ MAX}$	125	°C
Storage temperature	T_{STG}	–65 to 150	°C
Thermal Resistance Junction-to-Ambient	θ_{JA}	160	°C/W
ESD rating per JEDEC JESD22-A114		2,000	V
Latch-Up test per JEDEC 78		±100	mA

6.0 Electrical Characteristics

V_{CC} = 12 V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified (Note 1)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{IN} SECTION (Pin 3)						
Start-up low voltage threshold	$V_{INSTLOW}$	T_A= 25°C, positive edge	335	369	406	mV
Start-up current	I_{INST}	V_{IN} = 10 V, C_{VCC} = 10 µF		10	15	µA
Shutdown low voltage threshold	V_{UVDC}	T_A= 25°C, negative edge	201	221	243	mV
Input impedance	Z_{IN}	After start-up		25		kΩ
V_{SENSE} SECTION (Pin 2)						
Input leakage current	I_{BVS}	V_{SENSE} = 2 V			1	µA
Nominal voltage threshold	$V_{SENSE(NOM)}$	T_A=25°C, negative edge	1.523	1.538	1.553	V
Output OVP threshold - 01 (Note 2)	$V_{SENSE(MAX)}$	T_A=25°C, negative edge	1.754	1.846	1.938	V
Output OVP threshold - 11 (Note 2)	$V_{SENSE(MAX)}$	T_A=25°C, negative edge, Load = 100%	1.797	1.892	1.987	V
Output OVP threshold - 21 (Note 2)	$V_{SENSE(MAX)}$	T_A=25°C, negative edge, Load = 100 %	1.836	1.933	2.030	V
OUTPUT SECTION (Pin 7)						
Output low level ON-resistance	$R_{DS(ON)LO}$	I_{SINK} = 5 mA		40		Ω
Output high level ON-resistance	$R_{DS(ON)-HP}$	I_{SOURCE} = 5 mA		75		Ω
Rise time (Note 2)	t_R	T_A = 25°C, C_L = 330 pF 10% to 90%		200	300	ns
Fall time (Note 2)	t_F	T_A = 25°C, C_L = 330 pF 90% to 10%		40	60	ns
Maximum switching frequency -01, -11, -21 (Note 3)	$f_{SW(MAX)}$	Any combination of line and load		130	140	kHz
V_{CC} SECTION (Pin 8)						
Maximum operating voltage (Note 2)	$V_{CC(MAX)}$				16	V
Start-up threshold	$V_{CC(ST)}$	V_{CC} rising	10.8	12	13.2	V
Undervoltage lockout threshold	$V_{CC(UVL)}$	V_{CC} falling	5.5	6.0	6.6	V
Operating current	I_{CCQ}	C_L = 330 pF, V_{SENSE} = 1.5 V		3.5	5	mA

6.0 Electrical Characteristics (cont.)

V_{CC} = 12 V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified (Note 1)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
I_{SENSE} SECTION (Pin 6)						
Peak limit threshold	V_{PEAK}		1.045	1.1	1.155	V
Isense short protection reference	V_{RSNS}		0.127	0.15	0.173	V
CC regulation threshold limit (Note 2)	V_{REG-TH}			1.0		V
SD SECTION (Pin 4)						
Shutdown threshold	V_{SD-TH}	T_A = 25°C	0.95	1.0	1.05	V
Shutdown threshold in Startup (Note 2)	$V_{SD-TH(ST)}$			1.2		V
Input leakage current	I_{BVSD}	V_{SD} = 1.0 V			1	µA
Pull down resistance	R_{SD}	T_A = 25°C	7916	8333	8750	Ω
Pull up current source	I_{SD}	T_A = 25°C	96	107	118	µA

Notes:

Note 1. Adjust V_{CC} above the start-up threshold before setting at 12 V.

Note 2. These parameters are not 100% tested, guaranteed by design and characterization.

Note 3. Operating frequency varies based on the line and load conditions, see Theory of Operation for more details.

7.0 Typical Performance Characteristics

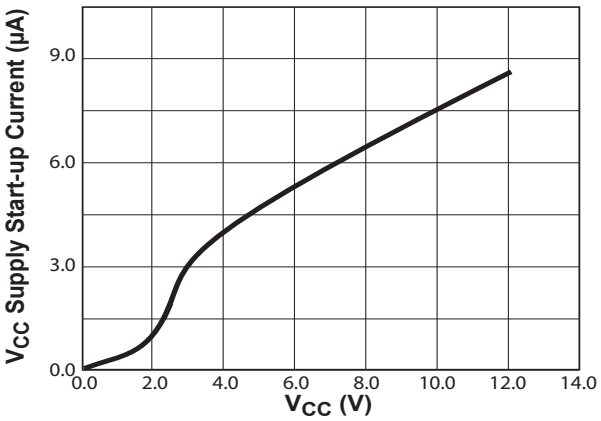


Figure 7.1 : V_{CC} vs. V_{CC} Supply Start-up Current

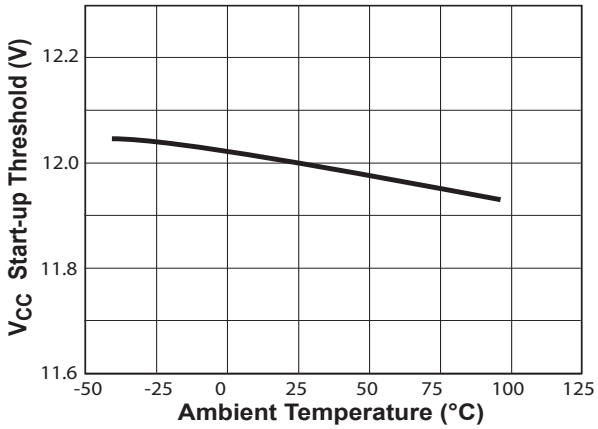


Figure 7.2 : Start-Up Threshold vs. Temperature

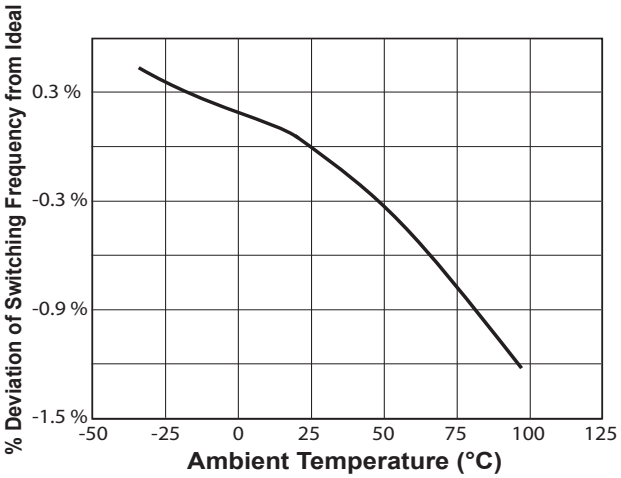


Figure 7.3 : % Deviation of Switching Frequency to Ideal Switching Frequency vs. Temperature

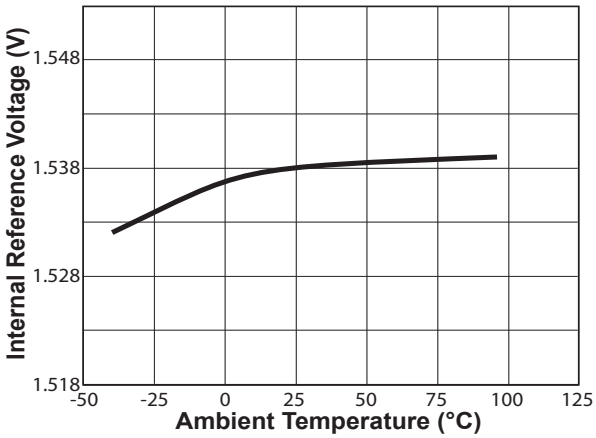


Figure 7.4 : Internal Reference vs. Temperature

8.0 Functional Block Diagram

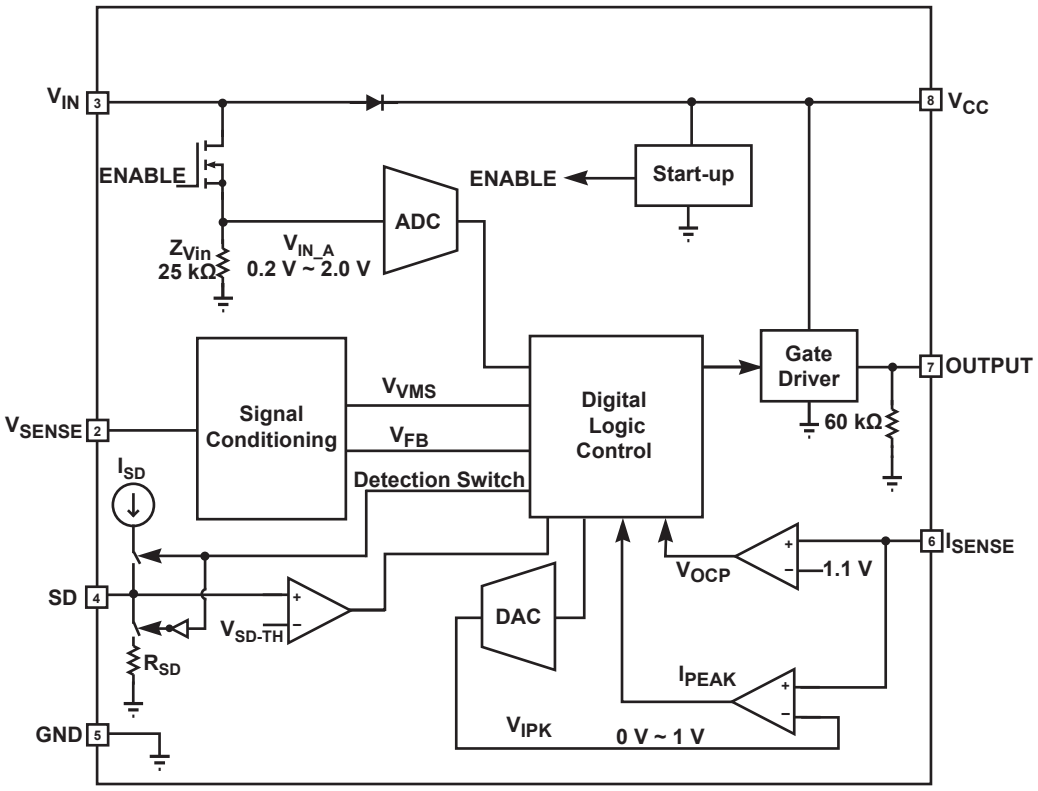


Figure 8.1 : iW1710 Functional Block Diagram

9.0 Theory of Operation

The iW1710 is a digital controller which uses a proprietary primary-side control technology to eliminate the opto-isolated feedback and secondary regulation circuits required in traditional designs. This results in a low-cost solution for AC/DC adapters. The iW1710 uses Critical Discontinuous Conduction Mode (CDCM) or Pulse Width Modulation (PWM) mode at high output power levels and switches to Pulse Frequency Modulation (PFM) mode at light load to minimize power dissipation to meet EPA 2.0 specification. Furthermore, iWatt's digital control technology enables fast dynamic response, tight output regulation, and full featured circuit protection with primary-side control.

Referring to the block diagram in Figure 8.1, the digital logic control block generates the switching on-time and off-time information based on the line voltage and the output voltage feedback signal and provides commands to dynamically control the external MOSFET current. The system loop is compensated internally by a digital error amplifier. Adequate system phase and gain margin are guaranteed by design and no external analog components are required for loop compensation. The iW1710 uses an advanced digital control algorithm to reduce system design time and improve reliability.

Furthermore, accurate secondary constant-current operation is achieved without the need for any secondary-side sense and control circuits.

The built-in protection features include overvoltage protection (OVP), output short circuit protection (SCP) and soft-start, AC line brown out, overcurrent protection, and Isense fault protection. Also the iW1710 automatically shuts down if it detects any of its sense pins to be either open or short.

iWatt's digital control scheme is specifically designed to address the challenges and trade-offs of power conversion design. This innovative technology is ideal for balancing new regulatory requirements for green mode operation with more practical design considerations such as lowest possible cost, smallest size and highest performance output control.

9.1 Pin Detail

Pin 2 – V_{SENSE}

Sense signal input from auxiliary winding. This provides the secondary voltage feedback used for output regulation.

Pin 3 – V_{IN}

Sense signal input from the rectified line voltage. V_{IN} is used for line regulation. The input line voltage is scaled down using a resistor network. It is used for input undervoltage and overvoltage protection. This pin also provides the supply current to the IC during start-up.

Pin 4 – SD

External shutdown control. If the shutdown control is not used, this pin should be connected to GND via a resistor. (see Section 10.16).

Pin 5 – GND

Ground.

Pin 6 – I_{SENSE}

Primary current sense. Used for cycle by cycle peak current control.

Pin 7 – OUTPUT

Gate drive for the external MOSFET switch.

Pin 8 – V_{CC}

Power supply for the controller during normal operation. The controller will start up when V_{CC} reaches 12 V (typical) and will shut-down when the V_{CC} voltage is below 6 V (typical). A decoupling capacitor should be connected between the V_{CC} pin and GND.

9.2 Start-up

Prior to start-up the V_{IN} pin charges up the V_{CC} capacitor through the diode between V_{IN} and V_{CC} (see Figure 8.1).

When V_{CC} is fully charged to a voltage higher than the start-up threshold $V_{CC(ST)}$, the ENABLE signal becomes active and enables the control logic; the V_{IN} switch turns on, and the analog-to-digital converter begins to sense the input voltage. Once the voltage on the V_{IN} pin is above $V_{INSTLOW}$, the iW1710 commences soft start function. An adaptive soft-start control algorithm is applied at startup state, during which the initial output pulses will be small and gradually get larger until the full pulse width is achieved. The peak current is limited cycle by cycle by Ipeak comparator.

If at any time the V_{CC} voltage drops below $V_{CC(UVL)}$ threshold then all the digital logic is reset. At this time V_{IN} switch turns off so that the V_{CC} capacitor can be charged up again towards the start-up threshold.

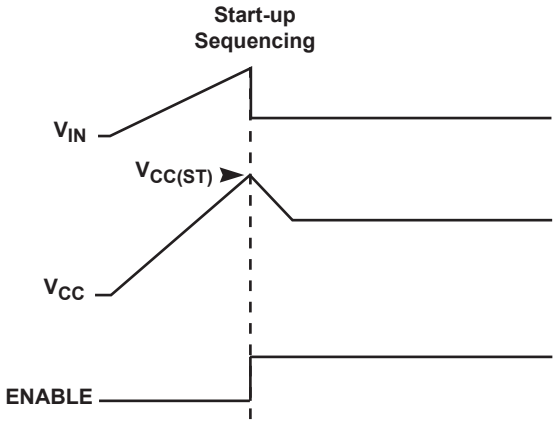


Figure 9.1 : Start-up Sequencing Diagram

9.3 Understanding Primary Feedback

Figure 9.2 illustrates a simplified flyback converter. When the switch Q1 conducts during $t_{ON}(t)$, the current $i_g(t)$ is directly drawn from rectified sinusoid $v_g(t)$. The energy $E_g(t)$ is stored in the magnetizing inductance L_M. The rectifying diode D1 is reverse biased and the load current I_O is supplied by the secondary capacitor C_O. When Q1 turns off, D1 conducts and the stored energy $E_g(t)$ is delivered to the output.

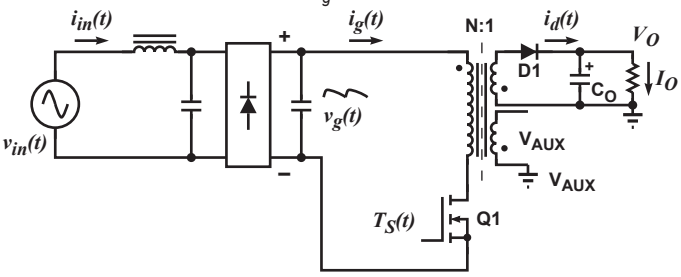


Figure 9.2 : Simplified Flyback Converter

In order to tightly regulate the output voltage, the information about the output voltage and load current needs to be accurately sensed. In the DCM flyback converter, this information can be read via the auxiliary winding. During the Q_1 on-time, the load current is supplied from the output filter capacitor C_O. The voltage across L_M is $v_g(t)$, assuming the voltage dropped across Q_1 is zero. The current in Q_1 ramps up linearly at a rate of:

$$\frac{di_g(t)}{dt} = \frac{v_g(t)}{L_M} \qquad (9.1)$$

At the end of on-time, the current has ramped up to:

$$i_{g\_peak}(t_{ON}) = \frac{v_g(t) \times t_{ON}}{L_M} \quad (9.2)$$

This current represents a stored energy of:

$$E_g = \frac{L_M}{2} \times i_{g\_peak}(t_{ON})^2 \quad (9.3)$$

When Q_1 turns off, $i_g(t)$ in L_M forces a reversal of polarities on all windings. Ignoring the communication-time caused by the leakage inductance L_K at the instant of turn-off, the primary current transfers to the secondary at a peak amplitude of:

$$i_d(t) = \frac{N_P}{N_S} \times i_{g\_peak}(t_{ON}) \quad (9.4)$$

Assuming the secondary winding is master and the auxiliary winding is slave.

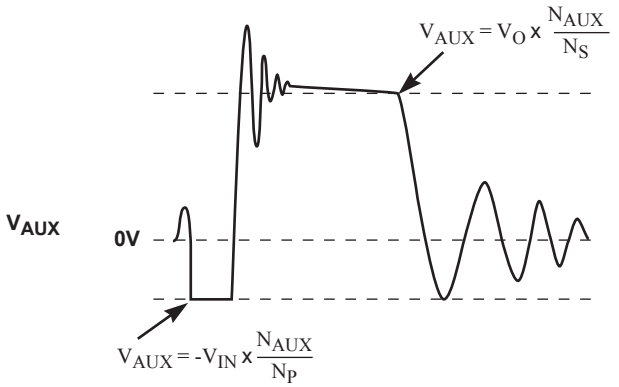


Figure 9.3 : Auxiliary Voltage Waveforms

The auxiliary voltage is given by:

$$V_{AUX} = \frac{N_{AUX}}{N_S}(V_O + \Delta V) \quad (9.5)$$

and reflects the output voltage as shown in Figure 9.3.

The voltage at the load differs from the secondary voltage by a diode drop and IR losses. The diode drop is a function of current, as are IR losses. Thus, if the secondary voltage is always read at a constant secondary current, the difference between the output voltage and the secondary voltage will be a fixed ΔV. Furthermore, if the voltage can be read when the secondary current is small; for example, at the knee of the auxiliary waveform (see Figure 9.3), then ΔV will also be small. With the iW1710, ΔV can be ignored.

The real-time waveform analyzer in the iW1710 reads the auxiliary waveform information cycle by cycle. The part then generates a feedback voltage V_{FB}. The V_{FB} signal precisely represents the output voltage and is used to regulate the output voltage.

9.4 Constant Voltage Operation

After soft-start has been completed, the digital control block measures the output conditions. It determines output power levels and adjusts the control system according to a light load or a heavy load. If this is in the normal range, the device operates in the Constant Voltage (CV) mode, and changes the pulse width (T_{ON}), and off time (T_{OFF}) in order to meet the output voltage regulation requirements. During this mode the PWM switching frequency is between 30 kHz and 130 kHz, depending on the line and load conditions.

If less than 0.2 V is detected on V_{SENSE} it is assumed that the auxiliary winding of the transformer is either open or shorted and the iW1710 shuts down.

9.5 Dynamic Load Transient

There are three components that compose the voltage drop during a load transient event.

$V_{DROP(cable)}$ is the drop in voltage due to the increased current going through the connector and/or the cable.

$$V_{DROP(cable)} = R_{CABLE} \times \Delta I_{OUT} \quad (9.6)$$

The second component which affects the voltage drop during load transient is $V_{DROP(sense)}$. This voltage drop is the drop in voltage before the V_{SENSE} signal is able to show a significant drop in output voltage. This is determined by V_{min} or the reference voltage at which a load transient is detected. The smaller the V_{min} is the smaller this drop in voltage is.

$$V_{DROP(sense)} = \left(V_{SENSE(nom)} - V_{SENSE(\min)}\right) \times \frac{V_{OUT(PCB)}}{V_{SENSE(nom)}} \quad (9.7)$$

Keep in mind that a smaller V_{min} is less tolerant of noise and distortions in V_{SENSE} than a larger one.

The final drop in voltage is due to the time from when V_{SENSE} drops V_{min} to when the next V_{SENSE} signal appears. In the worst case condition this is how much voltage drops during the longest switching period.

$$V_{DROP(IC)} = \frac{I_{OUT} \times T_{P(\text{No load})}}{C_{OUT}} \quad (9.8)$$

A larger output capacitance in this case greatly reduces the $V_{DROP(IC)}$.

When the iW1710 detects the output voltage to be significantly higher than the nominal output voltage, the device begins to increase the switching period which lowers the output voltage. $T_{PERIOD(CLAMP)}$ refers to the maximum switching period to which the iW1710 increases to when an output voltage is detected to be significantly over the nominal.

During fast load changes the output voltage may not have time to settle before the load is changed. Thus for this case when the power supply goes from light load to heavy load prior to output voltage settling $T_{PERIOD(CLAMP)}$ substitutes $T_{PERIOD(PFM)}$ in equation 9.8.

9.6 Valley Mode Switching

In order to reduce switching losses in the MOSFET and EMI, the iW1710 employs valley mode switching when I_{OUT} is above 50%. In valley mode switching, the MOSFET switch is turned on at the point where the resonant voltage across the drain and source of the MOSFET is at its lowest point (see Figure 9.4). By switching at the lowest V_{DS}, the switching loss will be minimized.

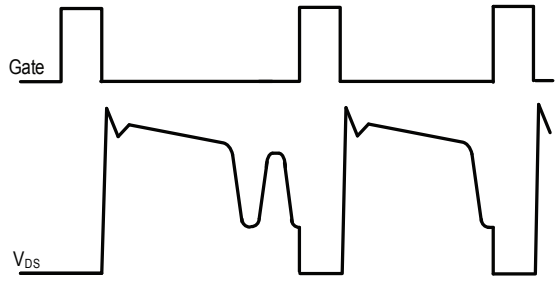


Figure 9.4 : Valley Mode Switching

Turning on at the lowest V_{DS} generates lowest dV/dt, thus valley mode switching can also reduce EMI. To limit the switching frequency range, the iW1710 can skips valleys (seen in the first cycle in Figure 9.4) when the switching frequency becomes too high.

iW1710 provides valley mode switching during constant output current operation. So, the EMI and switching losses are still minimized during CC mode. This feature is superior to other quasi-resonant technologies which only support valley mode switching during constant voltage operation. This is beneficial to applications, such as chargers, where the power supply mainly operates in CC mode.

9.7 Constant Current Operation

The constant current mode (CC mode) is useful in battery charging applications. During this mode of operation the iW1710 will regulate the output current at a constant level regardless of the output voltage, while avoiding continuous conduction mode.

To achieve this regulation the iW1710 senses the load current indirectly through the primary current. The primary current is detected by the I_{SENSE} pin through a resistor from the MOSFET source to ground.

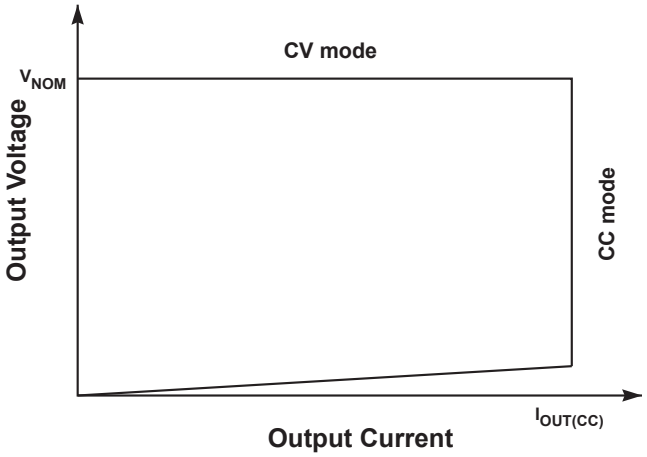


Figure 9.5 : Power Envelope

9.8 PFM Mode at Light Load

The iW1710 normally operates in a fixed frequency PWM or critical discontinuous conduction mode when I_{OUT} is greater than approximately 10% of the specified maximum load current. As the output load I_{OUT} is reduced, the on-time t_{ON} is decreased. At the moment that the load current drops below 10% of nominal, the controller transitions to Pulse Frequency Modulation (PFM) mode. Thereafter, the on-time will be modulated by the line voltage and the off-time is modulated by the load current. The device automatically returns to PWM mode when the load current increases.

9.9 Variable Frequency Operation

At each of the switching cycles, the falling edge of V_{SENSE} will be checked. If the falling edge of V_{SENSE} is not detected, the off-time will be extended until the falling edge of V_{SENSE} is detected. The maximum allowed transformer reset time is 120 µs. When the transformer reset time reaches this maximum reset time, the iW1710 immediately shuts off.

9.10 Internal Loop Compensation

The iW1710 incorporates an internal Digital Error Amplifier with no requirement for external loop compensation. For a typical power supply design, the loop stability is guaranteed to provide at least 45 degrees of phase margin and –20dB of gain margin.

9.11 Voltage Protection Functions

The iW1710 includes functions that protect against input line undervoltage (UV) and the output overvoltage (OVP).

The input voltage is monitored by the V_{IN} pin and the output voltage is monitored by the V_{SENSE} pin. If the voltage at these pins exceed their respective undervoltage or overvoltage thresholds the iW1710 shuts down immediately. However, the IC remains biased which discharges the V_{CC} supply. Once V_{CC} drops below the UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting start-up until the fault condition is removed.

9.12 PCL, OC and SRS Protection

Peak-current limit (PCL), over-current protection (OCP) and sense-resistor short protection (SRSP) are features built-into the iW1710. With the I_{SENSE} pin the iW1710 is able to monitor the primary peak current. This allows for cycle by cycle peak current control and limit. When the primary peak current multiplied by the I_{SENSE} sense resistor is greater than 1.1 V over current is detected and the IC will immediately turn off the gate drive until the next cycle. The output driver will send out switching pulse in the next cycle, and the switching pulse will continue if the OCP threshold is not reached; or, the switching pulse will turn off again if the OCP threshold is still reached.

If the I_{SENSE} sense resistor is shorted there is a potential danger of the over current condition not being detected. Thus the IC is designed to detect this sense-resistor-short fault after the start up, and shutdown immediately. The V_{CC} will be discharged since the IC remains biased. Once V_{CC} drops below the UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting start-up, but does not fully start-up until the fault condition is removed.

9.13 Shutdown

The shutdown (SD) pin in the iW1710 provides protection against overtemperature (OTP) and additional overvoltage (OVP) for the power supply.

The iW1710 switches between monitoring overtemperature fault and overvoltage fault. In order to detect the resistance in the NTC for an overtemperature fault, the iW1710 connects a current source to the SD pin and checks the voltage on the pin. To ensure that the current source is settled before the voltage is checked both OTP and OVP are detected on the last cycle, as depicted in figure 9.6.

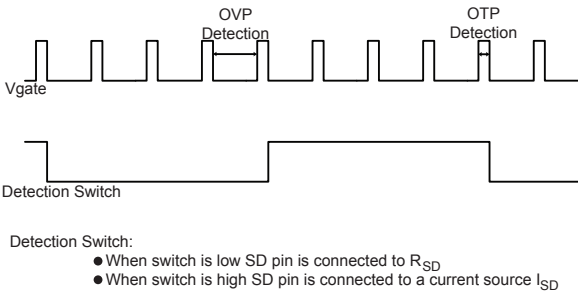


Figure 9.6 : SD Pin Detection Cycles

During an overvoltage monitor cycle the SD pin is connected to a resistance internal to the chip, R_{SD}, to ground and the voltage on the SD pin is observed.

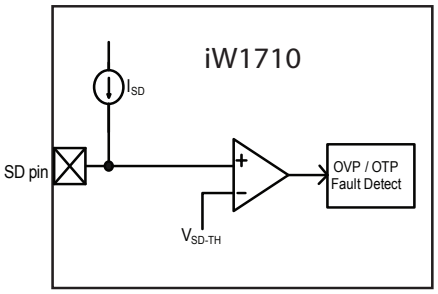


Figure 9.7 : Internal Function of SD Pin

10.0 Design Example

10.1 Design Procedure

This design example gives the procedure for a flyback converter using iW1710. Refer to Figure 12.1 for the application circuit. The design objectives for this adapter are given in table 10.1. It meets UL, IEC, and CEC requirements.

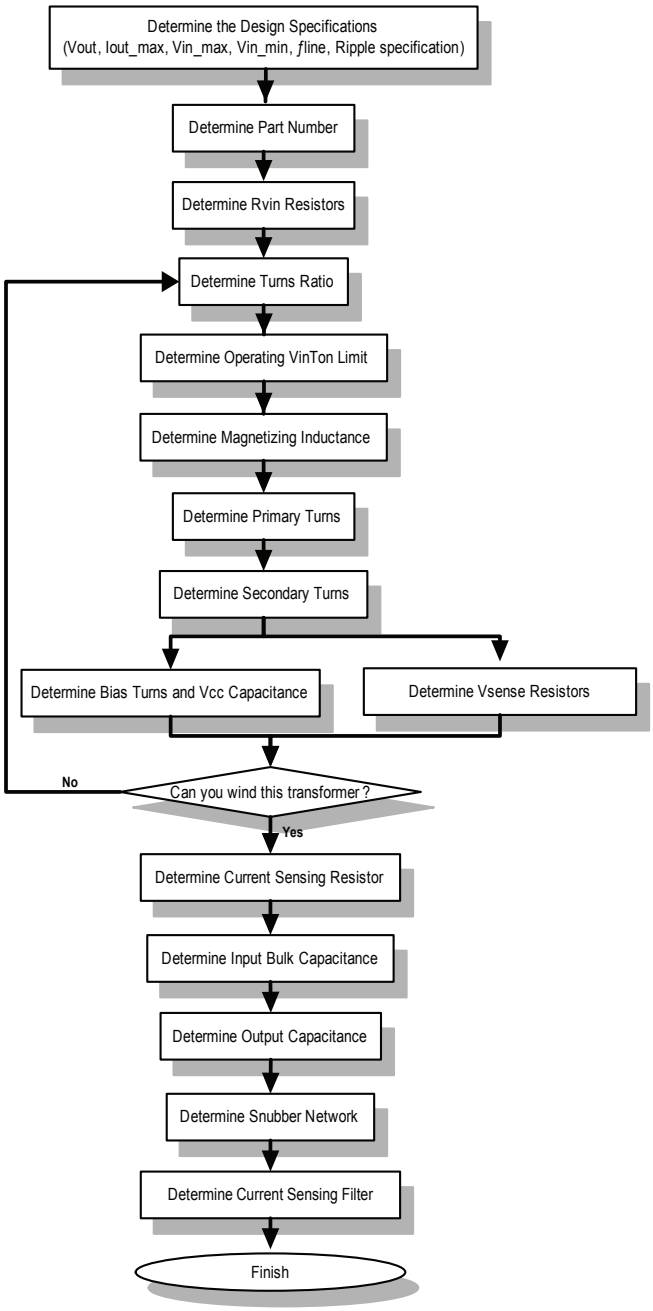


Figure 10.1 : iW1710 Design Flow Chart

Parameter	Symbol	Range
Input Voltage	V_{IN}	85 - 264 V_{RMS}
Frequency	f_{IN}	47 - 64 Hz
No Load Input	P_{IN}	100 mW
Output Voltage	$V_{OUT(Cable)}$	12.0 V
Output Current	I_{OUT}	1.2 A
Output Ripple	V_{RIPPLE}	< 100 mV
Power Out	P_{OUT}	15 W
EPA 2.0 Efficiency	η	80%

Table 10.1 : iW1710 Design Specification Table

10.2 Determine Part Number

Based on design specifications, choose the most suitable part for the design. For more information on the options see section 14.0.

Use equation 10.1 for V_{OUT} in the following calculations, where V_{FD} is the forward voltage of the output diode.

$$V_{OUT} = V_{OUT(Cable)} + V_{CableDrop} + V_{FD} \qquad (10.1)$$

For this example there is no cable so $V_{CableDrop}$ is 0 V , assuming V_{FD} is 0.5, V_{OUT} is:

$$V_{OUT} = 12.0V + 0V + 0.5V = 12.5V$$

10.3 Input Selection

V_{IN} resistors are chosen primarily to scale down the input voltage for the IC. The default scale factor for the input voltage in the IC is 0.0043 and the internal impedance of this pin is Z_{IN} (25 kΩ). Therefore, the V_{IN} resistors should equate to:

$$R_{Vin} = \frac{Z_{IN}}{0.0043} - Z_{IN} \qquad (10.2)$$

From equation 10.2, ideally R_{Vin} should be 5.79 MΩ. A lower value of R_{Vin} can decrease the startup time of the power supply. The value of R_{Vin} affects the ($V_{IN}T_{ON}$) limits of the IC.

$$\left(V_{IN} \cdot T_{ON}\right)_{\text{limit}} = 0.0043 \times \frac{720V \cdot \mu s}{Z_{IN} \Big/ \left(R_{Vin} + Z_{IN}\right)} \qquad (10.3)$$

$$\left(V_{IN} \cdot T_{ON}\right)_{PFM} = 0.0043 \times \frac{135V \cdot \mu s}{Z_{IN} \Big/ \left(R_{Vin} + Z_{IN}\right)} \qquad (10.4)$$

For this example R_{Vin} is chosen to be 5.1 MΩ therefore,

$$(V_{IN} \cdot T_{ON})_{\text{limit}} = 0.0043 \times \frac{720V \cdot \mu s}{25k\Omega \,/\!/\, (5.1M\Omega + 25k\Omega)} = 635V \cdot \mu s$$

$$(V_{IN} \cdot T_{ON})_{PFM} = 0.0043 \times \frac{135V \cdot \mu s}{25k\Omega \,/\!/\, (5.1M\Omega + 25k\Omega)} = 119V \cdot \mu s$$

Keep in mind, by changing R_{Vin} to be something other than 5.79 MΩ the minimum and maximum input voltage for start-up also changes.

Since the iW1710 uses the exact scaled value of V_{IN} for its calculations, there should be a filter capacitor on the input pin to filter out any noise that may appear on the V_{IN} signal. This is especially important for line in surge conditions.

10.4 Turns Ratio

The maximum allowable turns ratio between the primary and secondary winding is determined by the minimum detectable reset time of the transformer during PFM mode.

$$N_{TR(\max)} = \frac{(V_{IN} \cdot T_{ON})_{PFM}}{T_{RESET(\min)} \times V_{OUT}} \qquad (10.5)$$

Setting $T_{RESET(min)}$ at 1.5 µs,

$$N_{TR(\max)} = \frac{119V \cdot \mu s}{1.5\mu s \times 12.5V} = 6.3$$

For this example a turns ratio of 6 is chosen.

Keep in mind in valley mode switching the higher the turns ratio the lower the V_{DS} turn-on voltage, which means less switch turn-on power loss. Also consider the voltage stress on the MOSFET (V_{DS}) is higher with an increase in turns ratio. The voltage stress on the output diode is lower with an increase in turns ratio respectively.

10.5 Operating Maximum ($V_{IN}T_{ON}$)

Maximum operating $V_{IN}T_{ON}$ or $(V_{IN}T_{ON})_{MAX}$ for valley mode switching is traditionally designed at full load and lowest input voltage. For the iW1710, two constraints (equation 10.6 and 10.7) need to be satisfied so that indeed $(V_{IN}T_{ON})_{MAX}$ occurs at full load and lowest input voltage.

$$T_{P(QR\min)} > \frac{1}{100kHz} \qquad (10.6)$$

$$T'_{P(QR\min)} > \frac{1}{110kHz} + T_{RES} \qquad (10.7)$$

T_{RES} is the V_{DS} resonant period as shown in Figure 10.2. T_{RES} can be estimated to be approximately 2 µs as a starting point and then adjusted after the power supply is tested.

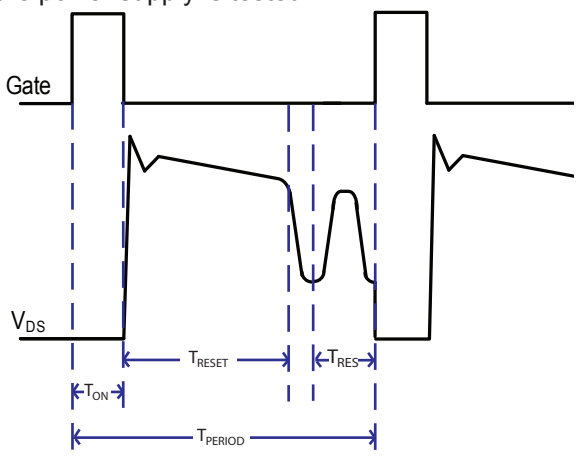


Figure 10.2 : V_{DS} Timing

When both criterion are met then $(V_{IN}T_{ON})_{MAX}$ can be determined by equation 10.8.

$$(V_{IN} \cdot T_{ON})_{\max} = \left[f_{SW(\max\ op)} \times \left(\frac{1}{V_{INDC(\min)}} + \frac{1}{N_{TR} \times V_{OUT}} \right) \right]^{-1}$$

$$\text{where, } f_{SW(\max\ op)} = \frac{1}{T_{P(QR\min)}} \qquad (10.8)$$

Where $V_{INDC(min)}$ is the minimum input voltage across the bulk capacitor. In order to avoid input undervoltage detection during normal operation, $V_{INDC(min)}$ should be set above the input undervoltage shutdown limit.

$$V_{INDC(\min)} > \frac{R_{Vin} + Z_{IN}}{Z_{IN}} \cdot V_{UVDC} \qquad (10.9)$$

Assuming T_{RES} is 2 µs then:

$$T_{P(QR\min)} > 10\mu s$$

$$T'_{P(QR\min)} > \frac{1}{110kHz} + 2\mu s = 11.1\mu s$$

$$V_{INDC(\min)} > \frac{5.1M\Omega + 25k\Omega}{25k\Omega} \times 0.369V = 76V$$

To give some margin, we use 79 V for $V_{INDC(min)}$ in equation 10.8,

$$\text{Choosing, } f_{SW(\max\ op)} = 72kHz \text{ and } T_{P(QR\min)} = 14\mu s$$

$$(V_{IN} \cdot T_{ON})_{\max} = \left[72kHz \times \left(\tfrac{1}{79V} + \tfrac{1}{6 \times 12.5V} \right) \right]^{-1} = 534V \cdot \mu s$$

Also, to provide enough margin for component values, usually:

$$(V_{IN} \cdot T_{ON})_{\max} < (V_{IN} \cdot T_{ON})_{\text{limit}} \times 0.85 \qquad (10.10)$$

$$(V_{IN} \cdot T_{ON})_{\max} < 635V \cdot \mu s \times 0.85 = 540V \cdot \mu s$$

Since we calculated 534 V·µs as our V_{IN}·T_{ON} we have enough margin.

10.6 Magnetizing Inductance

A feature of the iW1710 is the lack of dependence on the magnetizing inductance for the CC curve.

Although the constant current limit does not depend on the magnetizing inductance, there are still restrictions on the magnetizing inductance. The maximum L_M is limited by the amount of power that needs to come out of the transformer in order for the power supply to regulate. This is given by:

$$L_{M(\max)} = \frac{(V_{IN} \cdot T_{ON})^2_{\max} \times f_{sw(\max\ op)}}{2 \times P_{XFMR(\max)}}$$
$$P_{XFMR(\max)} = \frac{V_{OUT} \times I_{OUT}}{\eta_X} \qquad (10.11)$$

Where η_X is the efficiency of the transformer, for this example we assume it's 87 %.

$$P_{XFMR(\max)} = \frac{12.5V \times 1.2A}{0.87} = 17.2W$$
$$L_{M(\max)} = \frac{(534V \cdot \mu s)^2 \times 72kHz}{2 \times 17.2W} = 0.597mH$$

The minimum L_M is limited by the maximum allowable peak primary current. $V_{REG\text{-}TH}$ corresponds to the maximum I_{SENSE} voltage. See section 10.11 to calculate R_{Isense}. Therefore L_M is limited by:

$$L_{M(\min)} = \frac{2 \times P_{XFMR(\max)}}{f_{SW(\max\ op)} \times \left(V_{REG-TH} / R_{Isense} \right)^2} \qquad (10.12)$$

$$L_{M(\min)} = \frac{2 \times 12.5V \times 1.2A}{72kHz \times \left(1.0V / 1.08\Omega \right)^2} = 0.486mH$$

For this example, we choose L_M to be 0.577 mH.

If these limits do not give enough tolerance for L_M, increasing $(V_{IN}T_{ON})_{max}$ can raise the maximum limit on L_M. Take care not to go above $(V_{IN}T_{ON})_{limit}$. Also, keep in mind that if equation 10.6 and 10.7 are not met then $(V_{IN}T_{ON})_{max}$ does not occur at full load and lowest input voltage, thus some of the equations here would be invalid.

10.7 Primary Winding

In order to keep the transformer from saturation, the maximum flux density must not be exceeded. Therefore the minimum primary winding must meet:

$$N_{PRI} \geq \frac{(V_{IN} \cdot T_{ON})_{\max}}{B_{\max} \times A_e} \qquad (10.13)$$

Where B_{MAX} is maximum allowed flux density and A_e is the core area. From the transformer core datasheet we find that for this example B_{MAX} is 300 mT. For an EE19 core, A_e is 22.6 mm².

$$N_{PRI} \geq \frac{534V \cdot \mu s}{320mT \times 20.1mm^2} = 83.0T$$

For this example, we choose 90 primary turns.

10.8 Secondary Winding

From the primary winding turns, we obtain the secondary winding.

$$N_{SEC} = \frac{N_{PRI}}{N_{TR}} \qquad (10.14)$$

Thus, in our example:

$$N_{SEC} = \frac{90T}{6} = 15T$$

10.9 Bias Winding and V_{CC} Capacitance

V_{CC} is the supply to the iW1710 and should be below 16 V. The bias winding needs to ensure than V_{CC} does not exceed 16 V during normal operation.

$$N_{BIAS} = \frac{N_{SEC}(V_{CC} + V_{FD})}{V_{OUT}} \qquad (10.15)$$

Set V_{CC} at around 10 V

$$N_{BIAS} = \frac{15T \times 10.5V}{12.5V} = 12T$$

Choose a value for N_{BIAS} to be close to this number, for this example we choose 12 turns.

The V_{CC} capacitor (C_{Vcc}) stores the V_{CC} charge during IC operation and the controller checks this voltage and makes sure it is within range before starting and operating. The startup time is a function of how quickly this capacitor can charge up.

$$t_{START-UP} = \frac{C_{V_{CC}} \times V_{CC(ST)}}{\frac{V_{INAC} \times \sqrt{2}}{R_{Vin}} - I_{INST}} \qquad (10.16)$$

10.10 V_{SENSE} Resistors and Winding

The output voltage regulation is mainly determined by the feedback signal V_{SENSE}.

$$V_{SENSE} = V_{OUT\_PCB} \times K_{SENSE} \quad (10.17)$$

Where:

$$K_{SENSE} = \frac{R_{BVsns}}{\left(R_{BVsns} + R_{TVsns}\right)} \times \frac{N_{Vsense}}{N_{SEC}} \quad (10.18)$$

Internally, V_{SENSE} is compared to a reference voltage $V_{SENSE(nom)}$. Where, $V_{SENSE(nom)}$ is 1.538 V.

$$K_{SENSE} = \frac{V_{SENSE(nom)}}{V_{OUT\_PCB}} \quad (10.19)$$

$$K_{SENSE} = \frac{1.538V}{12.0V} = 0.128$$

From here we can find the ratio necessary for R_{BVsns} and R_{TVsns}. For this example we set R_{TVsns} to be 24 kΩ. Assuming we use the same winding for both V_{SENSE} and V_{CC}:

$$0.128 = \frac{R_{BVSNS}}{R_{BVSNS} + 24k\Omega} \times \frac{12T}{15T}$$
$$\rightarrow R_{BVSNS} = 4.57k\Omega$$

At this point the transformer design is complete. This would be a good time to confirm that this transformer is feasible to build.

10.11 Current Sense Resistor

The I_{SENSE} resistor determines the maximum current output of the power supply. The output current of the power supply is determined by:

$$I_{OUT} = \tfrac{1}{2} \times N_{TR} \times I_{PRI(pk)} \times \frac{T_{RESET}}{T_{PERIOD}} \times \eta_X \quad (10.20)$$

When the maximum current output is achieved the voltage seen on the I_{SENSE} pin (V_{Isense}) should reach its maximum. Thus, at constant current limit:

$$I_{PRI(pk)} = \frac{V_{Isense(CC)}}{R_{Isense}} \quad (10.21)$$

Substituting this into equation 10.20 we get:

$$V_{Isense(CC)} = \frac{T_{PERIOD}}{T_{RESET}} \times K_C \quad (10.22)$$

For iW1710 K_C is 0.5 V, therefore R_{Isense} depends on the maximum output current by;

$$R_{Isense} = \frac{N_{TR} \times K_C}{2 \times I_{OUT}} \times \eta_X \quad (10.23)$$

From table 10.1 I_{OUT} is given to be 1.2 A, therefore R_{Isense} is:

$$R_{ISNS} = \frac{6 \times 0.5V}{2 \times 1.2A} \times 0.87 = 1.08\Omega$$

We recommend using ±1% tolerance resistors for R_{Isense}.

10.12 Input Bulk Capacitor

The input bulk capacitor, C_{BULK} is chosen to maintain enough input power to sustain constant output power even as the input voltage is dropping. In order for this to be true C_{BULK} must be:

$$C_{BULK} = \frac{2 \times P_{IN} \times \left[0.25 + \frac{1}{2\pi} \times \arcsin\left(\frac{V_{INDC(\min)}}{\sqrt{2} \times V_{INAC(\min)}}\right)\right]}{\left(2 \times V_{INAC(\min)}^2 - V_{INDC(\min)}^2\right) \times f_{line}} \quad (10.24)$$

$$P_{IN} = \frac{V_{OUT(Cable)} \times I_{OUT}}{\eta_{\text{power supply}}}$$

$V_{INAC(min)}$ is the minimum input voltage (rms) to be inputted into the power supply and f_{line} is the lowest line frequency for the power supply (in this case 47 Hz). $V_{INDC(min)}$ is calculated from equation 10.9.

$$P_{IN} = \frac{12.5V \times 1.2A}{0.72} = 20.8W$$
$$C_{BULK} = \frac{2 \times 20.8W \times \left[0.25 + \frac{1}{2\pi} \times \arcsin\left(\frac{79V}{\sqrt{2} \times 85V_{ac}}\right)\right]}{\left(2 \times (85V_{ac})^2 - (79V)^2\right) \times 47Hz} = 39\mu F$$

10.13 Output Capacitance

The output capacitance affects both the steady state ripple and the dynamic response of the power supply.

Assuming an ideal capacitor where ESR (equivalent series resistance) and ESL (equivalent series inductance) are negligible then:

$$C_{OUT(\text{Steady State})} = \frac{Q_{OUT}}{V_{OUT(ripple)}} \quad (10.25)$$

The output capacitor supplies the load current when the secondary current is below the output current.

$$Q_{OUT} = \frac{L_M \times \left(I_{SEC(pk)} - I_{OUT}\right)^2}{2 \times N_{TR}^2 \times \eta_X \times V_{OUT}} \quad (10.26)$$

The $I_{SEC(pk)}$ is:

$$I_{SEC(pk)} = \frac{\left(V_{IN} \cdot T_{ON}\right)_{MAX}}{L_M} \times N_{TR} \times \eta_X \quad (10.27)$$

So to keep $V_{OUT(ripple)}$ to be 100 mV,

$$I_{SEC(pk)} = \frac{534V \cdot \mu s}{0.541mH} \times 6 \times 0.87 = 5.152A$$

$$Q_{OUT} = \frac{0.541mH\left(5.152A - 1.2A\right)^2}{2 \times 6^2 \times 0.87 \times 12.5V} = 10.8\mu C$$

$$C_{OUT(\text{Steady State})} = \frac{10.8\mu C}{100mV} = 208\mu F$$

In this calculation ESR and ESL are ignored; the reason this calculation is still valid is because of the second stage LC filter on the output of the supply. These two components reduce the ESR and ESL ripple; however keep in mind that the ripple is a little higher in reality than this calculation would suggest.

Assume that the load transient goes from no load to $I_{OUT(HIGH)}$. Then from section 9.5, equation 9.8 we find that the relationship between output capacitance ($C_{OUT(Dynamic)}$) and $V_{DROP(IC)}$ is :

$$C_{OUT(\text{Dynamic})} = \frac{I_{OUT(HIGH)} \times T_{P(\text{No load})}}{V_{DROP(IC)}} \qquad (10.28)$$

Then solving for $V_{DROP(IC)}$ from Figure 9.4, where $V_{Dynamic(DROP)}$ is the maximum allowable drop in voltage for the design during dynamic response, $V_{DROP(Cable)}$ is the drop in voltage due to the cable resistance, and $V_{DROP(sense)}$ is the drop in voltage before V_{SENSE} signal is low enough to register a dynamic transient.

$$C_{OUT(\text{Dynamic})} = \frac{I_{OUT(HIGH)} \times T_{P(\text{No load})}}{V_{Dynamic(Drop)} - V_{DROP(Cable)} - V_{DROP(sense)}} \qquad (10.29)$$

Where $T_{P(\text{No load})}$ is the maximum period under no load condition, given by equation 10.30:

$$T_{P(\text{No load})} = \frac{R_{\text{Preload}} \times \left(V_{IN} \cdot T_{ON}\right)^2_{PFM}}{2 \times L_M \times V_{OUT}^2} \times \eta_{\text{No load}} \qquad (10.30)$$

Assume that we want no more than 1.0 V drop on $V_{OUT(PCB)}$ during load transient from no load to 50% load and the efficiency of the power supply at no load ($\eta_{\text{No load}}$) is 50% , then $C_{OUT(Dynamic)}$ is:

$$T_{P(PFM)} = \frac{5.6k\Omega \times \left(119V \cdot \mu s\right)^2}{2 \times 0.541mH \times \left(12.5V\right)^2} = 461\mu s$$

Since there is no cable, $V_{DROP(cable)}$ is 0 V.

$$V_{DROP(sense)} = \left(1.538V - 1.48V\right) \times \frac{12.0V}{1.538V} = 0.543V$$

Plug everything into equation 10.19:

$$C_{OUT(\text{Dynamic})} = \frac{0.5A \times 461\mu s}{1.0V - 0V - 0.543V} = 504\mu F$$

Pick the larger capacitance value between $C_{OUT(Dynamic)}$ and $C_{OUT(Steady\ State)}$. In this case C_{OUT} is chosen to be 680 µF.

10.14 Snubber Network

The snubber network is implemented to reduce the voltage stress on the MOSFET immediately following the turn off of the gate drive. The goal is to dissipate the energy from the leakage inductance of the transformer. For simplicity and a more conservative design first assume the energy of the leakage inductance is only dissipated through the snubber. Thus:

$$\tfrac{1}{2} \times L_{lk} \times I_{PRI(pk)}^2 = \tfrac{1}{2} \times C_{SNUB} \times \left[V_{Snub(pk)}^2 - V_{Snub(val)}^2\right] \qquad (10.31)$$

L_{lk} can be measured from the transformer and V_{DS} is the voltage across the MOSFET. $V_{Snub(pk)}$ and $V_{Snub(val)}$ refer to the voltage measured across the snubber capacitor. Choose a C_{SNUB}, keeping in mind that the larger the value of C_{SNUB} the lower the voltage stress is on the MOSFET. However, capacitors are more expensive the larger their capacitance. Choose C_{SNUB} based on these two criteria and select $V_{Snub(pk)}$ and $V_{Snub(val)}$. Now a resistor needs to be selected to dissipate $V_{Snub(pk)}$ to $V_{Snub(val)}$ during the on-time of the gate driver. The dissipation of this resistor is given by:

$$\frac{V_{Snub(val)}}{V_{Snub(pk)}} = e^{-T_{P(\text{min op})} / R_{SNUB} \cdot C_{SNUB}} \qquad (10.32)$$

Using equation 10.32 solve for R_{SNUB}. This gives a conservative estimate of what C_{SNUB} and R_{SNUB} should be.

Included in the snubber network is also a resistor in series with a diode. The diode directs current to the snubber capacitor when the MOSFET is turned off; however there is some reverse current that goes through the diode immediately after the MOSFET is turned back on. This reverse current occurs because there is a short period of time when the diode still conducts after switching from forward biased to reverse biased. This conduction distorts the falling edge of the V_{SENSE} signal and affects the operation of the IC. So, the resistor in series with the diode is there to diminish the reverse current that goes through the diode immediately after the MOSFET is turned on.

10.15 T_{ON} Delay Filter

iW1710 also contains a feature that allows for adjustment to match high line and low line constant current curves. The mismatch in high line and low line is due to the delay from the IC propagation delay, driver turn-on delay, and the MOSFET turn-on delay. The driver turn-on delay maybe

further increased by a gate resistor to the MOSFET. To adjust for these delays the iW1710 factors these delays into its calculations and slightly over compensates for them to provide flexibility. R_{Dly} and C_{Dly} provide extra delay in the circuit to tweak the compensation. To determine values R_{Dly} and C_{Dly} follow these steps:

1. Measure the difference between high line and low line constant current limit without filter components.
2. Find the curve that best matches this difference from Figure 11.1.
3. Find the L_M that matches the power supply, and find the τ_{RC}.
4. Find R_{Dly} and C_{Dly} from equation 10.33

$$\tau_{RC} = R_{Dly} \times C_{Dly} \qquad (10.33)$$

10.16 SD Protection

The SD pin can be configured to provide three different types of protection: OTP protection, OVP protection and both OVP and OTP Protection. Figure 10.3 shows the three configurations plus the configuration for no OTP and OVP protection.

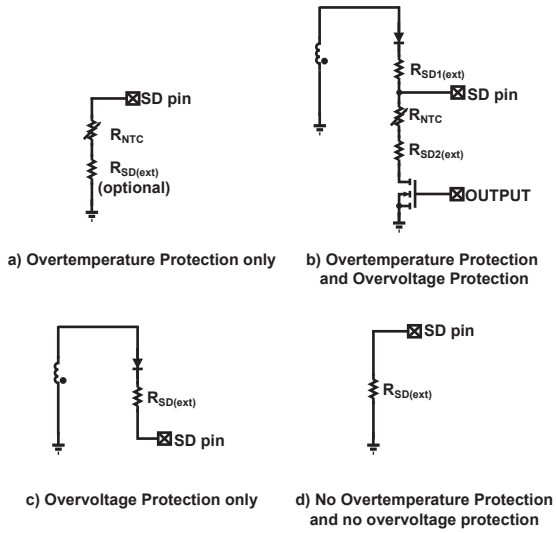


Figure 10.3 : SD Pin Application Configurations

OTP Only

To detect an overtemperature protection the iW1710 sends a 107 μA current (I_{SD}) to the SD pin every four cycles (see section 9.13). On the last cycle the iW1710 observes the voltage on the SD pin and detects an OTP fault if the voltage is lower than V_{SD-TH}, 1.0 V during normal operation and 1.2 V during startup. So $R_{SD(ext)}$ in series with NTC must meet

$$\left(R_{NTC} + R_{SD(ext)}\right) \times I_{SD} > V_{SD-TH} \qquad (10.34)$$

in order not to trigger OTP fault during normal operation.

OVP Only

For the other four cycles, the iW1710 connects the SD pin to R_{SD} to ground (see section 9.13). At the last cycle the iW1710 observes the voltage on the SD pin and detects an OVP fault if the voltage is higher than V_{SD-TH}, 1 V. In order to not trigger OVP fault, assuming 0 V drop across the series diode, $R_{SD(ext)}$ must meet:

$$\frac{V_{OUT\_PCB}}{N_{SEC}} \times N_{AUX} \times \frac{R_{SD}}{R_{SD} + R_{SD(ext)}} < V_{SD-TH} \qquad (10.35)$$

where, R_{SD} = 8.333 kΩ

Both OTP and OVP

To find $R_{SD1(ext)}$ so that OVP can be detected, use equation 10.35. To find $R_{SD2(ext)}$ in series with the NTC use equation 10.34.

No OTP and OVP

If OTP and OVP from the SD pin are not needed, simply place a resistor, $R_{SD(ext)}$ to ground from the SD pin. Make sure $R_{SD(ext)}$ meets equation 10.36 so OTP protection does not trip.

$$R_{SD(ext)} \times I_{SD} > V_{SD-TH} \qquad (10.36)$$

Note that this means OVP is not detected through the SD pin; however, OVP from V_{SENSE} pin is still active and the iW1710still shuts down if overvoltage condition is detected.

Since for this example OTP and OVP are not necessary we place a resistor from SD pin to ground and calculate its value from equation 10.36.

$$R_{SD(ext)} > {}^{1.2V}\!/_{100\mu A} = 12k\Omega$$

10.17 PCB Layout

In the iW1710, there are two signals that are important to control the output performance; these are the I_{SENSE} signal and the V_{SENSE} signal. The I_{SENSE} resistor should be close to the source of the MOSFET to avoid any trace resistance from contaminating the I_{SENSE} signal. Also, the I_{SENSE} signal should be placed close to the I_{SENSE} pin. The V_{SENSE} signal should be placed close to the transformer to improve the quality of the sensing signal. Also for better output performance all

bypass capacitors should be placed close to their respective pins.

To reduce EMI, switching loops need to be minimized. These loops include:

1. The input bulk capacitor, primary winding, MOSFET and R_{Isense} loop.
2. The output diode, output capacitor and secondary winding loop.
3. V_{CC} winding and rectifier diode loop.

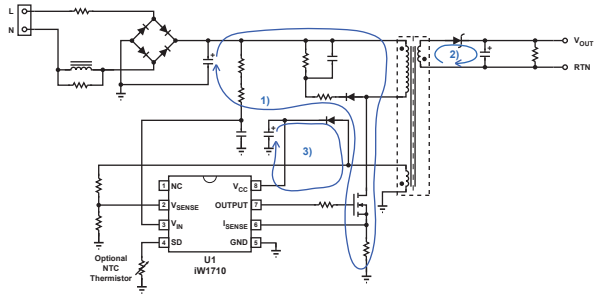


Figure 10.4 : Switching Loops

To improve ESD performance provide a low impedance path from the ground pin of the transformer to the ac power source and make sure this path does not go through the IC ground pin. A discharge spark gap helps to transfer ESD and EOS energy from the secondary side of the power supply directly to the external ac power source.

In a switch-mode power supply there are several ground signals, namely: the power ground, the switching ground and the control logic ground. These ground signals should be connected by a star connection. Ground traces should be kept as short as possible. A thick trace on the switching ground helps to lessen switching losses.

11.0 Design Example Performance Characteristics

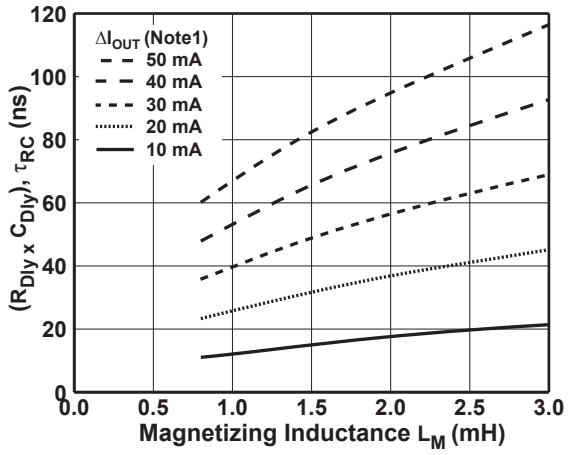


Figure 11.1 : T_{ON} Compensation Chart

12.0 Application Circuit

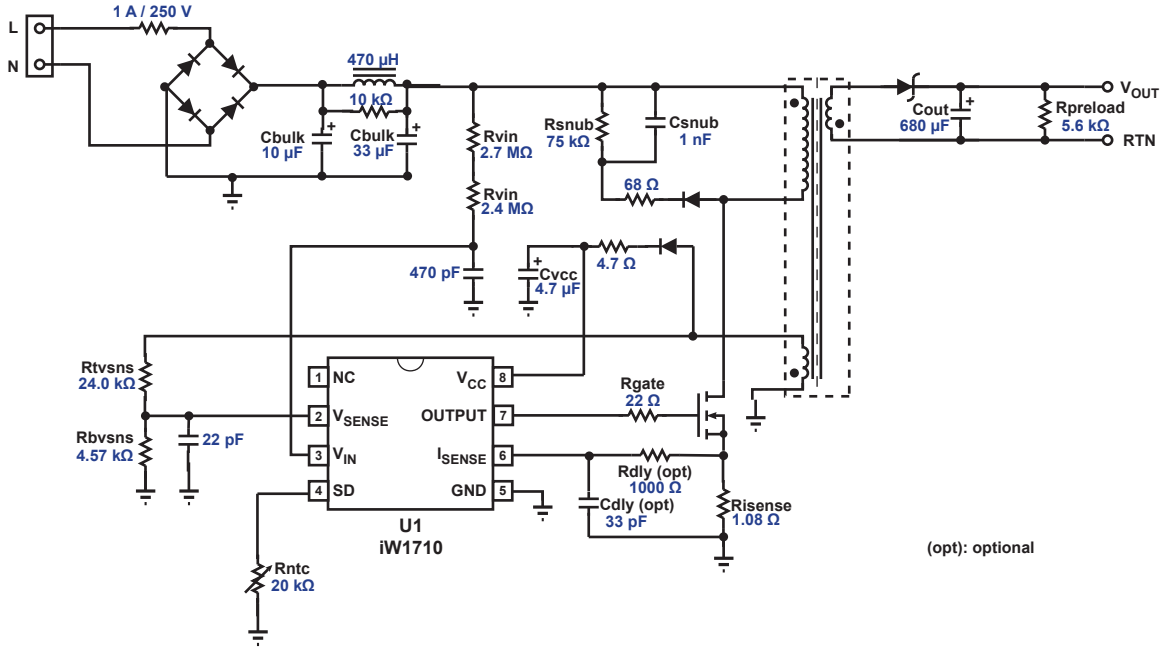
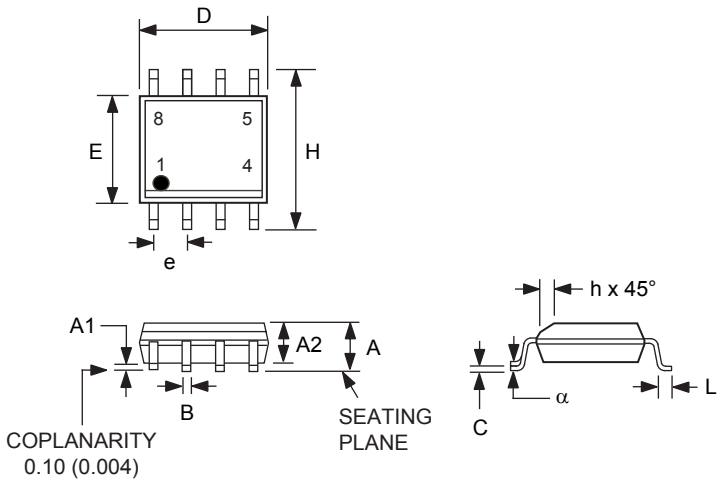


Figure 12.1 : Typical Application Circuit

Note 1: ΔI_{OUT} refers to the difference in constant current limit between 264 V_{ac} and 90 V_{ac} when no R_{DLY} and C_{DLY} are applied.

13.0 Physical Dimensions

8-Lead Small Outline (SOIC) Package



Symbol	Inches		Millimeters	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.0040	0.010	0.10	0.25
A2	0.049	0.059	1.25	1.50
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
h	0.10	0.020	0.25	0.50
L	0.016	0.049	0.4	1.25
α	0°	8°		

Figure 13.1 : Physical dimensions, 8-lead SOIC package

Compliant to JEDEC Standard MS12F

Controlling dimensions are in inches; millimeter dimensions are for reference only

This product is RoHS compliant and Halide free.

Soldering Temperature Resistance:
[a] Package is IPC/JEDEC Std 020D Moisture Sensitivity Level 1
[b] Package exceeds JEDEC Std No. 22-A111 for Solder Immersion Resistance; package can withstand 10 s immersion < 270˚C

Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 mm per side.

The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic bocy exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.

14.0 Ordering Information

Part Number	Options	Package	Description
iW1710-01	Cable Comp = 0 mV	SOIC-8	Tape & Reel[1]
iW1710-21	Cable Comp = 300 mV	SOIC-8	Tape & Reel[1]

Note 1: Tape & Reel packing quantity is 2,500/reel.

Trademark Information

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