ISL97687IRTZ-HEVALZ, ISL97687IRTZ-LEVALZ

Evaluation Board

AN1674
Rev 0.00
October 12, 2011

The ISL97687 is a PWM controlled LED driver that supports 4 channels of LED current and LED peak current with jumpers for Monitor and TV LCD backlight applications. It is capable of driving 160mA per channel from a 9V to 32V input supply, with current sources rated up to 75V absolute maximum. ISL97687IRTZ has two types of driver boards; "ISL97687IRTZ-LEVALZ" and "ISL97687IRTZ-HEVALZ" for driving up to 12 LEDs and 22 LEDs per channel, as shown in Figures 1, 2, 3, and 4. The key differences between each board are summarized in Table 1.

Quick Start Guide

ISL97687 provides many different PWM dimming methods. The interface modes and its settings are summarized in Table 2. Those interfaces can be selected with switch and jumper settings of the evaluation board as shown in Figures 5 and 6.

- **Direct PWM Dimming Mode**
  Insert Jumper in the top position of the JP_PWM_SET to apply VDC to the PWM_SET/PLL pin. In this mode, all other inputs (ACTL, STV , EN_PS, EN_VSYNC, EN_ADIM) will be neglected. The LED dimming frequency and phase of the LEDs will be the same as the input of PWMI, as shown in Figures 7 and 8.
- **Decoded PWM Dimming Mode**
  Insert Jumper in the bottom position of the JP_PWM_SET to apply the POT resistor of R_PWM_SET to adjust LED dimming frequency in Figure 9. The JP_CPLL should be opened.
- **VSYNC Mode**
  Connect the JP_CPLL and disconnect the JP_PWM_SET. Set the switch SW_EN_VSYNC to be ON. The LED dimming frequency will be selected by frame signal coming to the STV pin (see the Table 1 in the ISL97687 datasheet). Figure 11 shows the waveforms at VSYNC mode.
- **Phase Shift Mode**
  Connect Jumper to JP_PWM_SET for decoded PWM dimming mode or JP_CPLL for VSYNC mode and then set switch SW_EN_PS to ON. Figure 10 shows phase shifted channel output. Figure 12 shows the channel output waveforms in the phase shifted VSYNC mode.
- **ACTL Interface Mode**
  Connect Jumper JP_PWM_SET for decoded PWM dimming mode or JP_CPLL for VSYNC mode and then set switch SW_EN_ADIM to ON. Apply an analog control signal of 0.3V (0% dimming) ~3.0V (100% dimming) with adjusting POT R_ACTL or directly connect to the jumper pin by removing JP_ACTL. In the ACTL or ACTL*PWMI mode, the PWMI pin should not be floating or GND but tied to VDC or applying the PWM signal.

The ISL97687 evaluation board provides the adjustments of boost switching frequency, LED dimming frequency, and LED peak current with jumpers and potentiometer,s as shown in Figure 6. Please use the following steps for the adjustment and selection of the analog settings.

- **Boost Switching Frequency Adjustment**
  Place jumper JP_OSC to connect the OSC pin to the potentiometer and then change the resistance of the potentiometer R_OSC for the boost switching frequency adjustment.
- **Dimming Frequency Adjustment**
  Place jumper JP_PWM_SET between the middle and lower pins to connect the PWM_SET pin to the potentiometer for the dimming frequency adjustment.
- **LED Peak Current Adjustment**
  For two-step LED peak current settings, place jumper JP_ISET1 and JP_ISET2 each to connect potentiometers to the pin of ISET1 and ISET2. Adjust the LED peak current to change the resistance of the potentiometers, R_ISET1 and R_ISET2.
- **OVP Threshold Setting**
  The OVP level can be set based on Equation 1. The boost can regulate down to 30% of OVP. The OVP level should be considered max forward voltage of strings and margin of low temperature start-up.

$$OVP = 1.21V \times (R_{UPPER} + R_{LOWER}) / R_{LOWER} \quad \text{(EQ. 1)}$$

  Please refer to the ISL97687 datasheet for detailed switching and regulation adjustment.

For power-up, set switch SW_nSHUT to high and connect JP_nSHUT to PVIN. Apply input voltage to the PVIN and PGND pins based on the load conditions according to Table 1.

Each LED string can be configured with jumpers adjusted to a maximum of 12 LEDs for ISL97687IRTZ-LEVALZ or a maximum of 22 LEDs for ISL97687IRTZ-HEVALZ per channel. Please make sure the minimum number of LEDs/string will be limited by 30% of boost OVP level.

The populated LEDs are rated 150mA maximum, but care should be taken with the board temperature in setting the LED peak current according to the ambient temperature.

TABLE 1. COMPARISON OF ISL97687IRTZ-LEVALZ, ISL97687IRTZ-HEVALZ

EVALUATION BOARD	ISL97687IRTZ-LEVALZ	ISL97687IRTZ-HEVALZ
Max LEDs/Ch	Driving up to 12 LEDs/Ch	Driving up to 22 LEDs/Ch
OVP Limit	49.6V (14.9V of 30% OVP)	79.3V (23.8V of 30% OVP)
Current Limit	4.25A (sense resistor 40mΩ)	4.25A (sense resistor 40mΩ)
Input Voltage Range	10V to 19V for 120mA/12 LEDs	20V to 30V for 120mA/22 LEDs

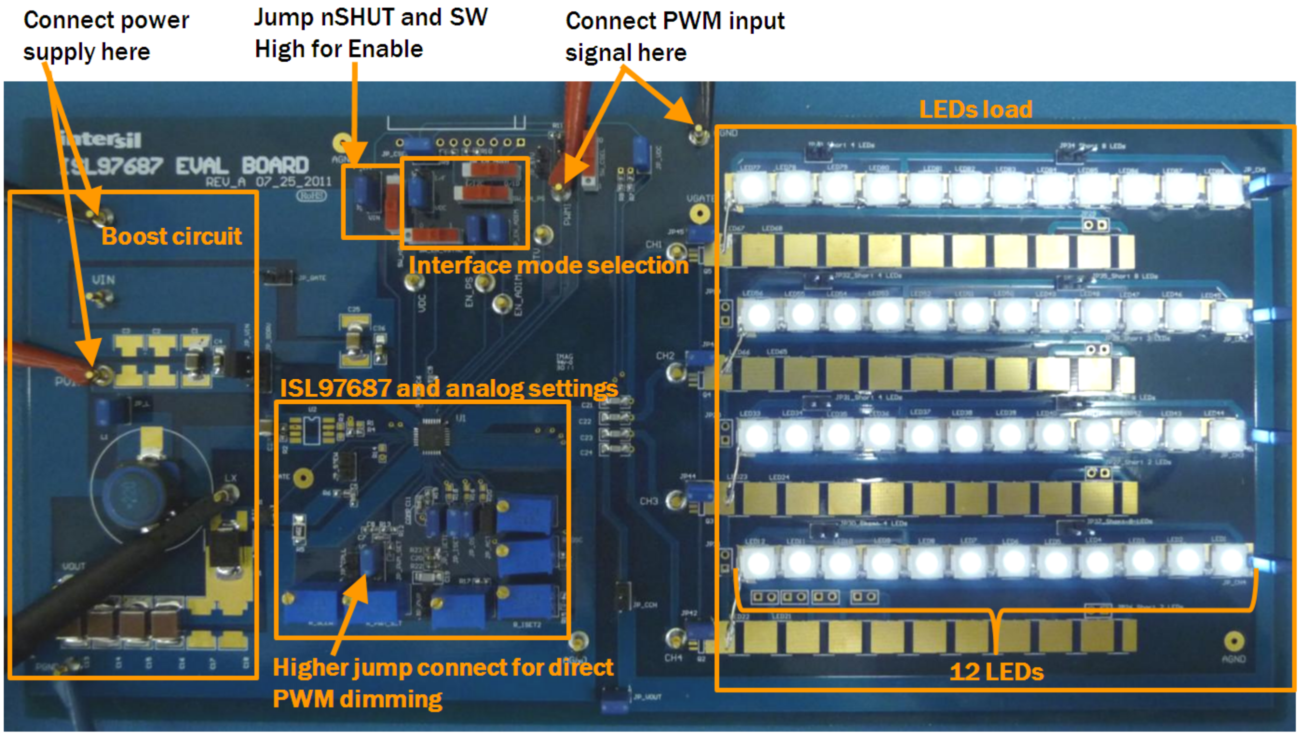


FIGURE 1. PHOTO OF ISL97687IRTZ-LEVALZ

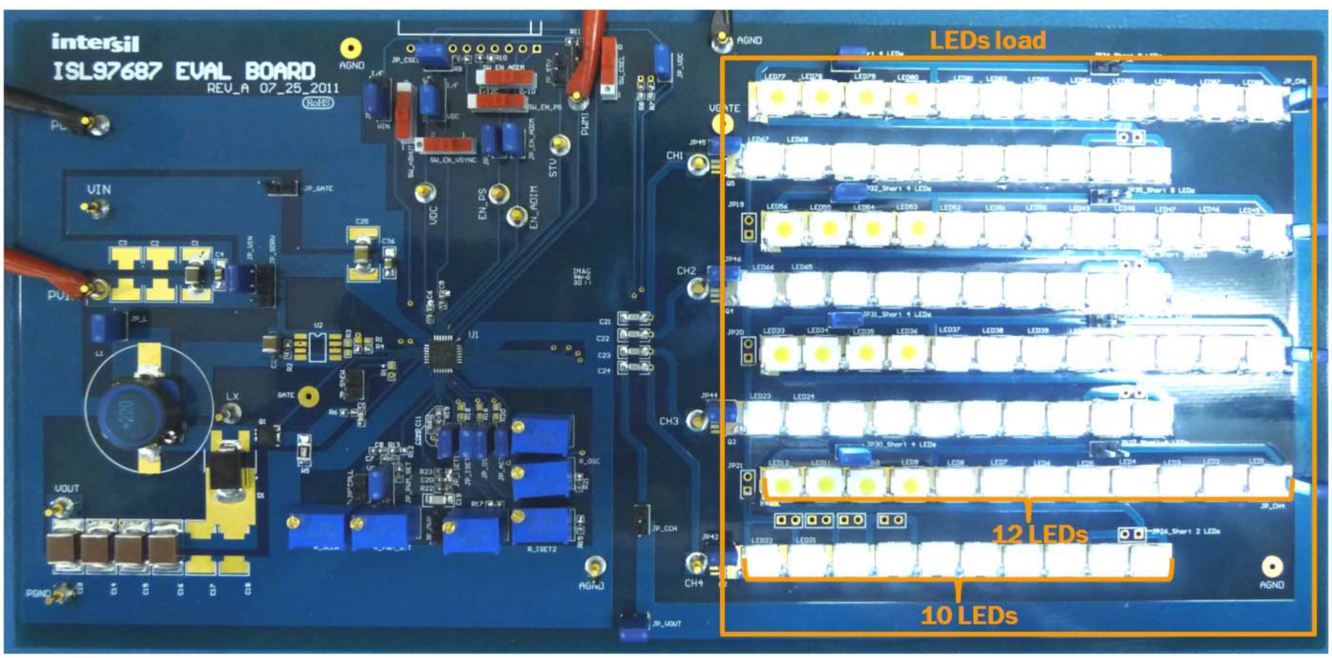


FIGURE 2. PHOTO OF ISL97687IRTZ-HEVALZ

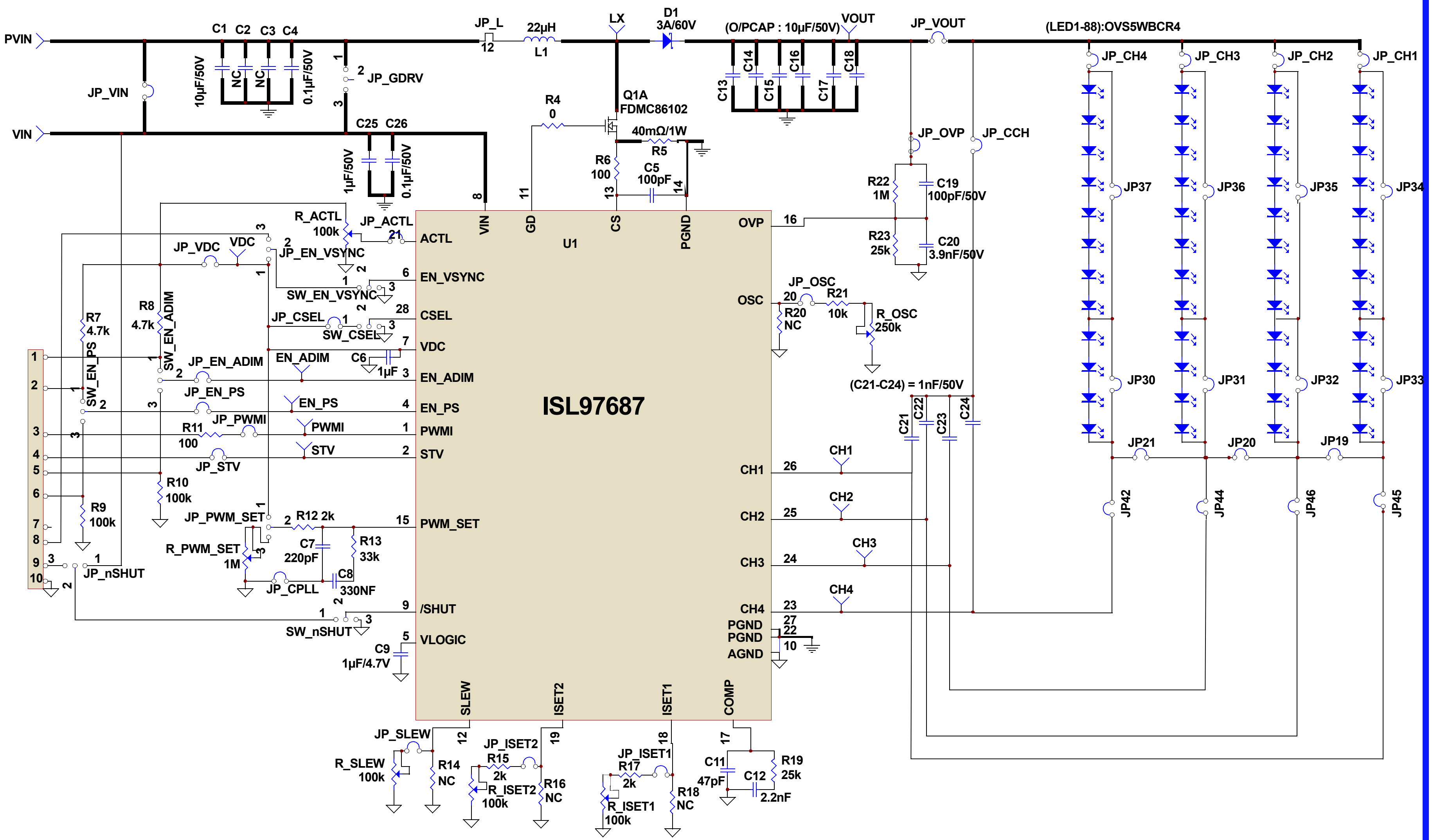


FIGURE 3. SCHEMATIC OF ISL97687IRTZ-LEVALZ

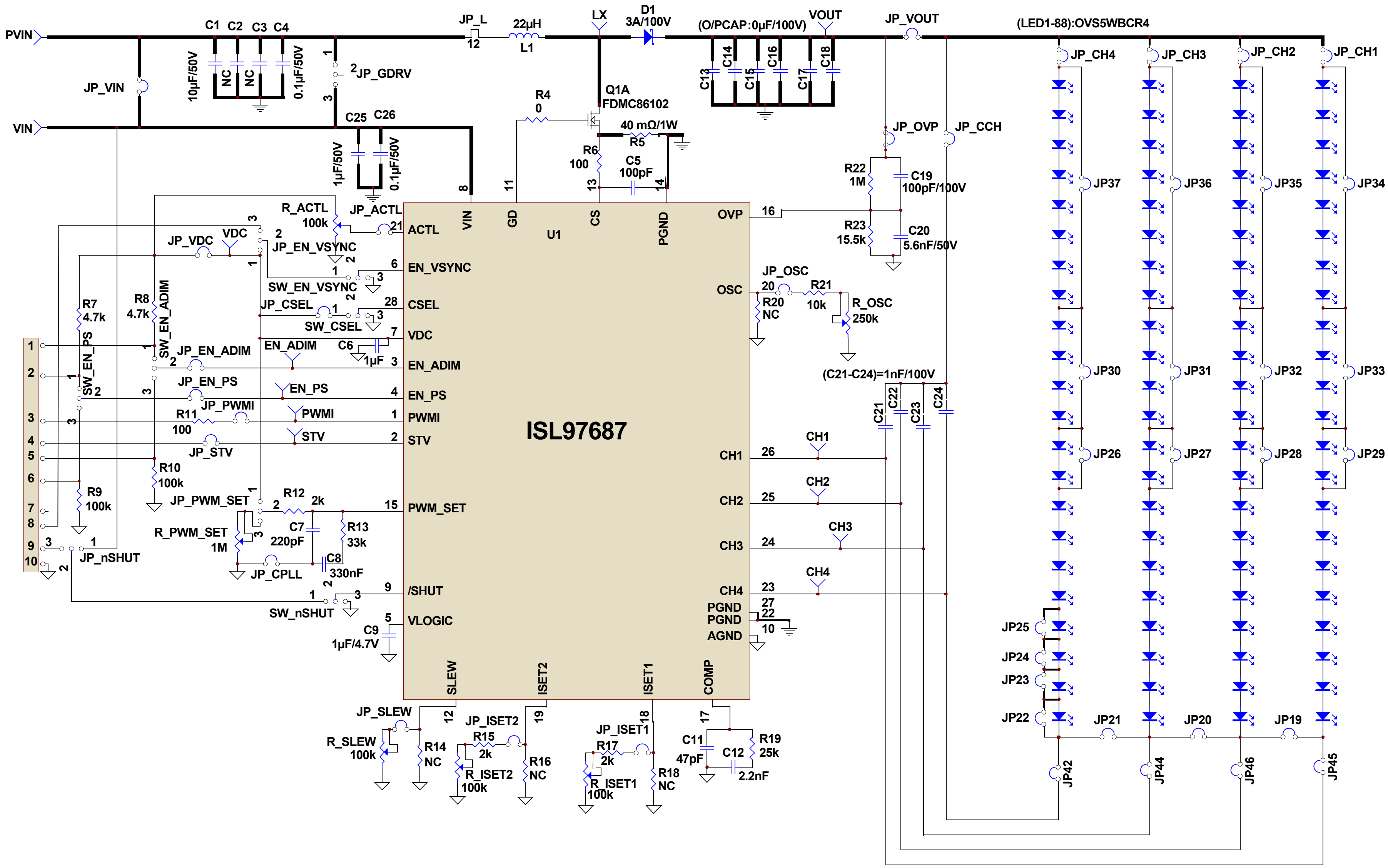
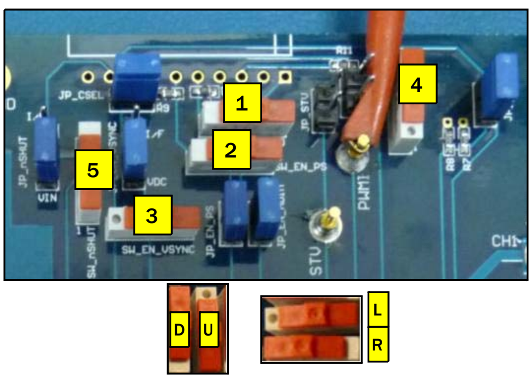


FIGURE 4. SCHEMATIC OF ISL97687IRTZ-HEVALZ

TABLE 2. SWITCH SETTINGS FOR INTERFACE MODE SELECTION

INTERFACE MODE	INPUT SIGNAL AND COMPONENT CONNECTION TO THE PIN						
	JP_PWM_SET/PLL	PWMI	ACTL	STV	EN_ADIM	EN_VSYNC	EN_PS
Direct PWM dimming mode	H	Y	N	N	N	N	N
Direct PWM dimming mode only	Resistor connection for dimming frequency adjustment	Y	N	N	L	L	L
VSYNC mode	RC loop filter for PLL	Y	Y	Y	Y	H	Y
Phase shift mode	Resistor connection for dimming frequency adjustment or RC loop filter for VSYNC	Y	Y	Y	Y	Y	H
ACTL mode	Resistor connection for dimming frequency adjustment or RC loop filter for VSYNC	H	Y	Y	H	Y	Y
ACTL * PWMI mode	Resistor connection for dimming frequency adjustment or RC loop filter for VSYNC	Y	Y	Y	H	Y	Y

H: Tied to VDC Y: Input signal available or mode selectable
L: Tied to GND N: Input signal not available or negligible



1 SW_EN_ADIM: Analog dimming mode, L:OFF, R:ON

2 SW_EN_PS: Phase shift mode, L: OFF, R: ON

3 SW_EN_VSYNC : Dim. synchronization with STV
L:ON, R:OFF

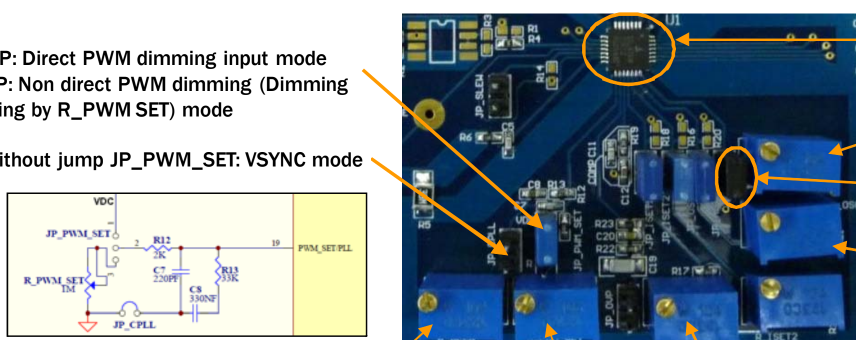
4 SW_CSEL: LED current setting pin selection
U: Select ISET2 pin
D: Select ISET1 pin

5 SW_nSHUT: ENABLE, D: OFF, U:ON

FIGURE 5. JUMP SETTINGS FOR INTERFACE MODE SELECTION

JP_PWM_SET
- HIGHER JUMP: Direct PWM dimming input mode
- LOWER JUMP: Non direct PWM dimming (Dimming frequency setting by R_PWM SET) mode

JP_CPLL without jump JP_PWM_SET: VSYNC mode



ISL97687

Adjustment for ACTL input

Remove jumper to provide direct access to ACTL pin

Adjustment for Boost frequency

Adjustment for FPWM Adjustment for ISET1 Adjustment for ISET2

FIGURE 6. JUMP/RESISTOR SETTINGS FOR LED DIMMING CURRENT AND FREQUENCY ADJUSTMENT

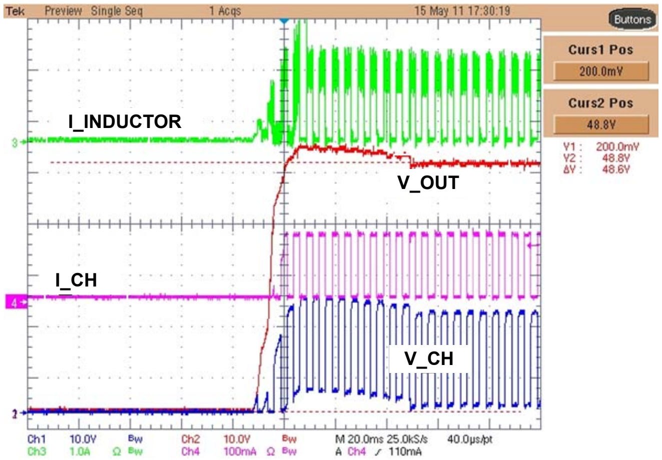


FIGURE 7. START-UP (DIRECT PWM DIMMING, V_{IN}: 19V, I_{CH}: 120mA, LEDs: 4P18S, f_{DIM}: 200Hz)

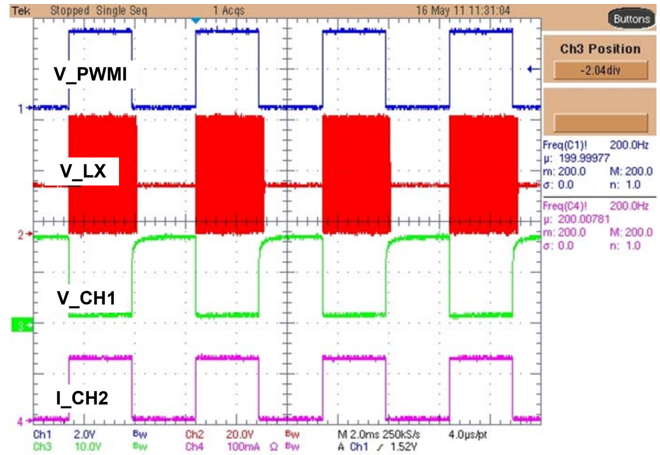


FIGURE 8. DIRECT PWM DIMMING (V_{IN}: 19V, LEDs: 4P18S, f_{DIM}: 200Hz)

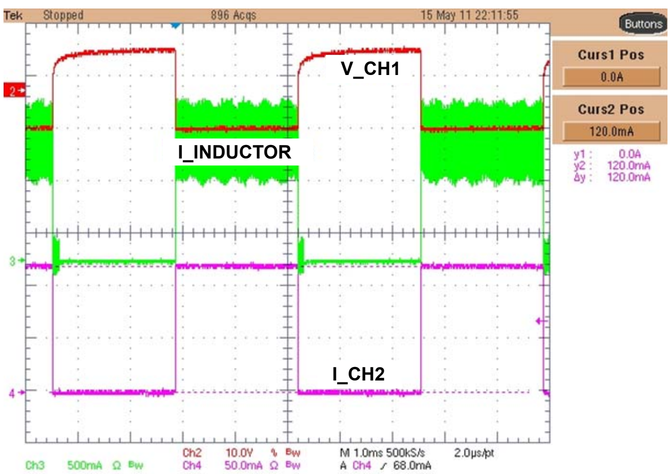


FIGURE 9. PWM DIMMING WITHOUT PHASE SHIFT (V_{IN}: 19V, I_{CH}: 120mA, LEDs: 4P18S, f_{DIM}: 200Hz)

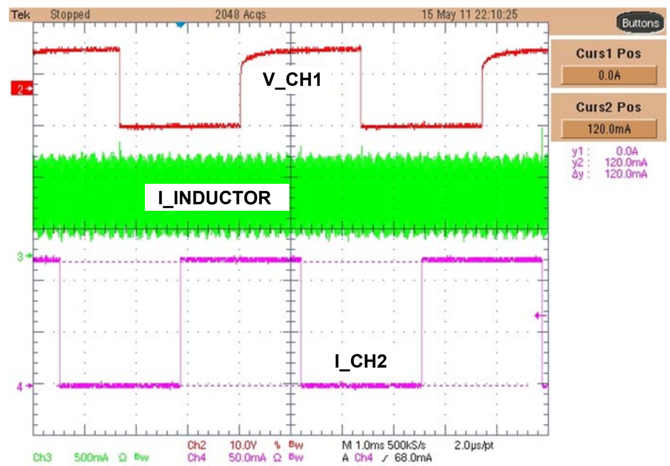


FIGURE 10. PWM DIMMING WITH PHASE SHIFT (V_{IN}: 19V, I_{CH}: 120mA, LEDs: 4P18S, f_{DIM}: 200Hz)

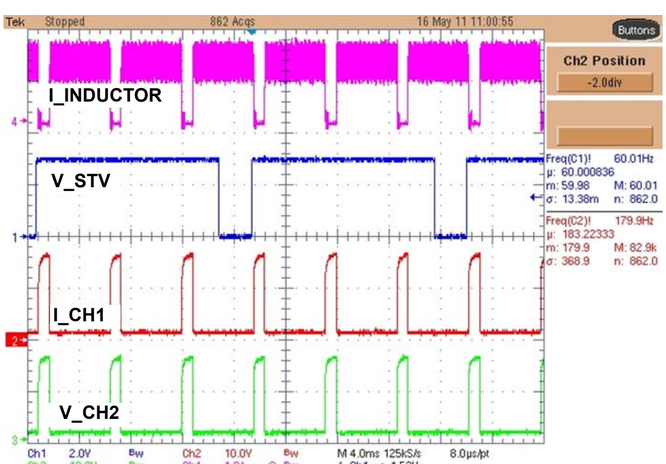


FIGURE 11. V_{SYNC} ENABLED DIMMING WITHOUT PHASE SHIFT (V_{IN}: 19V, I_{CH}: 120mA, LEDs: 4P18S, 180Hz OUTPUT PHASE AND FREQUENCY LOCKED TO 60Hz STV)

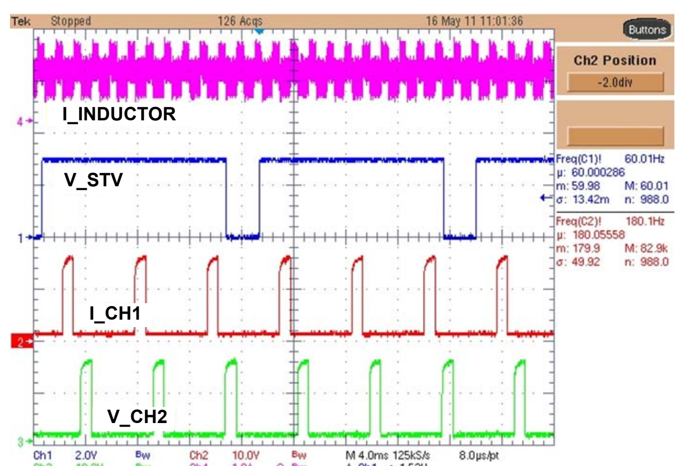


FIGURE 12. V_{SYNC} ENABLED WITH PHASE SHIFT (V_{IN}: 19V, I_{CH}: 120mA, LEDs: 4P18S, 180Hz OUTPUT PHASE AND FREQUENCY LOCKED TO 60Hz STV)

ISL97687 Layout Guideline

Great care is needed in designing a PC board for stable ISL97687 operation. As shown in the typical application diagrams in Figures 3 and 4, the separation of PGND and AGND of each ISL97687 is essential, keeping the AGND referenced only local to the chip. This minimizes switching noise injection to the feedback sensing and analog areas, as well as eliminating DC errors from high current flow in resistive PC board traces. PGND and AGND should be on the top and bottom layers, respectively, in the two layer PCB in Figures 14 and 16. A star ground connection should be formed by connecting the LED ground return and AGND pins to the thermal pad with 9 to 12 vias shown in Figures 13 and 15. The ground connection should be into this ground net, on the top plane. The bottom plane then forms a quiet analog ground area, that both shields components on the top plane, as well as providing easy access to all sensitive components. For example, the ground side of the ISET1/2 resistors can be dropped to the bottom plane, providing a very low impedance path back to the AGND pin, which does not have any circulating high currents to interfere with it. The bottom plane can also be used as a thermal ground, so the AGND area should be sized sufficiently large to dissipate the required power. For multi-layer boards, the AGND plane can be the second layer. This provides easy access to the AGND net, but allows a larger thermal ground and main ground supply to come up through the thermal vias from a lower plane.

This type of layout is particularly important for this type of product, as the ISL97687 has a high power boost, resulting in high current flow in the main loop's traces. Careful attention should be focused on the following layout details:

1. Boost input capacitors, output capacitors, inductor and Schottky diode should be placed together in a nice tight layout. Keeping the grounds of the input, output, ISL97687 and the current sense resistor connected with a low impedance and wide metal is very important to keep these nodes closely coupled.
2. Figure 15 shows important traces of the current sensor (RS) and the OVP resistors (RU, RL). The current sensor track line should be short, so that it remains as close as possible to the Current Sense (CS) pin. Additionally, the CS pin is referenced from the adjacent PGND pin. It is extremely important that this PGND pin is placed with a good reference to the bottom of the sense resistor. In Figure 15, you can see that this ground pin is not connected to the thermal pad, but instead used to effectively sense the voltage at the bottom of the current sense resistor. However, this pin also takes the gate driver current, so it must still have a wide connection and a good connection back from the sense resistor to the star ground. Also, the RC filter on CS should be placed referenced to this PGND pin and be close to the chip.
3. If possible, try to maintain the central ground node on the board and use the input capacitors to avoid excessive input ripple for high output current supplies. The filtering capacitors should be placed close to the VIN pin.
4. For optimum load regulation and true V_{OUT} sensing, the OVP resistors should be connected independently to the top of the output capacitors and away from the higher dv/dt traces. The OVP connection then needs to be as short as possible to the pin. The AGND connection of the lower OVP components is critical for good regulation. At 70V output, a 100mV change at V_{OUT} translates to a 1.7mV change at OVP, so a small ground error due to high current flow, if referenced to PGND, can be disastrous.
5. The bypass capacitors connected to VDC and VLOGIC need to be as close to the pin as possible, and again, should be referenced to AGND. This is also true for the COMP network and the rest of the analog components (on ISET1/2, PWM_SET, etc.).
6. The heat of the chip is mainly dissipated through the exposed thermal pad, so maximizing the copper area around it is a good idea. A solid ground is always helpful for the thermal and EMI performance.
7. The inductor and input and output capacitors should be mounted as tight as possible, to reduce the audible noise and inductive ringing.

General Power PAD Design Considerations

Figure 13 shows an example of how to use vias to remove heat from the IC. We recommend you fill the thermal pad area with vias. A typical via array would be to fill the thermal pad footprint with vias spaced such that the center-to-center spacing is three times the radius of the via. Keep the vias small, but not so small that their inside diameter prevents solder wicking through the holes during reflow.

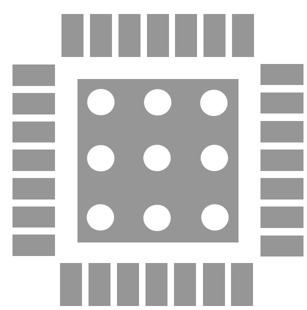


FIGURE 13. ISL97687 TQFN PCB VIA PATTERN

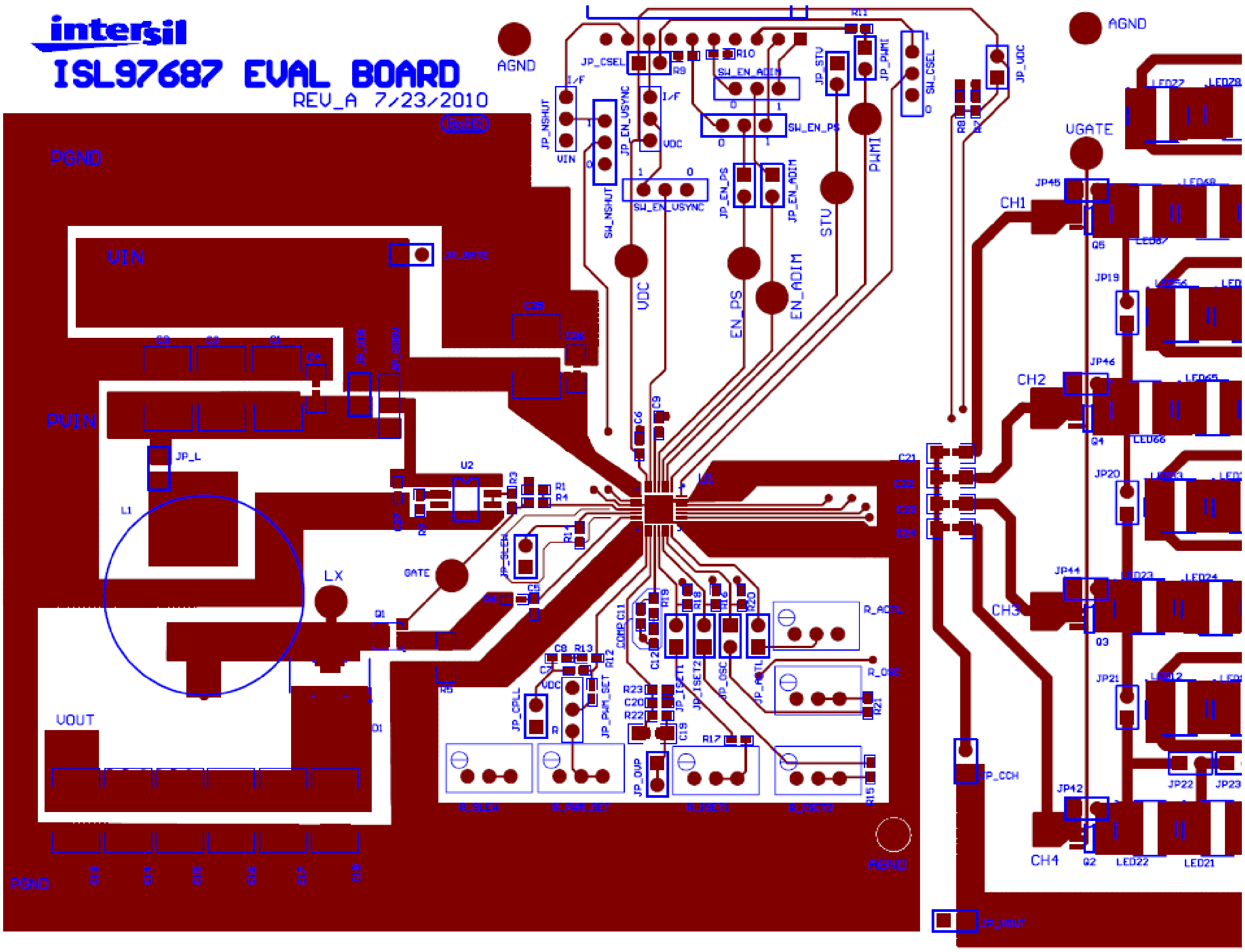


FIGURE 14. ISL97687 TOP LAYER OF EVALUATION BOARD

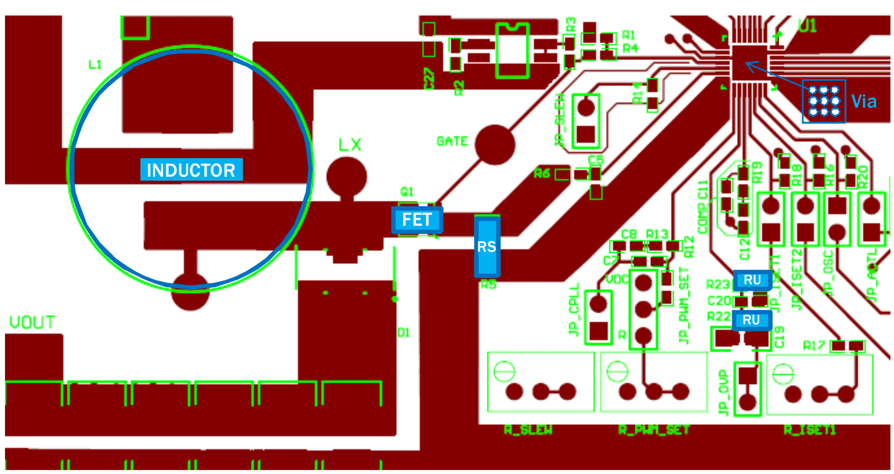


FIGURE 15. CURRENT SENSOR AND OVP RESISTORS

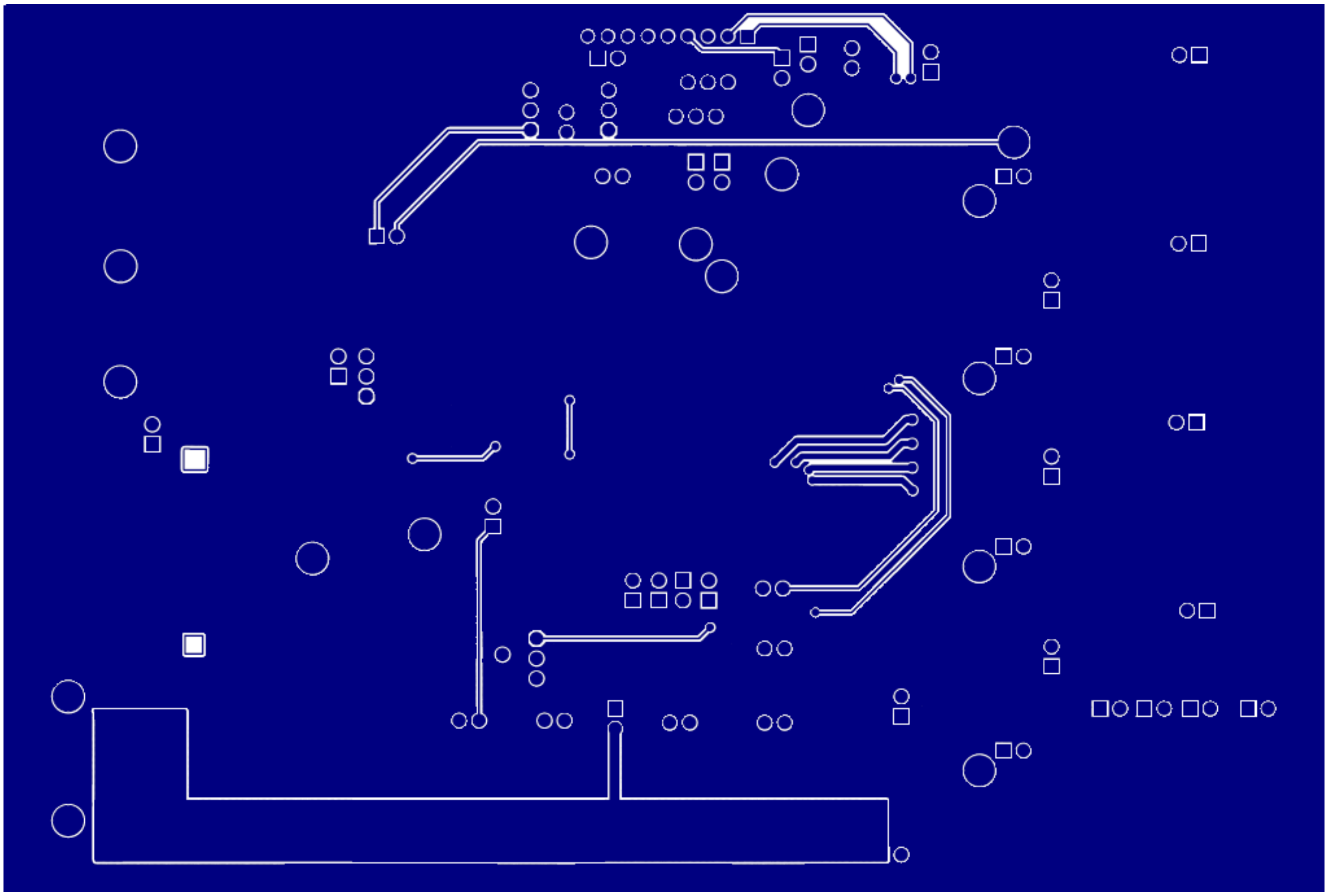


FIGURE 16. ISL97687 BOTTOM LAYER OF EVALUATION BOARD

Bill of Materials

ISL97687IRTZ-LEVALZ	ISL97687IRTZ-HEVALZ	DESIGNATOR	FOOTPRINT
0	0	R4	603
0	0	R2	603
0.1µF/50V	0.1µF/50V	C26	805
0.1µF/50V	0.1µF/50V	C4	805
1M	1M	R22	603
1nF/50V	1nF/100V	C21, C22, C23, C23	805
1µF/10V	1µF/10V	C6, C9	603
1µF/50V	1µF/50V	C25	1210
2.2nF	2.2nF	C12	603
2k	2k	R12, R15, R17	603
3A/60V	3A/100V	D1	SMB/C/D2PAK
4.7k	4.7k	R7, R8	603
4.7µF/50V	4.7µF/50V	C27	603
3.9nF	5.6nF	C20	603
100	100	R6, R11	603
100k	100k	R9, R10	603

Bill of Materials (Continued)

ISL97687IRTZ-LEVALZ	ISL97687IRTZ-HEVALZ	DESIGNATOR	FOOTPRINT
100k	100k	R_SLEW	VRES
100k	100k	R_ISET2	VRES
100k	100k	R_ISET1	VRES
100k	100k	R_ACTL	VRES
1M	1M	R_PWM_SET	VRES
250k	250k	R_OSC	VRES
100pF	100pF	C5	603
100pF/50V	100pF/100V	C19	C19
10k	10k	R21	603
10µF/50V	10µF/100V	C13, C14, C15, C16, C17	1210/2220
10µF/35V	10µF/35V	C1	1210
22µH	22µH	L1	SLF12575T-220M4R0-PF
25k use for V_{OUT} OVP: 50V 25k use for V_{OUT} OVP: 50V	15.5k use for V_{OUT} OVP: 80V 25k use for V_{OUT} OVP: 50V	R23	603
40mΩ/1W	40mΩ/1W	R5	1206
220pF	220pF	C7	603
25k	25k	R19	603
330nF	330nF	C8	603
33k	33k	R13	603
47pF	47pF	C11	603
FDMC86102	FDMC86102	Q1	FDMC86102
SWITCH	SWITCH	SW_EN_PS	SWITCH-SLIDE-SPDT
SWITCH	SWITCH	SW_CSEL	SWITCH-SLIDE-SPDT
SWITCH	SWITCH	SW_EN_ADIM	SWITCH-SLIDE-SPDT
SWITCH	SWITCH	SW_EN_VSYNC	SWITCH-SLIDE-SPDT
150mA/3.2V	150mA/3.2V	(LED1:LED88)	OVS5WBCR4

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

Colophon 7.0