

# SN54AHCT157, SN74AHCT157 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MUXES

SCLS347K – MAY 1996 – REVISED JULY 2003

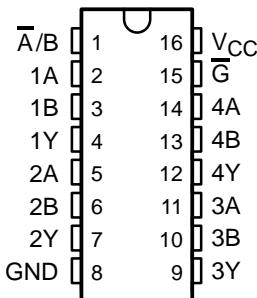
- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17

## description/ordering information

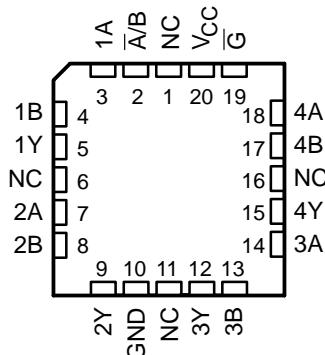
These quadruple 2-line to 1-line data selectors/multiplexers are designed for 4.5-V to 5.5-V V<sub>CC</sub> operation.

The 'AHCT157 devices feature a common strobe (G) input. When the strobe is high, all outputs are low. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The devices provide true data.

SN54AHCT157 . . . J OR W PACKAGE  
SN74AHCT157 . . . D, DB, DGV, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54AHCT157 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74AHCT157N	SN74AHCT157N
	SOIC – D	Tube	SN74AHCT157D	AHCT157
		Tape and reel	SN74AHCT157DR	
	SOP – NS	Tape and reel	SN74AHCT157NSR	AHCT157
	SSOP – DB	Tape and reel	SN74AHCT157DBR	HB157
	TSSOP – PW	Tube	SN74AHCT157PW	HB157
		Tape and reel	SN74AHCT157PWR	
-55°C to 125°C	TVSOP – DGV	Tape and reel	SN74AHCT157DGVR	HB157
	CDIP – J	Tube	SNJ54AHCT157J	SNJ54AHCT157J
	CFP – W	Tube	SNJ54AHCT157W	SNJ54AHCT157W
	LCCC – FK	Tube	SNJ54AHCT157K	SNJ54AHCT157FK

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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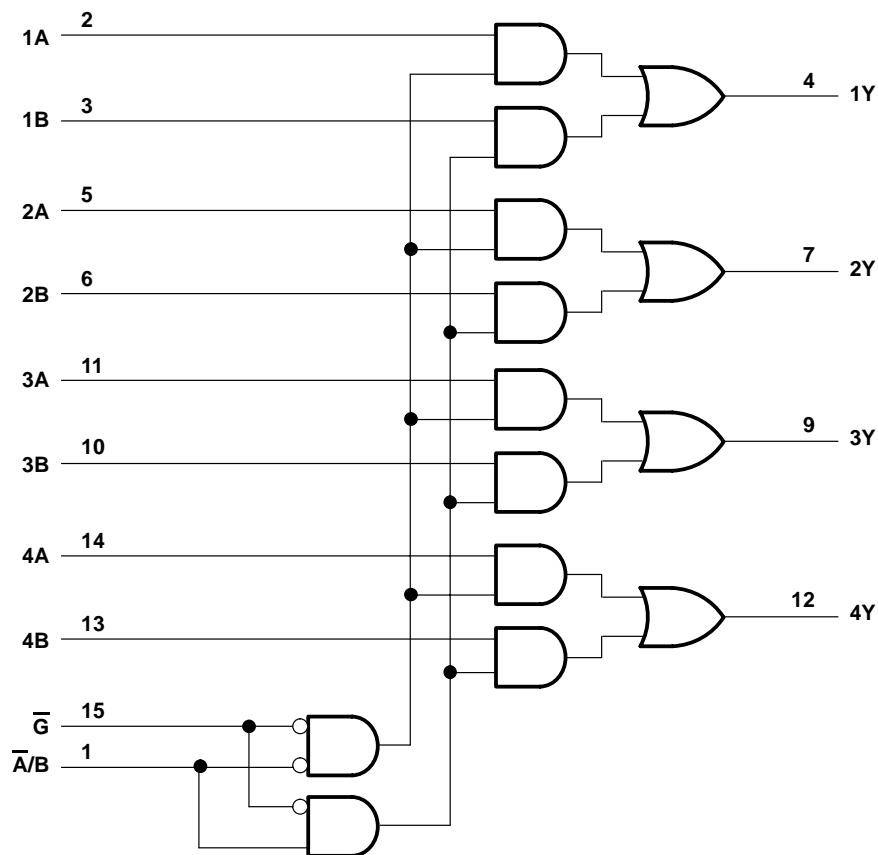
# SN54AHCT157, SN74AHCT157 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

SCLS347K – MAY 1996 – REVISED JULY 2003

FUNCTION TABLE

INPUTS				OUTPUT
$\bar{G}$	$\bar{A}/B$	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, and W packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V	
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to 7 V	
Output voltage range, $V_O$ (see Note 1) .....	–0.5 V to $V_{CC}$ + 0.5 V	
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–20 mA	
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	±20 mA	
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	±25 mA	
Continuous current through $V_{CC}$ or GND .....	±50 mA	
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package .....	73°C/W	
DB package .....	82°C/W	
DGV package .....	120°C/W	
N package .....	67°C/W	
NS package .....	64°C/W	
PW package .....	108°C/W	
Storage temperature range, $T_{STG}$ .....	–65°C to 150°C	

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 3)**

		SN54AHCT157		SN74AHCT157		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	5.5	0	5.5	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–8		–8	mA
$I_{OL}$	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall time		20		20	ns/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54AHCT157, SN74AHCT157 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MUXES

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AHCT157	SN74AHCT157	UNIT
			MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 $\mu$ A	4.5 V	4.4	4.5		4.4	4.4	V
	I <sub>OH</sub> = -8 mA		3.94			3.8	3.8	
V <sub>OL</sub>	I <sub>OL</sub> = 50 $\mu$ A	4.5 V		0.1		0.1	0.1	V
	I <sub>OL</sub> = 8 mA			0.36		0.44	0.44	
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V		$\pm$ 0.1		$\pm$ 1*	$\pm$ 1	$\mu$ A
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		2		20	20	$\mu$ A
$\Delta$ I <sub>CC</sub> <sup>†</sup>	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V		1.35		1.5	1.5	mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V	2	10			10	pF

\* On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V  $\pm$  0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN54AHCT157	SN74AHCT157	UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 15 pF	4.1**	6.4**		1**	7.5**	1 7.5
t <sub>PHL</sub>				4.1**	6.4**		1**	7.5**	1 7.5
t <sub>PLH</sub>	A/B	Y	C <sub>L</sub> = 15 pF	5.3**	8.1**		1**	9.5**	1 9.5
t <sub>PHL</sub>				5.3**	8.1**		1**	9.5**	1 9.5
t <sub>PLH</sub>	G	Y	C <sub>L</sub> = 15 pF	5.6**	8.6**		1**	10**	1 10
t <sub>PHL</sub>				5.6**	8.6**		1**	10**	1 10
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 50 pF	5.6	8.7		1	10.8	1 9.8
t <sub>PHL</sub>				5.6	8.7		1	10.8	1 9.8
t <sub>PLH</sub>	A/B	Y	C <sub>L</sub> = 50 pF	6.8	10.4		1	13.2	1 12
t <sub>PLH</sub>				6.8	10.4		1	13.2	1 12
t <sub>PLH</sub>	G	Y	C <sub>L</sub> = 50 pF	7.1	11		1	13.5	1 12
t <sub>PHL</sub>				7.1	11		1	13.5	1 12

\*\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics V<sub>CC</sub> = 5 V, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C (see Note 4)

PARAMETER	SN74AHCT157			UNIT
	MIN	TYP	MAX	
V <sub>OL(P)</sub> Quiet output, maximum dynamic V <sub>OL</sub>			0.4 0.8	V
V <sub>OL(V)</sub> Quiet output, minimum dynamic V <sub>OL</sub>			-0.4 -0.8	V
V <sub>OH(V)</sub> Quiet output, minimum dynamic V <sub>OH</sub>			4.8	V
V <sub>IH(D)</sub> High-level dynamic input voltage			2	V
V <sub>IL(D)</sub> Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are for surface-mount packages only.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

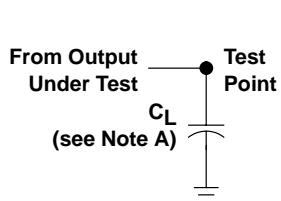


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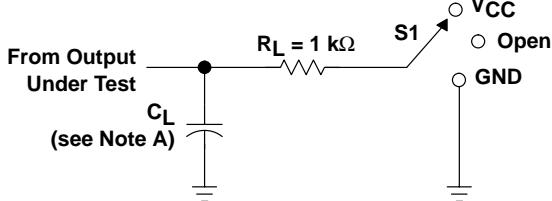
operating characteristics,  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	No load, $f = 1$ MHz	11	pF

### PARAMETER MEASUREMENT INFORMATION

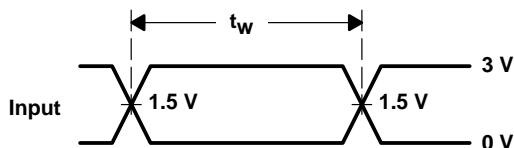


LOAD CIRCUIT FOR  
TOTEM-POLE OUTPUTS

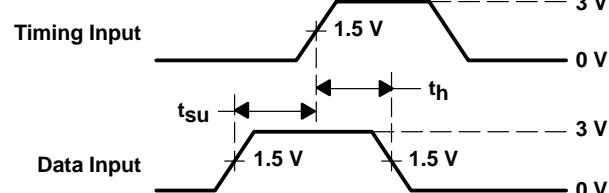


LOAD CIRCUIT FOR  
3-STATE AND OPEN-DRAIN OUTPUTS

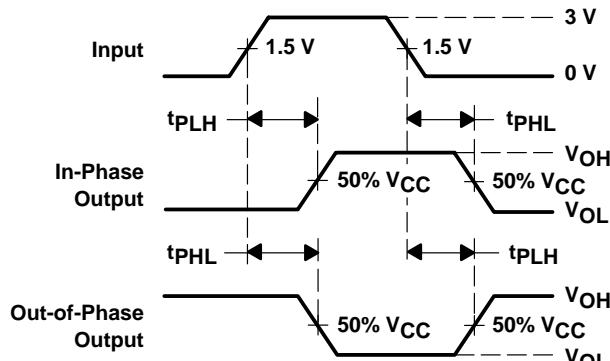
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{CC}$
$t_{PHZ}/t_{PZH}$	GND
	Open Drain
	$V_{CC}$



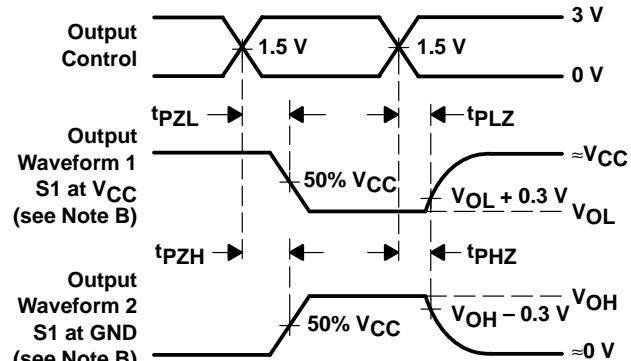
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

NOTES:

- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHCT157D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT157	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHCT157DBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB157	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHCT157DG4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT157	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHCT157DGVR	ACTIVE	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB157	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHCT157DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT157	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHCT157N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHCT157N	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHCT157PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB157	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHCT157PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB157	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

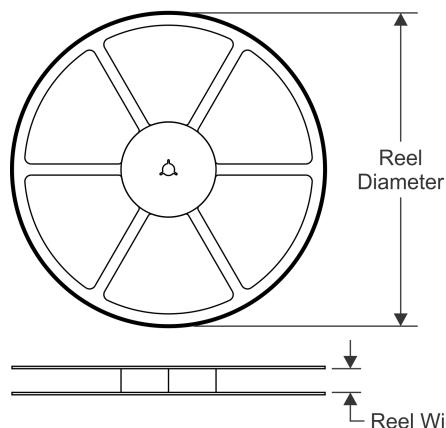
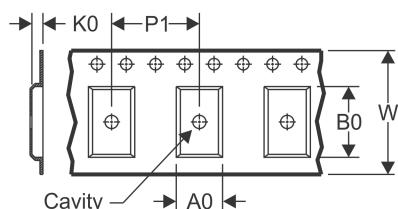
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

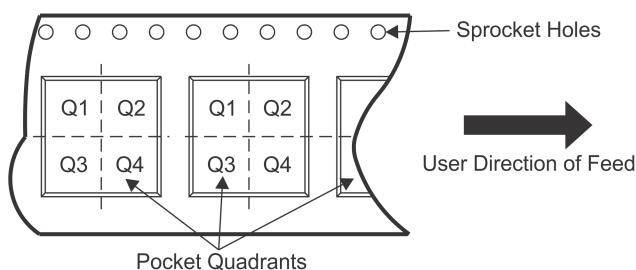
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


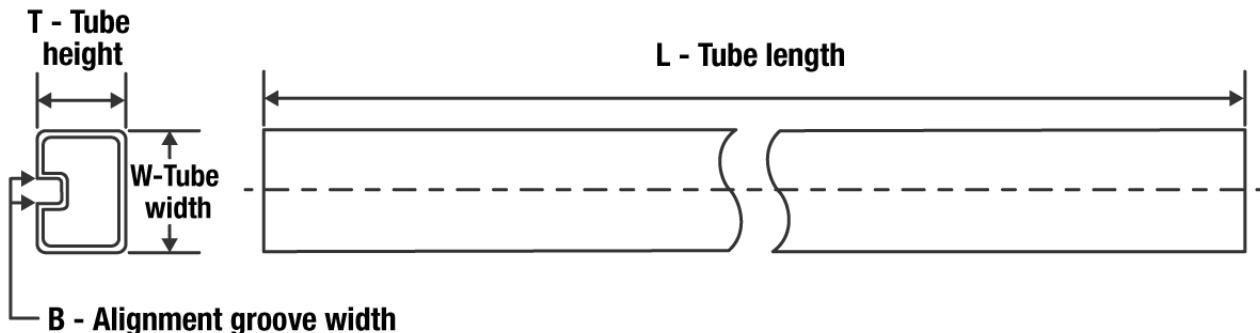
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT157DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHCT157DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHCT157DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHCT157PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT157DBR	SSOP	DB	16	2000	853.0	449.0	35.0
SN74AHCT157DGVR	TVSOP	DGV	16	2000	853.0	449.0	35.0
SN74AHCT157DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74AHCT157PWR	TSSOP	PW	16	2000	853.0	449.0	35.0

**TUBE**


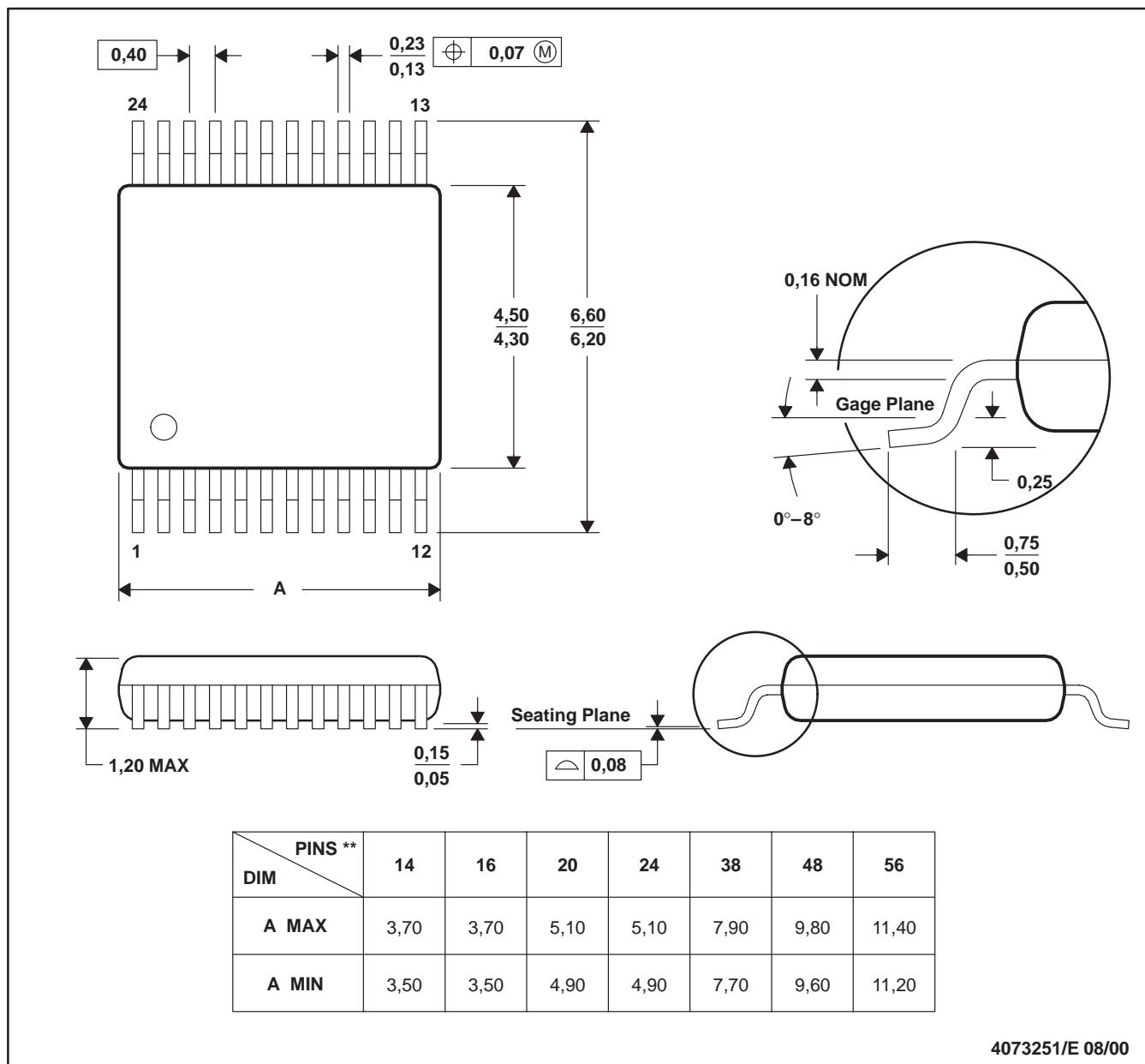
\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74AHCT157D	D	SOIC	16	40	507	8	3940	4.32
SN74AHCT157DG4	D	SOIC	16	40	507	8	3940	4.32
SN74AHCT157N	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHCT157N	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHCT157PW	PW	TSSOP	16	90	530	10.2	3600	3.5

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



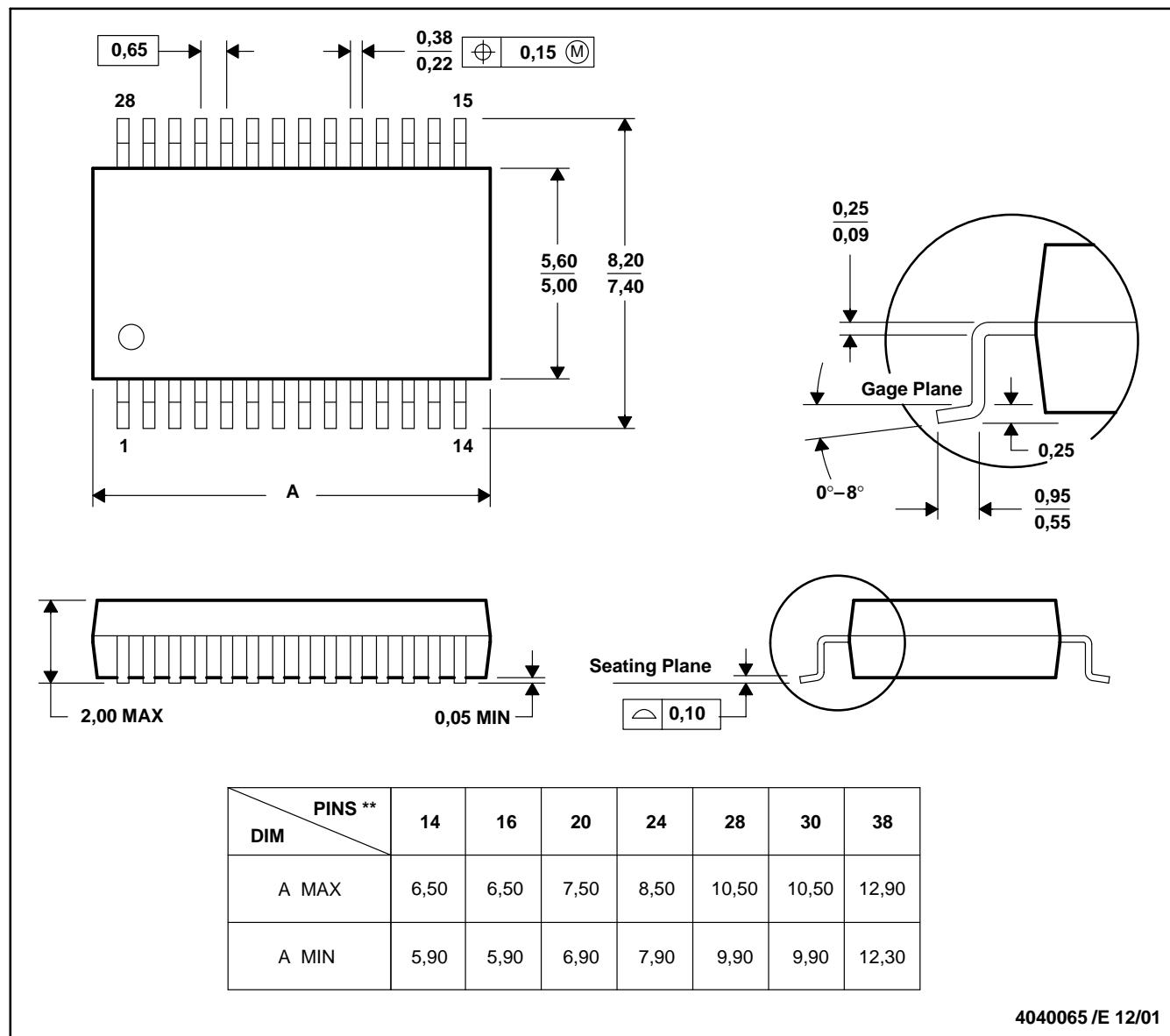
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NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN

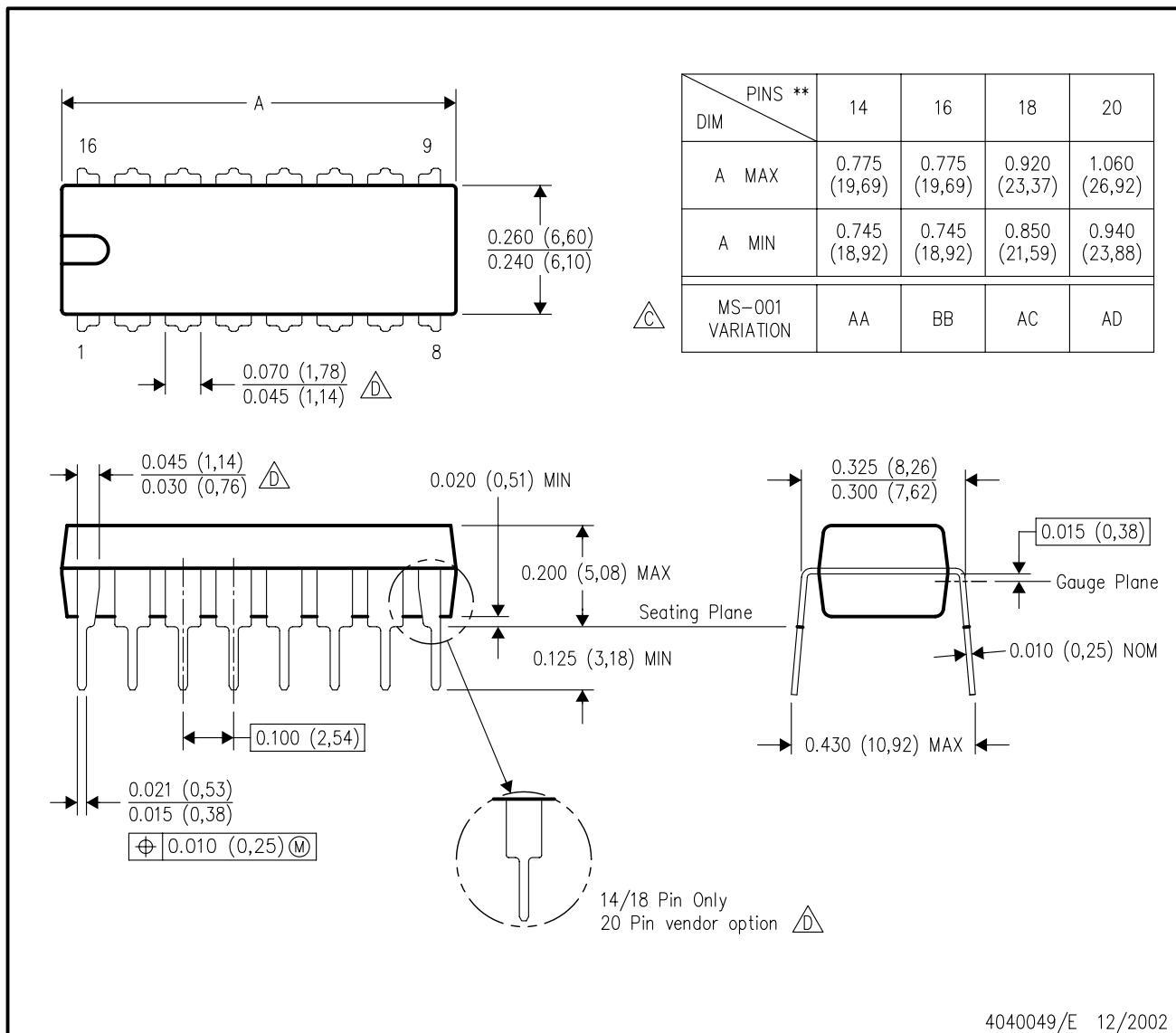


NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

## N (R-PDIP-T\*\*)

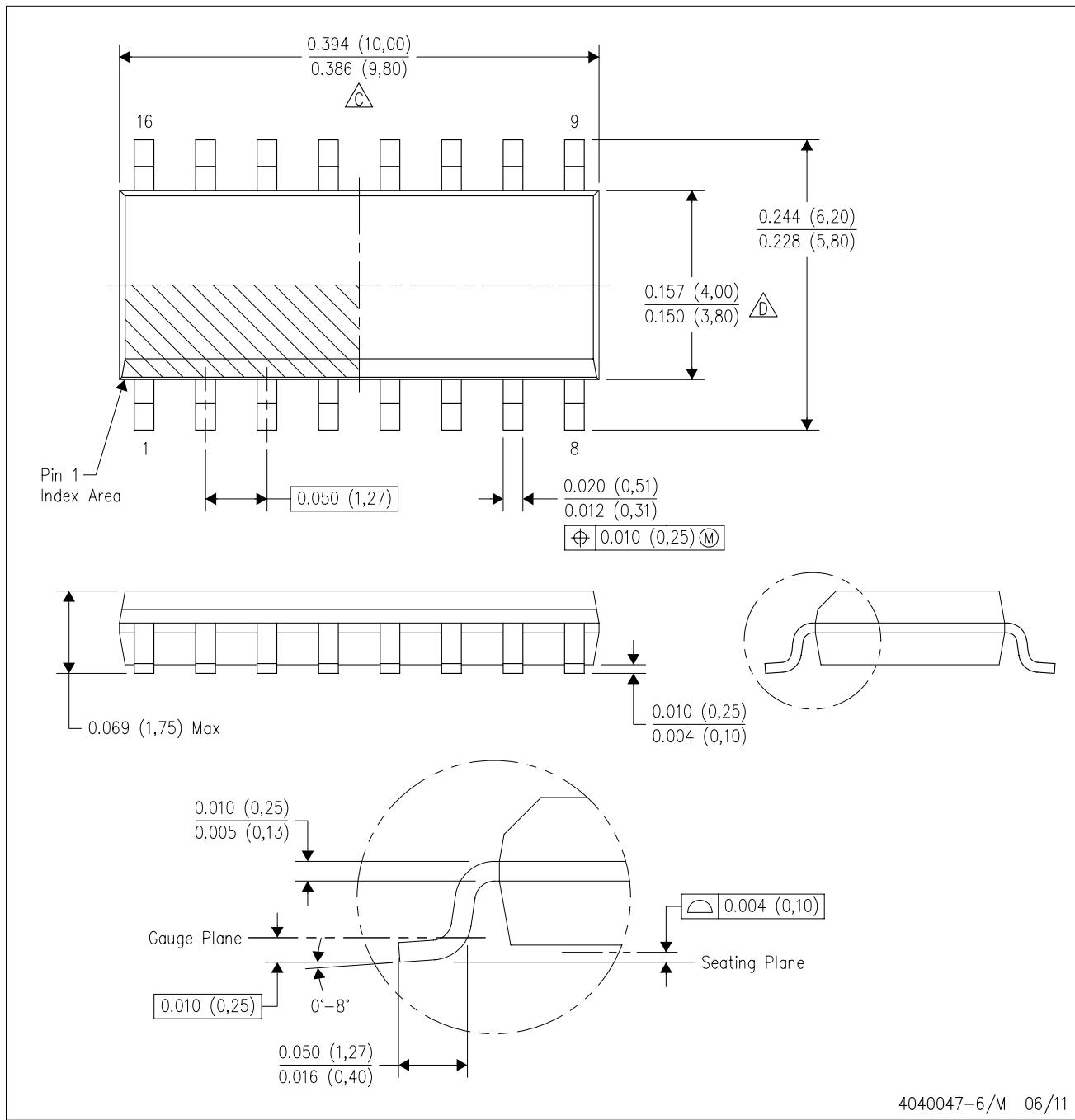
16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

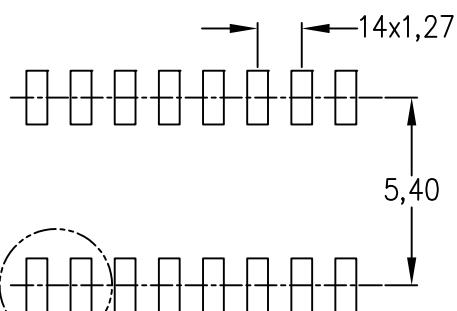
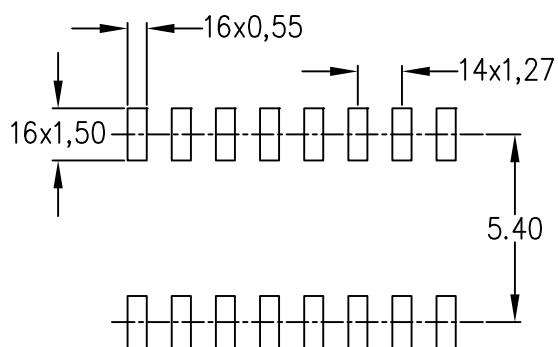
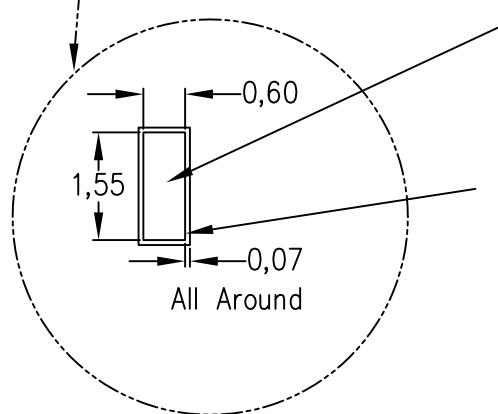
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)Example  
Non Soldermask Defined PadExample  
Pad Geometry  
(See Note C)Example  
Solder Mask Opening  
(See Note E)

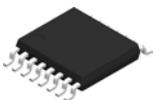
4211283-4/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

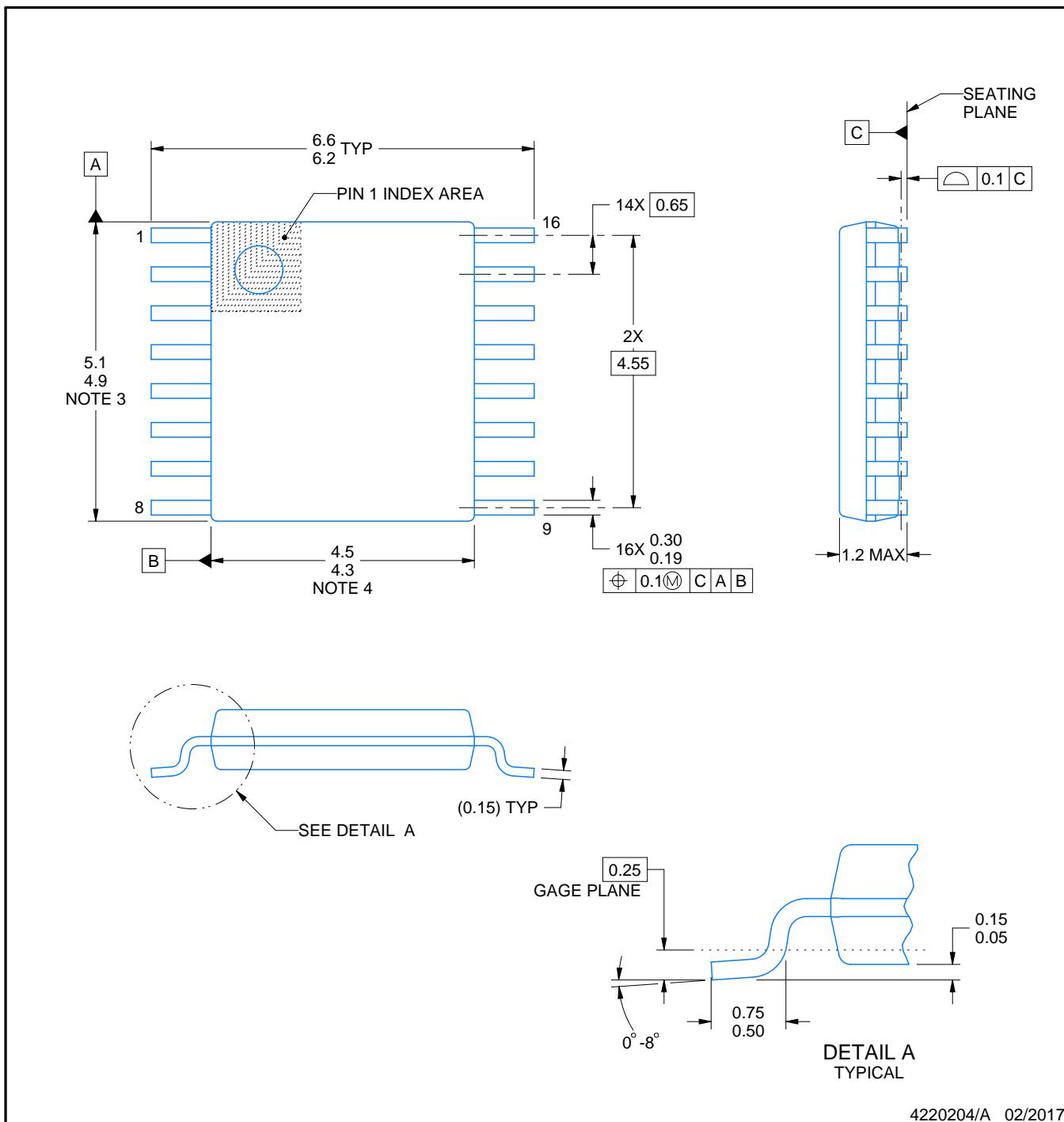
# PACKAGE OUTLINE

PW0016A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



## NOTES:

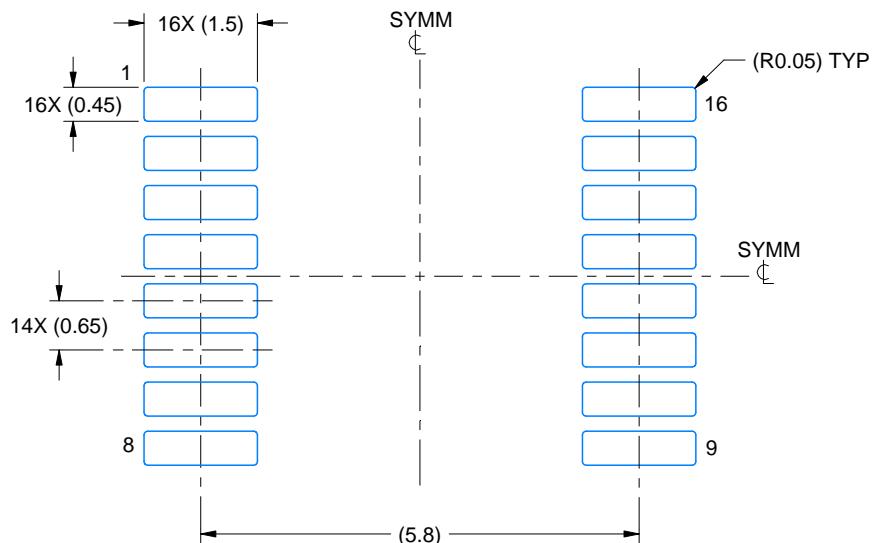
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

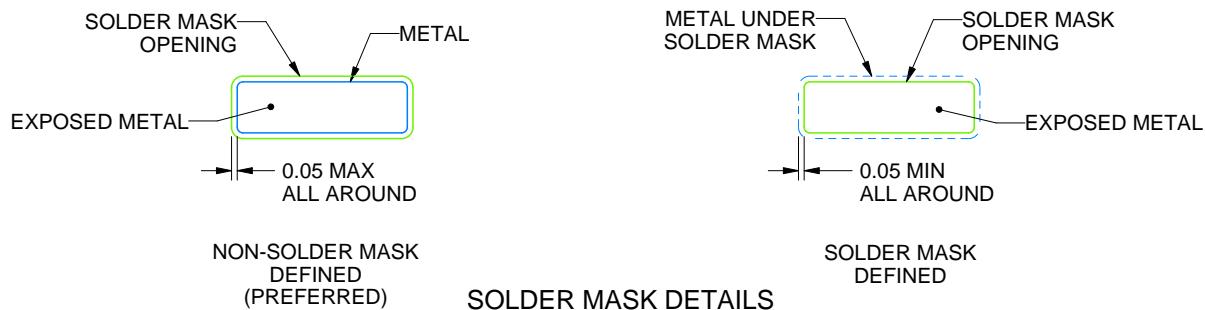
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

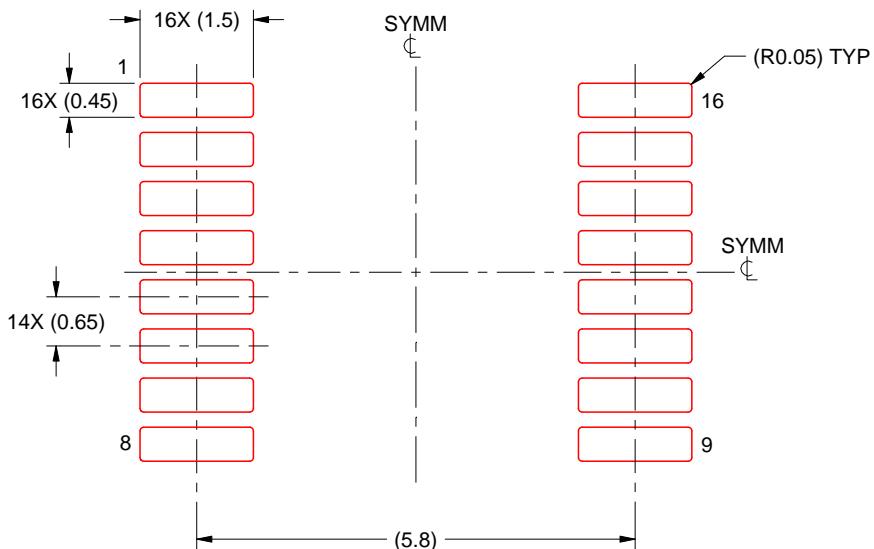
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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