NE521

High-Speed Dual-Differential Comparator/Sense Amp

ON Semiconductor®

http://onsemi.com

Features

- TTL-Compatible Strobes and Outputs
- Large Common-Mode Input Voltage Range
- Operates from Standard Supply Voltages
- Pb−Free Packages are Available

Applications

- MOS Memory Sense Amp
- A-to-D Conversion
- High-Speed Line Receiver

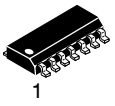
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage Positive Negative	 V+ V−	 +7.0 −7.0	V
Differential Input Voltage	V_{IDR}	±6.0	V
Input Voltage Common Mode Strobe/Gate	V_{IN}	 ±5.0 +5.25	V
Maximum Power Dissipation (Note 1) T_A = 25°C (Still−Air) N Package D Package	P_D	 1420 1040	mW
Thermal Resistance, Junction−to−Ambient N Package D Package	$R_{\theta JA}$	 100 145	°C/W
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature	T_J	150	°C
Lead Soldering Temperature (10 sec max)	T_{sld}	+230	°C

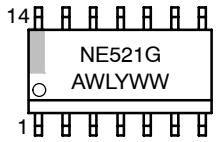
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

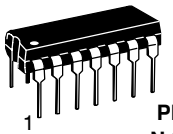
1. Derate above 25°C at the following rates:
   N package at 10 mW/°C
   D package at 6.9 mW/°C.

MARKING DIAGRAMS

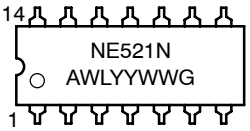


SOIC−14
D SUFFIX
CASE 751A





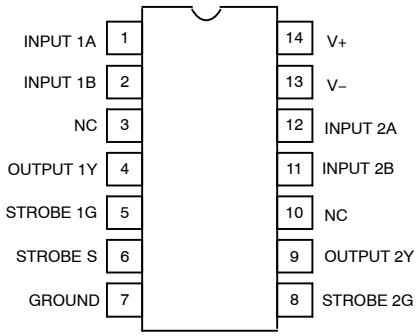
PDIP−14
N SUFFIX
CASE 646



A = Assembly Location
WL = Wafer Lot
Y, YY = Year
WW = Work Week
G = Pb−Free Package

PIN CONNECTIONS

D, N Packages



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

LOGIC FUNCTION TABLE

V_{ID} (A^+, B)	Strobe S	Strobe G	Output (Y)
$V_{ID} \leq -V_{OS}$	H	H	L
$-V_{OS} < V_{ID} < V_{OS}$	H	H	Undefined
$V_{ID} \geq V_{OS}$	H	H	H
X	L	X	H
X	X	L	H

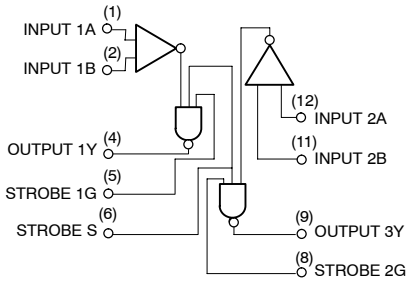


Figure 1. Block Diagram

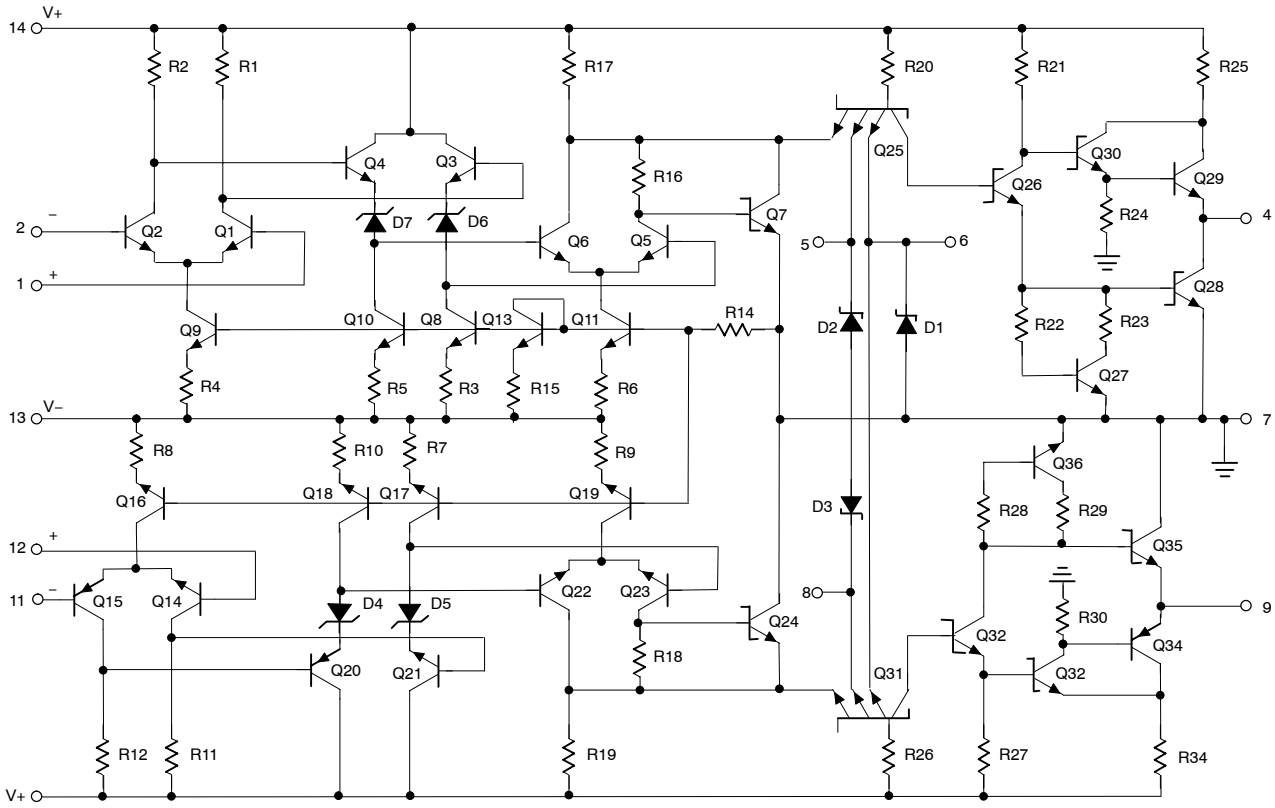


Figure 2. Equivalent Schematic

DC ELECTRICAL CHARACTERISTICS ($V+ = +5.0$ V; $V- = -5.0$ V, $T_A = 0°C$ to $+70°C$, unless otherwise noted.)

Characteristic	Test Conditions	Symbol	Limits			Unit
			Min	Typ	Max	
Input Offset Voltage	$V+ = +4.75$ V; $V- = -4.75$ V	V_{OS}				mV
At 25°C			–	6.0	7.5	
Overtemperature Range			–	–	10	
Input Bias Current	$V+ = +5.25$ V; $V- = -5.25$ V	I_{BIAS}				μA
At 25°C			–	7.5	20	
Overtemperature Range			–	–	40	
Input Offset Current	$V+ = +5.25$ V; $V- = -5.25$ V	I_{OS}				μA
At 25°C			–	1.0	5.0	
Overtemperature Range			–	–	12	
Common-Mode Voltage Range	$V+ = +4.75$ V; $V- = -4.75$ V	V_{CM}	−3.0	–	+3.0	V
Input Current	$V+ = +5.25$ V; $V- = -5.25$ V	I_{IH}				μA
High	$V_{IH} = 2.7$ V					
	1G or 2G Strobe		–	–	50	
	Common Strobe S		–	–	100	
Input Current	$V_{IL} = 0.5$ V	I_{IL}				mA
Low	1G or 2G Strobe		–	–	−2.0	
	Common Strobe S		–	–	−4.0	
Output Voltage	$V_{I(S)} = 2.0$ V					V
High	$V+ = +4.75$ V; $V- = -4.75$ V; $I_{LOAD} = -1.0$ mA	V_{OH}	2.7	3.4		
Low	$V+ = +5.25$ V; $V- = -5.25$ V; $I_{LOAD} = 20$ mA	V_{OL}			0.5	
Supply Voltage						V
Positive	–	$V+$	4.75	5.0	5.25	
Negative		$V-$	−4.75	−5.0	−5.25	
Supply Current	$V+ = +5.25$ V; $V- = -5.25$ V;					mA
Positive	$T_A = 25°C$	I_{CC+}	–	27	35	
Negative		I_{CC-}	–	−15	−28	
Short−Circuit Output Current	–	I_{SC}	−40	–	−100	mA

AC ELECTRICAL CHARACTERISTICS ($T_A = 25°C$; $R_L = 280\ \Omega$; $C_L = 15$ pF, $V+ = 5.0$ V; $V- = 5.0$ V, guaranteed by characterization)

Characteristic	From Input	To Output	Symbol	Limits			Unit
				Min	Typ	Max	
Large−Signal Switching Speed							
Propagation Delay							ns
Low to High (Note 2)	Amp	Output	$t_{PLH(D)}$	–	9.6	12	
High to Low (Note 2)	Amp	Output	$t_{PHL(D)}$	–	8.2	9.0	
Low to High (Note 3)	Strobe	Output	$t_{PLH(S)}$	–	4.8	10	
High to Low (Note 3)	Strobe	Output	$t_{PHL(S)}$	–	3.9	6.0	
Max. Operating Frequency	–	–	f_{MAX}	40	55	–	MHz

2. Response time measured from 0 V point of ± 100 mV_{P-P} 10 MHz square wave to the 1.5 V point of the output.
3. Response time measured from 1.5 V point of input to 1.5 V point of the output.

TYPICAL PERFORMANCE CHARACTERISTICS

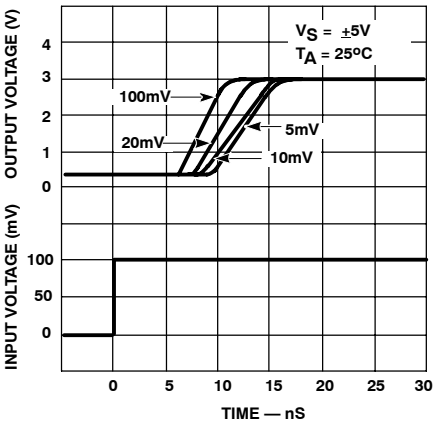


Figure 3. Response Time for Various Input Overdrives

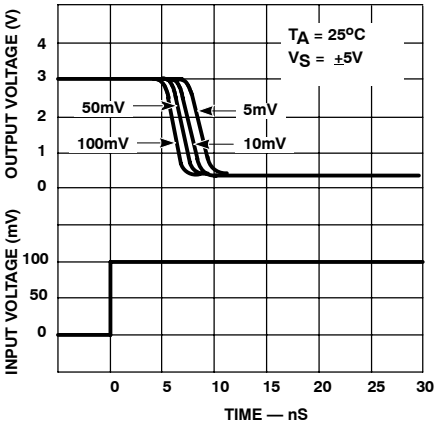


Figure 4. Response Time for Various Input Overdrives

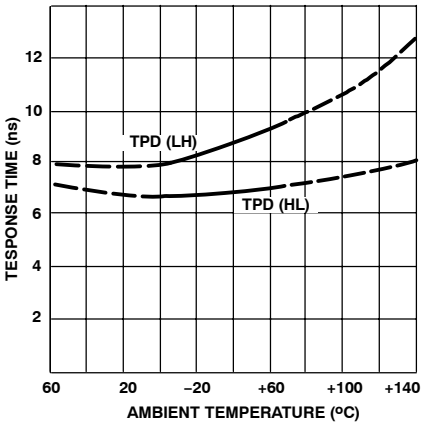


Figure 5. Response Time vs. Temperature

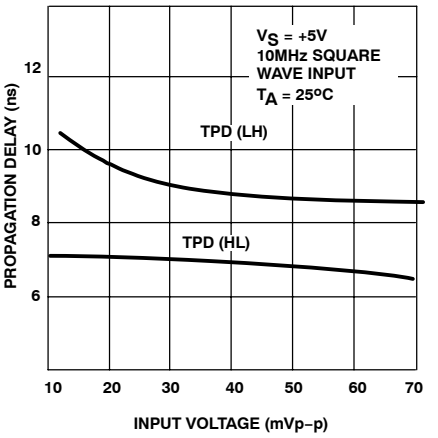


Figure 6. Propagation Delay for Various Input Voltages

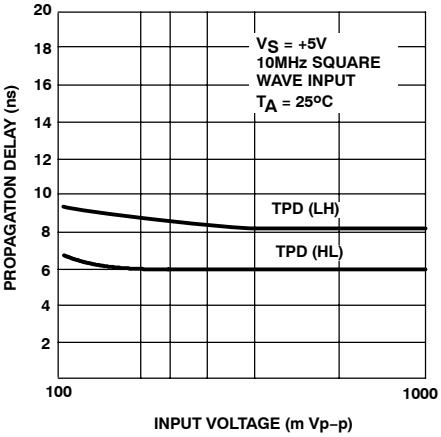


Figure 7. Propagation Delay for Various Input Voltages

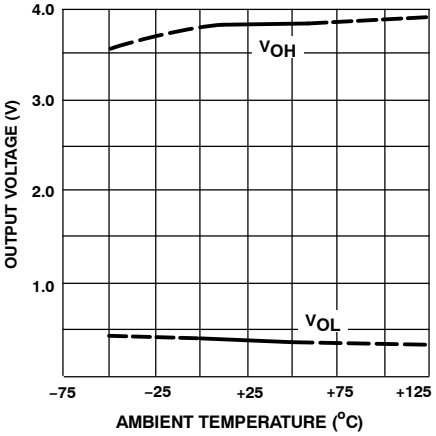


Figure 8. Output Voltage vs. Ambient Temperature

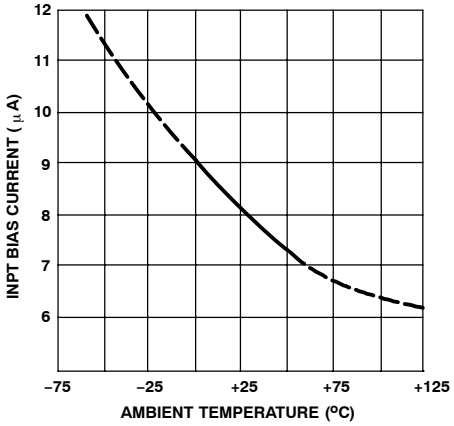


Figure 9. Input Bias Current vs. Ambient Temperature

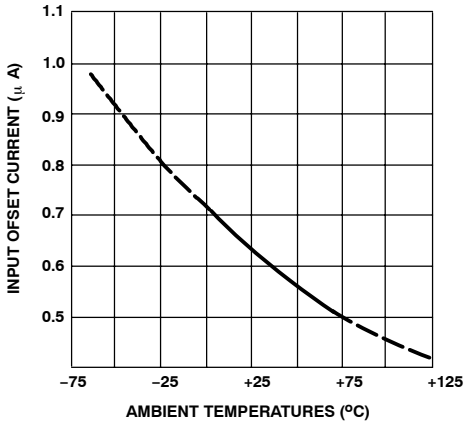


Figure 10. Input Offset Current vs. Ambient Temperature

ORDERING INFORMATION

Device	Temperature Range	Package	Shipping†
NE521D	0 to +70°C	SOIC−14	55 Units/Rail
NE521DG		SOIC−14 (Pb−Free)	
NE521DR2		SOIC−14	2500/Tape & Reel
NE521DR2G		SOIC−14 (Pb−Free)	
NE521N		PDIP−14	25 Units/Rail
NE521NG		PDIP−14 (Pb−Free)	

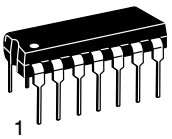
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

PDIP−14
CASE 646−06
ISSUE S

DATE 22 APR 2015



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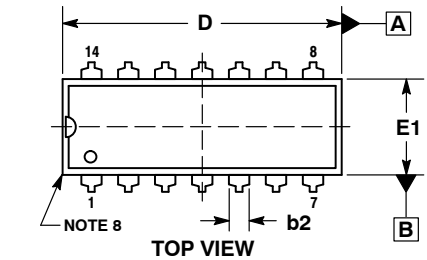
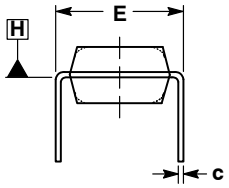
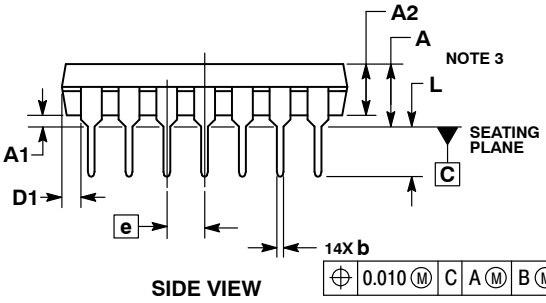


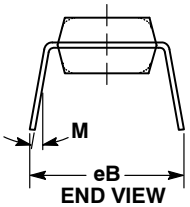
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW

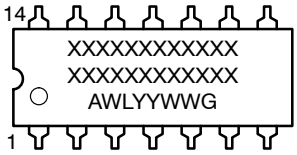


END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.735	0.775	18.67	19.69
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42428B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	PDIP−14		PAGE 1 OF 2

PDIP−14
CASE 646−06
ISSUE S

DATE 22 APR 2015

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. NO CONNECTION
5. GATE
6. SOURCE
7. DRAIN
8. DRAIN
9. SOURCE
10. GATE
11. NO CONNECTION
12. GATE
13. SOURCE
14. DRAIN

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. NO CONNECTION
5. SOURCE
6. DRAIN
7. GATE
8. GATE
9. DRAIN
10. SOURCE
11. NO CONNECTION
12. SOURCE
13. DRAIN
14. GATE

STYLE 6:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 7:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 8:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 9:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

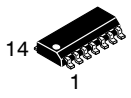
STYLE 10:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 11:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 12:
PIN 1. COMMON CATHODE
2. COMMON ANODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. COMMON ANODE
7. COMMON CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. ANODE/CATHODE
14. ANODE/CATHODE

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

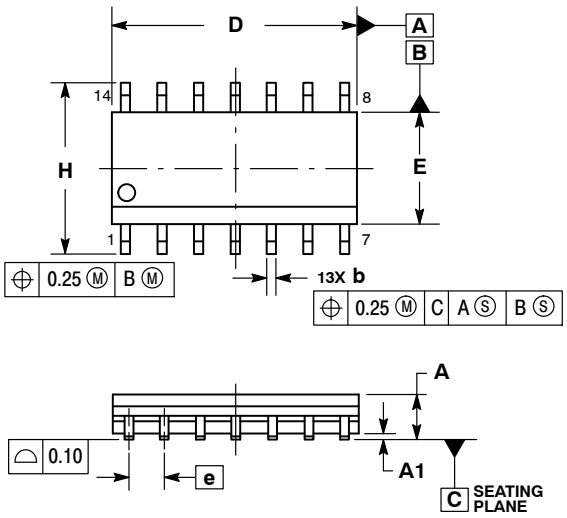
ON Semiconductor®

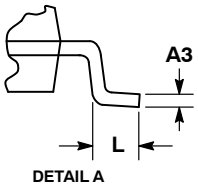


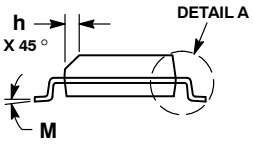
SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



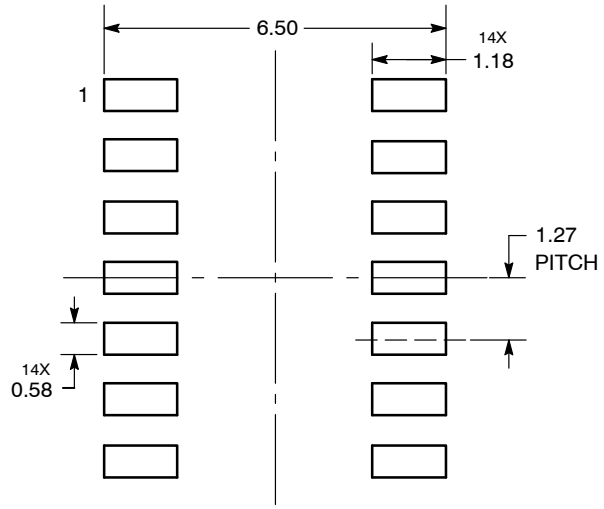




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

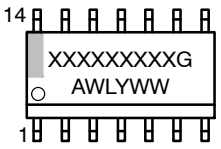
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLES ON PAGE 2

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SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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