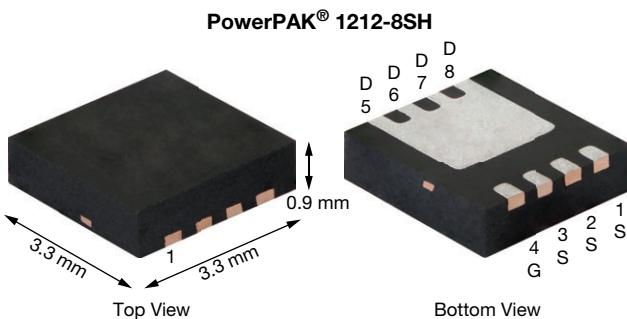


## N-Channel 20 V (D-S) Fast Switching MOSFET



### FEATURES

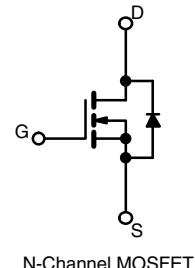
- TrenchFET® power MOSFET
- 2.5 V rated  $R_{DS(on)}$
- PWM optimized
- 100 %  $R_g$  tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



RoHS  
COMPLIANT  
HALOGEN  
FREE

### APPLICATIONS

- Synchronous rectification
- Load switch



### PRODUCT SUMMARY

$V_{DS}$ (V)	20
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5$ V	0.0062
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 2.5$ V	0.0098
$Q_g$ typ. (nC)	17.5
$I_D$ (A)	19.5
Configuration	Single

### ORDERING INFORMATION

Package	PowerPAK 1212-8
Lead (Pb)-free and halogen-free	SiSH106DN-T1-GE3

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	10 s	STEADY STATE	UNIT
Drain-source voltage	$V_{DS}$	20	20	V
Gate-source voltage	$V_{GS}$	$\pm 12$	$\pm 12$	
Continuous drain current ( $T_J = 150$ °C) <sup>a</sup>	$I_D$	19.5	12.5	A
		15.6	10	
Pulsed drain current	$I_{DM}$	60	60	
Continuous source current (diode conduction) <sup>a</sup>	$I_S$	3.2	1.3	
Single avalanche current	$I_{AS}$	30	30	mJ
Single avalanche energy	$E_{AS}$	45	45	
Maximum power dissipation <sup>a</sup>	$P_D$	3.8	1.5	W
		2	0.8	
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150		°C
Soldering recommendations (peak temperature) <sup>b, c</sup>		260		

### THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient <sup>a</sup>	$R_{thJA}$	24	33	°C/W
		65	81	
Maximum junction-to-case (drain)	$R_{thJC}$	1.9	2.4	

#### Notes

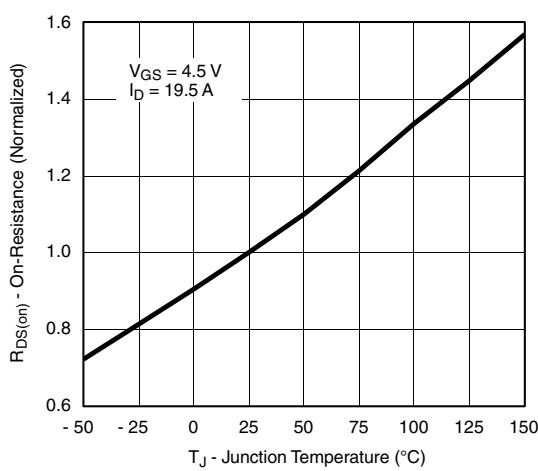
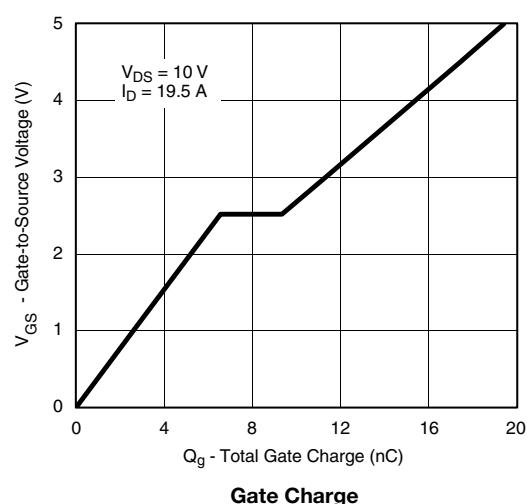
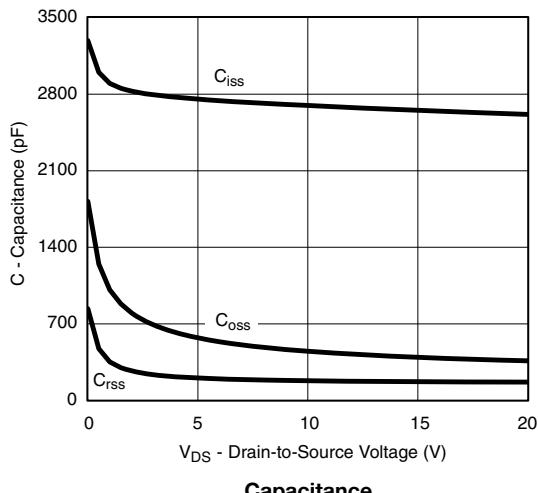
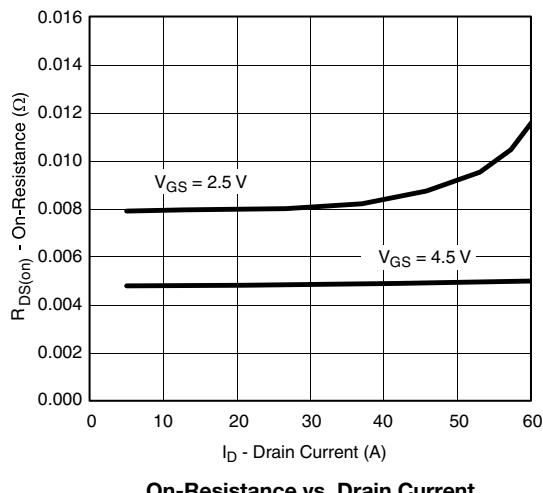
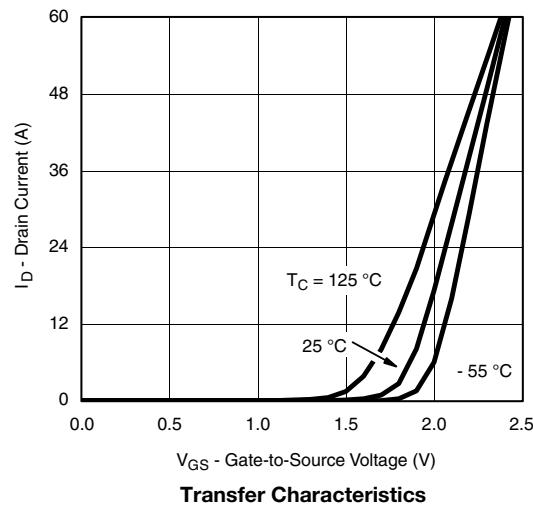
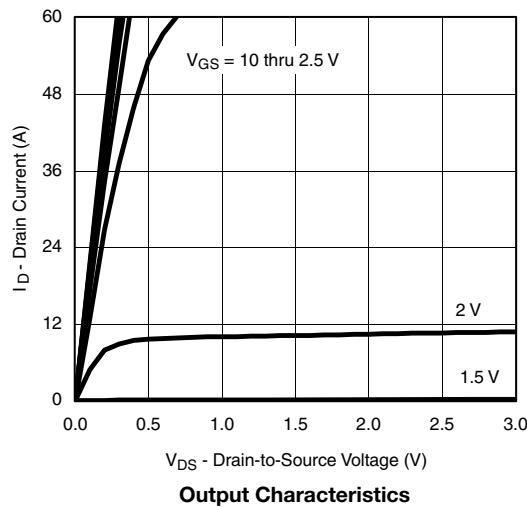
- Surface mounted on 1" x 1" FR4 board
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK 1212-8SH is a leadless package within the PowerPAK 1212-8 package family. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

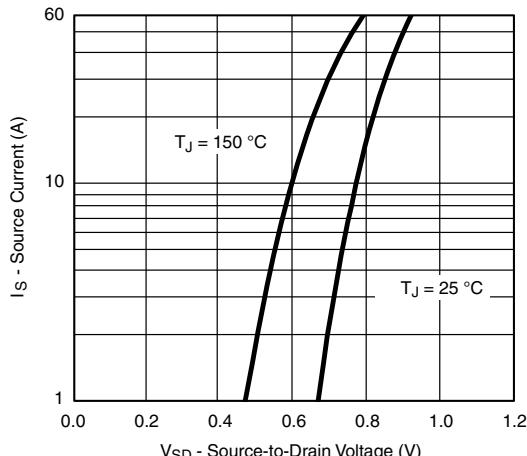
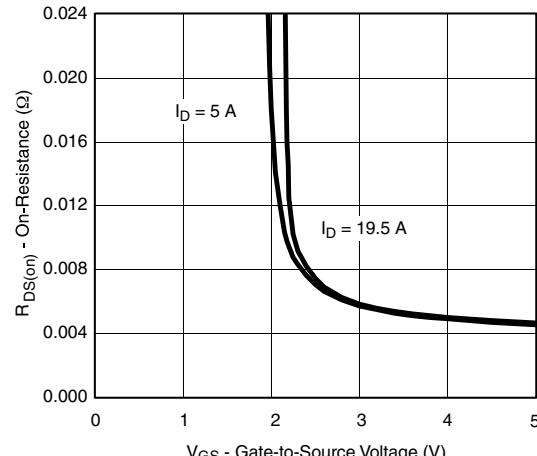
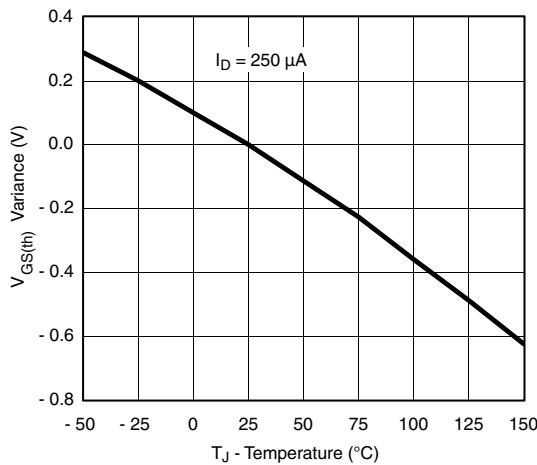
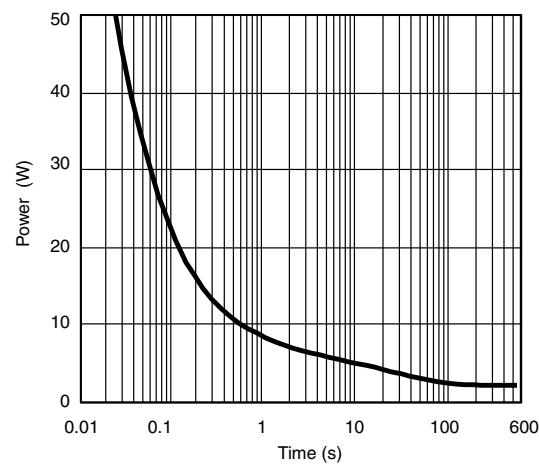
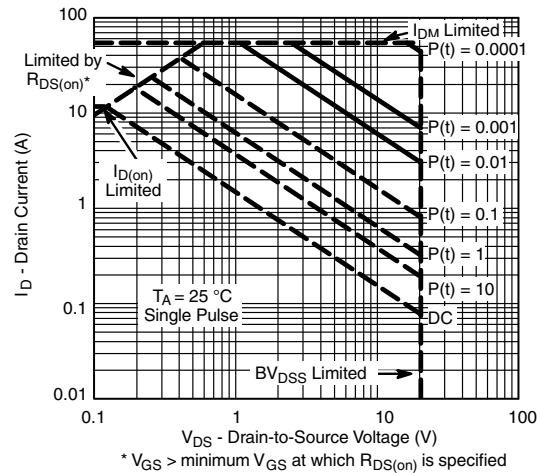
<b>SPECIFICATIONS</b> ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Gate threshold voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$ , $I_D = 250 \mu\text{A}$	0.6	-	1.5	V
Gate-body leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}$ , $V_{GS} = \pm 12 \text{ V}$	-	-	$\pm 100$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 20 \text{ V}$ , $V_{GS} = 0 \text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 20 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $T_J = 55^\circ\text{C}$	-	-	5	
On-state drain current <sup>a</sup>	$I_{D(\text{on})}$	$V_{DS} \geq 5 \text{ V}$ , $V_{GS} = 4.5 \text{ V}$	40	-	-	A
Drain-source on-state resistance <sup>a</sup>	$R_{DS(\text{on})}$	$V_{GS} = 4.5 \text{ V}$ , $I_D = 19.5 \text{ A}$	-	0.0051	0.0062	$\Omega$
		$V_{GS} = 2.5 \text{ V}$ , $I_D = 15.5 \text{ A}$	-	0.0081	0.0098	
Forward transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15 \text{ V}$ , $I_D = 19.5 \text{ A}$	-	105	-	S
Diode forward voltage <sup>a</sup>	$V_{SD}$	$I_S = 3.2 \text{ A}$ , $V_{GS} = 0 \text{ V}$	-	0.8	1.2	V
<b>Dynamic <sup>b</sup></b>						
Total gate charge	$Q_g$	$V_{DS} = 10 \text{ V}$ , $V_{GS} = 4.5 \text{ V}$ , $I_D = 19.5 \text{ A}$	-	17.5	27	nC
Gate-source charge	$Q_{gs}$		-	6.6	-	
Gate-drain charge	$Q_{gd}$		-	2.8	-	
Gate resistance	$R_g$	$f = 1 \text{ MHz}$	0.7	1.4	2.1	$\Omega$
Turn-on delay time	$t_{d(\text{on})}$	$V_{DD} = 10 \text{ V}$ , $R_L = 10 \Omega$ $I_D \geq 1 \text{ A}$ , $V_{GEN} = 10 \text{ V}$ , $R_g = 6 \Omega$	-	25	40	ns
Rise time	$t_r$		-	15	25	
Turn-off delay time	$t_{d(\text{off})}$		-	50	75	
Fall time	$t_f$		-	12	20	
Source-drain reverse recovery time	$t_{rr}$	$I_F = 3.2 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$	-	30	60	

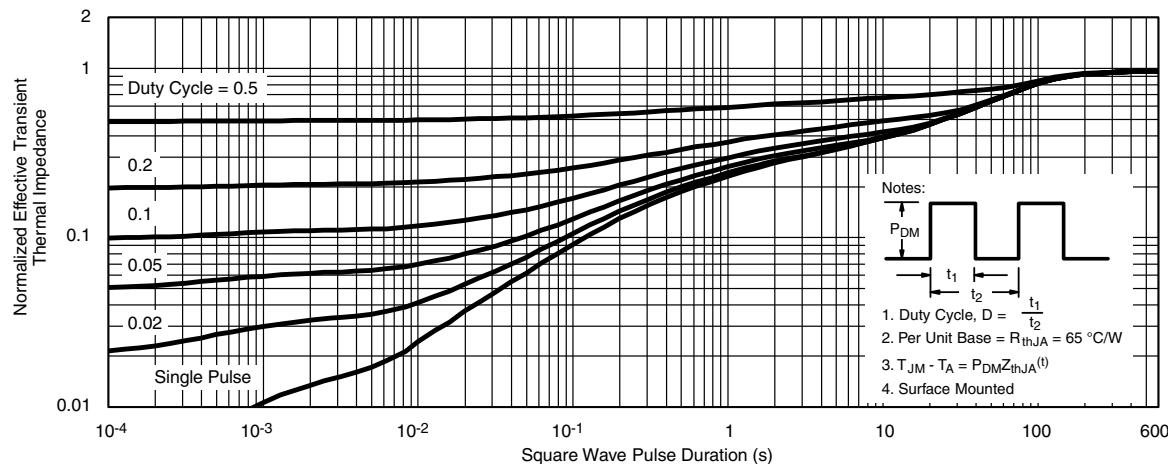
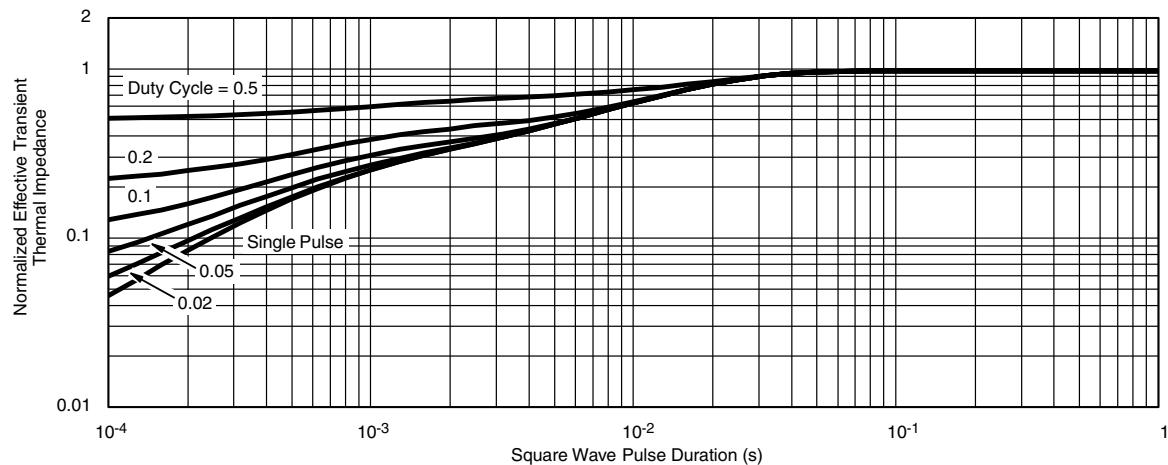
**Notes**

- a. Pulse test; pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2 \%$
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

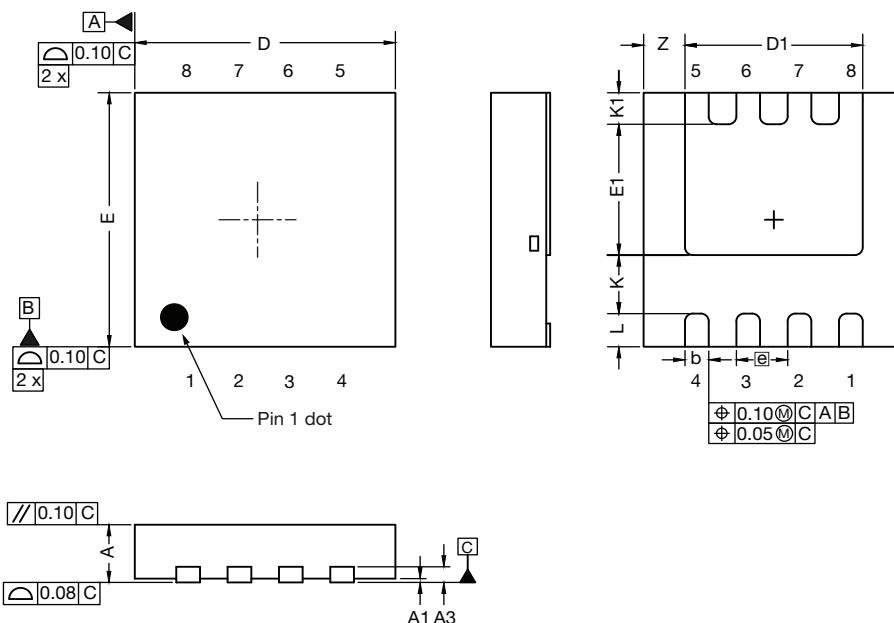
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)


**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Source-Drain Diode Forward Voltage**

**On-Resistance vs. Gate-to-Source Voltage**

**Threshold Voltage**

**Single Pulse Power, Junction-to-Ambient**

**Safe Operating Area**

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Normalized Thermal Transient Impedance, Junction-to-Ambient**

**Normalized Thermal Transient Impedance, Junction-to-Case**

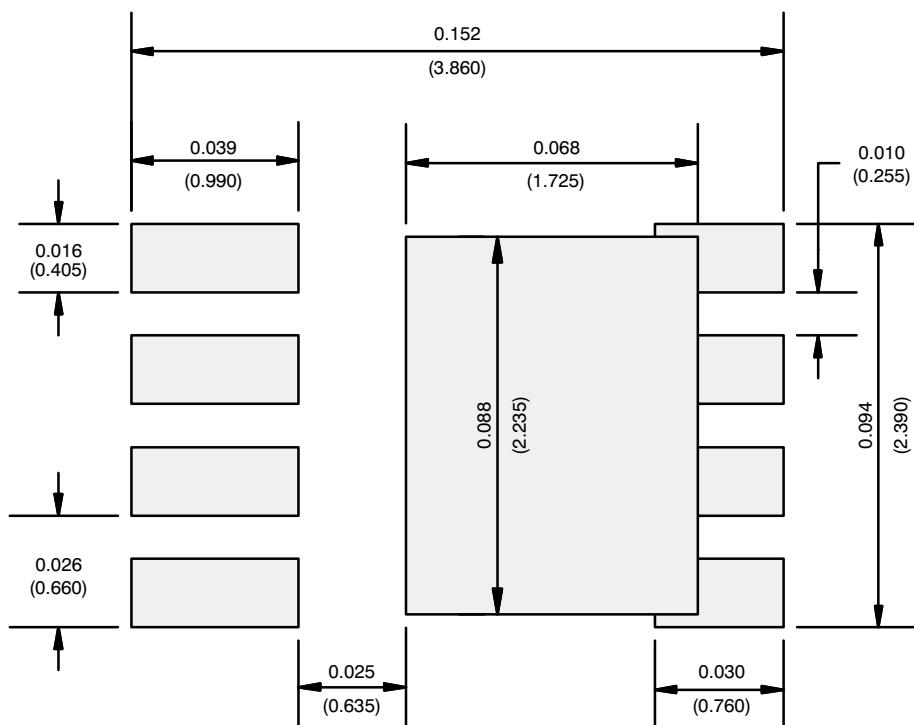
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## Case Outline for PowerPAK® 1212-SWLH and PowerPAK® 1212-8SH



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.82	0.90	0.98	0.032	0.035	0.038
A1	0.00	-	0.05	0.000	-	0.002
A3	0.20 ref.			0.008 ref.		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.15	2.25	2.35	0.085	0.089	0.093
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	1.60	1.70	1.80	0.063	0.067	0.071
e	0.65 bsc.			0.026 bsc.		
K	0.76 ref.			0.030 ref.		
K1	0.41 ref.			0.016 ref.		
L	0.33	0.43	0.53	0.013	0.017	0.021
Z	0.525 ref.			0.021 ref.		

ECN: S20-0930-Rev. C, 07-Dec-2020  
DWG: 6062

**RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single**

Recommended Minimum Pads  
Dimensions in Inches/(mm)

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