



PSMN013-100BS

N-channel 100V 13.9mΩ standard level MOSFET in D2PAK

21 February 2014

Product data sheet

1. General description

Standard level N-channel MOSFET in D2PAK package qualified to 175°C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

2. Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive

3. Applications

- DC-to-DC converters
- Load switching
- Motor control
- Server power supplies

4. Quick reference data

Table 1. Quick reference data

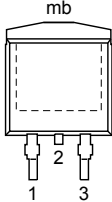
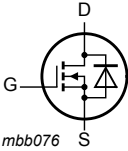
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	-	100	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; Fig. 2	[1]	-	-	68	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	-	170	W
T _j	junction temperature			-55	-	175	°C
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 15 A; T _j = 100 °C; Fig. 12 ; Fig. 13		-	19.4	25	mΩ
		V _{GS} = 10 V; I _D = 15 A; T _j = 25 °C; Fig. 13		-	10.8	13.9	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	V _{GS} = 10 V; I _D = 25 A; V _{DS} = 50 V; Fig. 15 ; Fig. 14		-	17	23.8	nC
Q _{G(tot)}	total gate charge	V _{GS} = 10 V; I _D = 25 A; V _{DS} = 50 V; Fig. 14 ; Fig. 15		-	59	83	nC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 68\text{ A}$; $V_{sup} \leq 100\text{ V}$; unclamped; $R_{GS} = 50\text{ }\Omega$	-	-	127	mJ

[1] Continuous current is limited by package

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 D2PAK (SOT404)	 mbb076
2	D	drain[1]		
3	S	source		
mb	D	mounting base; connected to drain		

[1] It is not possible to make connection to pin 2.

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN013-100BS	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN013-100BS	PSMN013-100BS

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	100	V
V_{DGR}	drain-gate voltage	$T_j \leq 175\text{ °C}$; $T_j \geq 25\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	100	V

Symbol	Parameter	Conditions		Min	Max	Unit
V _{GS}	gate-source voltage			-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	170	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2	[1]	-	47	A
		V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	[1]	-	68	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3		-	272	A
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
T _{sld(M)}	peak soldering temperature			-	260	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C	[1]	-	68	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	272	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 68 A; V _{sup} ≤ 100 V; unclamped; R _{GS} = 50 Ω		-	127	mJ

[1] Continuous current is limited by package

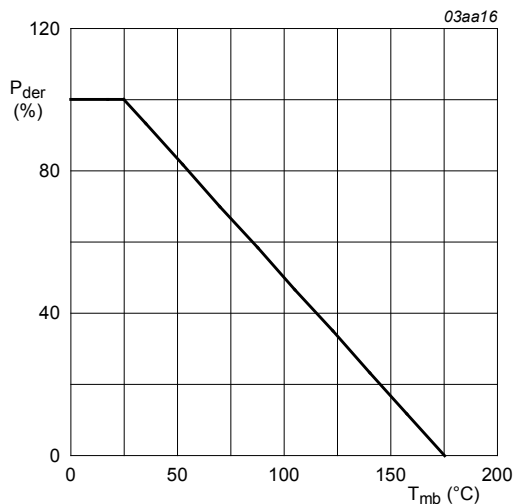


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

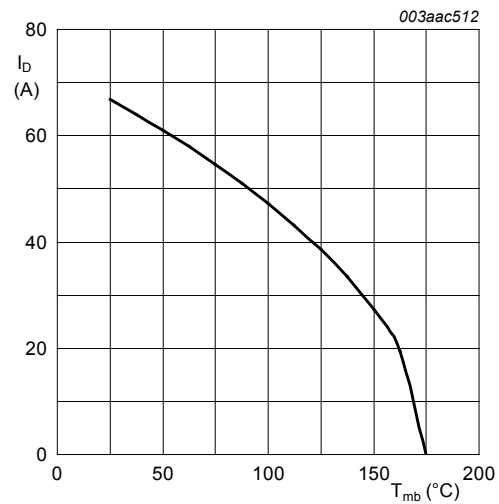
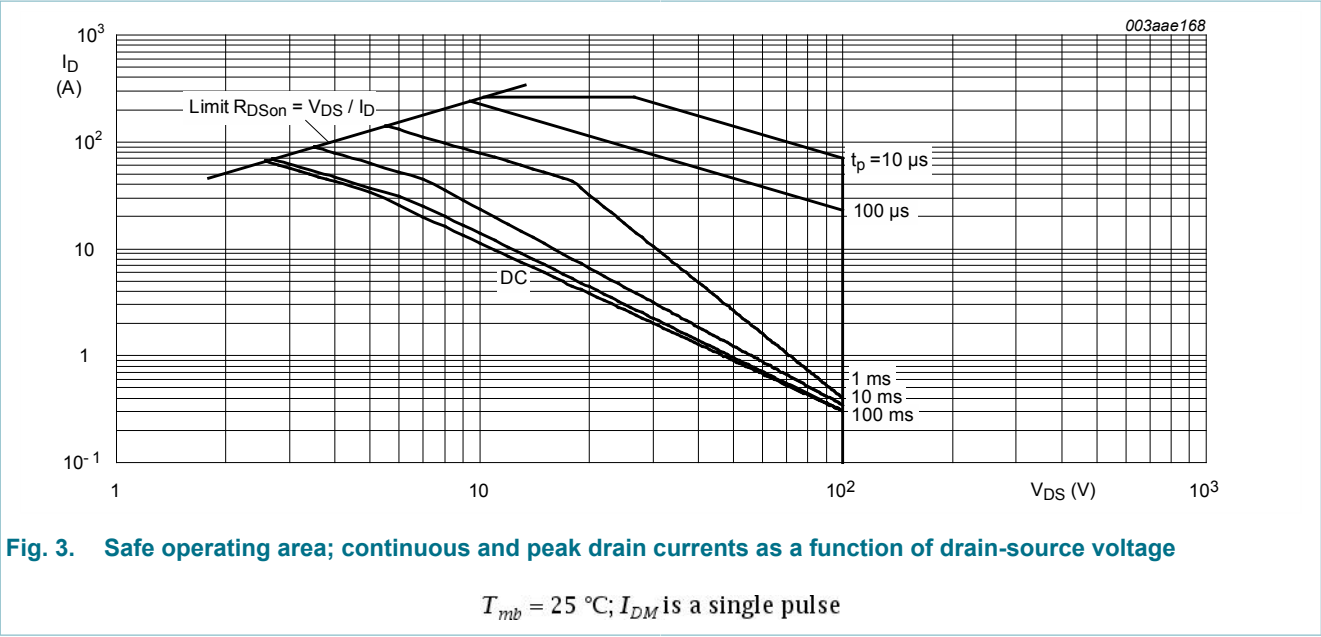


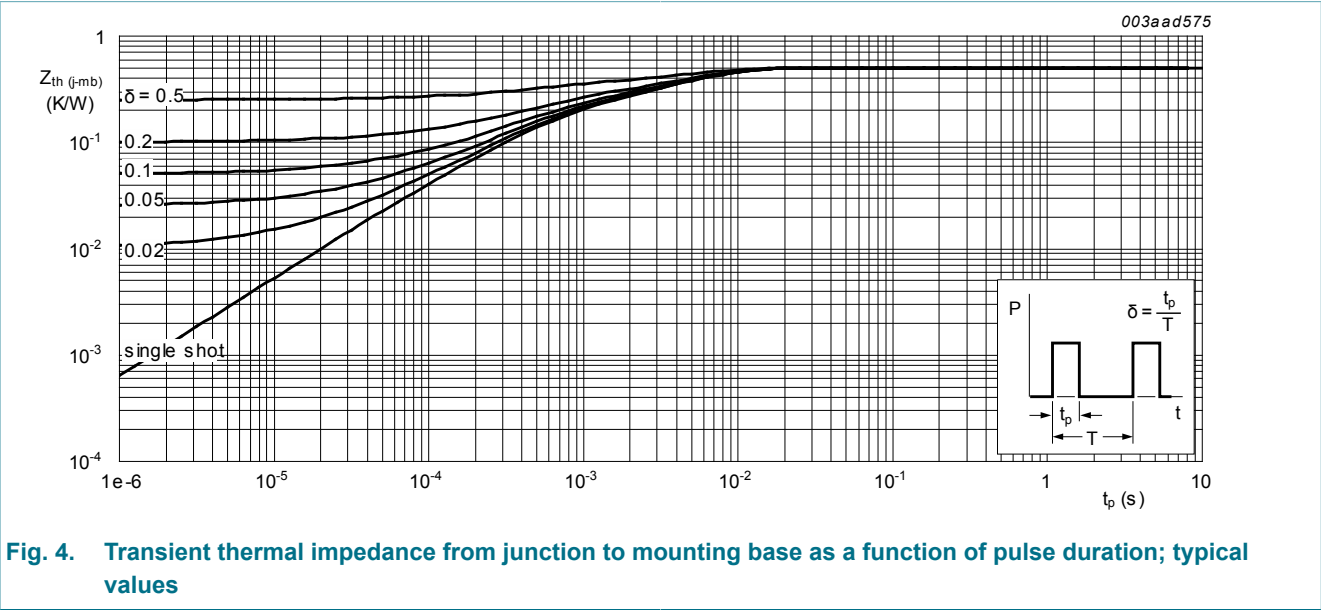
Fig. 2. Continuous drain current as a function of mounting base temperature



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.5	0.9	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a printed-circuit board	-	50	-	K/W



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_J = -55 \text{ }^\circ\text{C}$	90	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_J = 25 \text{ }^\circ\text{C}$	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_J = 175 \text{ }^\circ\text{C};$ Fig. 10	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_J = 25 \text{ }^\circ\text{C};$ Fig. 10; Fig. 11	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_J = -55 \text{ }^\circ\text{C};$ Fig. 10	-	-	4.6	V
I_{DSS}	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_J = 125 \text{ }^\circ\text{C}$	-	-	100	μA
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_J = 25 \text{ }^\circ\text{C}$	-	0.06	2	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_J = 25 \text{ }^\circ\text{C}$	-	10	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_J = 25 \text{ }^\circ\text{C}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_J = 100 \text{ }^\circ\text{C};$ Fig. 12; Fig. 13	-	19.4	25	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_J = 175 \text{ }^\circ\text{C};$ Fig. 12; Fig. 13	-	29.5	38.9	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_J = 25 \text{ }^\circ\text{C};$ Fig. 13	-	10.8	13.9	mΩ
R_G	gate resistance	$f = 1 \text{ MHz}$	0.5	1	2	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ Fig. 14; Fig. 15	-	59	83	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	47.6	66.7	nC
Q_{GS}	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ Fig. 14; Fig. 15	-	13.8	19.4	nC
$Q_{GS(th)}$	pre-threshold gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ Fig. 15; Fig. 14	-	9.2	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	4.6	-	nC
Q_{GD}	gate-drain charge		-	17	23.8	nC
$V_{GS(pl)}$	gate-source plateau voltage	$V_{DS} = 50 \text{ V};$ Fig. 15; Fig. 14	-	4.4	-	V
C_{iss}	input capacitance	$V_{DS} = 50 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$	-	3195	4315	pF
C_{oss}	output capacitance	$T_J = 25 \text{ }^\circ\text{C};$ Fig. 16	-	221	300	pF

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C _{rss}	reverse transfer capacitance	V _{DS} = 50 V; R _L = 2 Ω; V _{GS} = 10 V; R _{G(ext)} = 4.7 Ω; T _j = 25 °C		-	136	191	pF
t _{d(on)}	turn-on delay time			-	20.7	31.1	ns
t _r	rise time			-	25	37.5	ns
t _{d(off)}	turn-off delay time			-	52.5	78.8	ns
t _f	fall time			-	24	36	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 15 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 17		-	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 25 A; dI _S /dt = 100 A/μs; V _{GS} = 0 V; V _{DS} = 50 V		-	52	68	ns
Q _r	recovered charge			-	109	142	nC

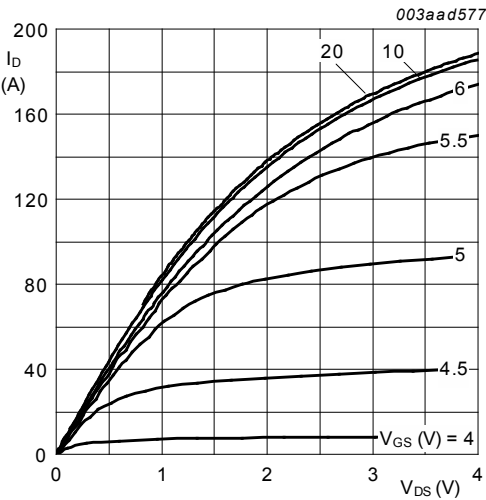


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_j = 25\text{ }^{\circ}\text{C}$

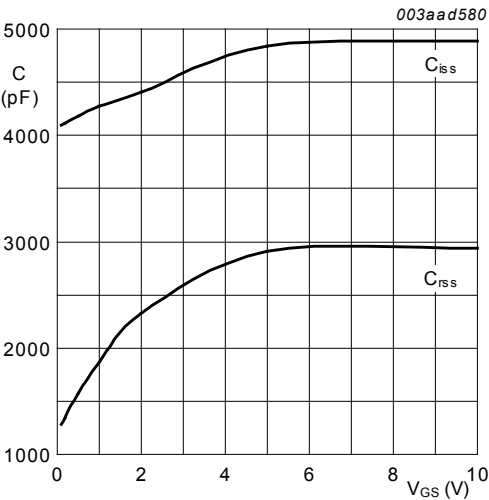


Fig. 6. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

$V_{DS} = 0\text{ V}; f = 1\text{ MHz}$

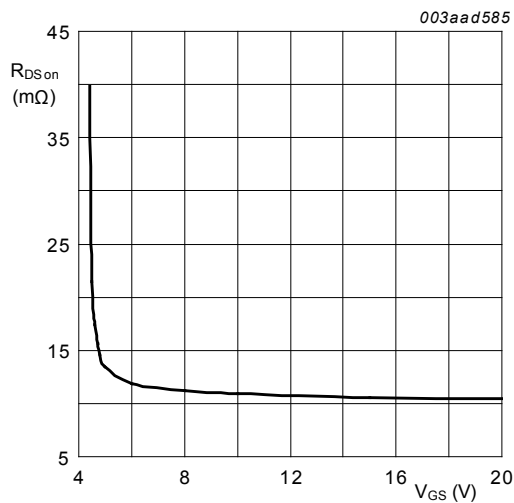


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$$T_J = 25\text{ °C}$$

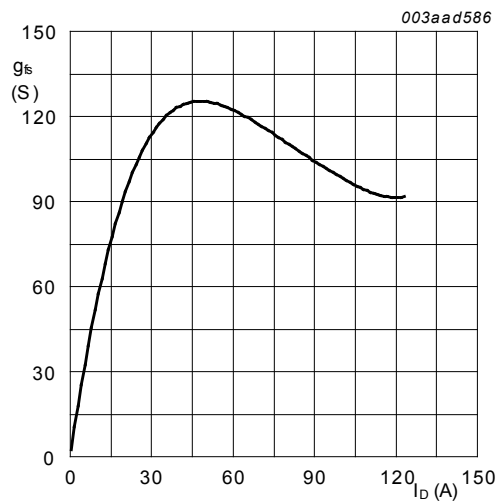


Fig. 8. Forward transconductance as a function of drain current; typical values

$$T_J = 25\text{ °C}; V_{DS} = 15\text{ V}$$

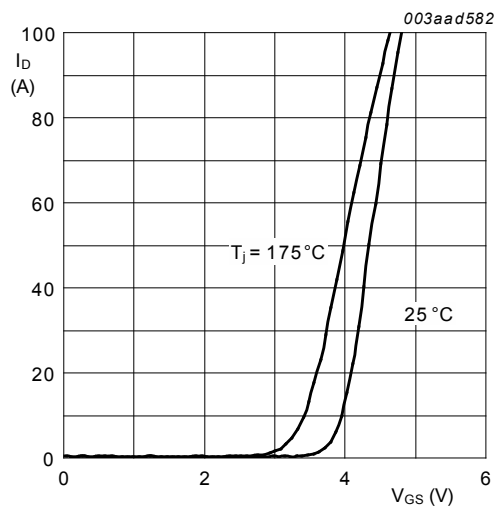


Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$$V_{DS} > I_D \times R_{DS(on)}$$

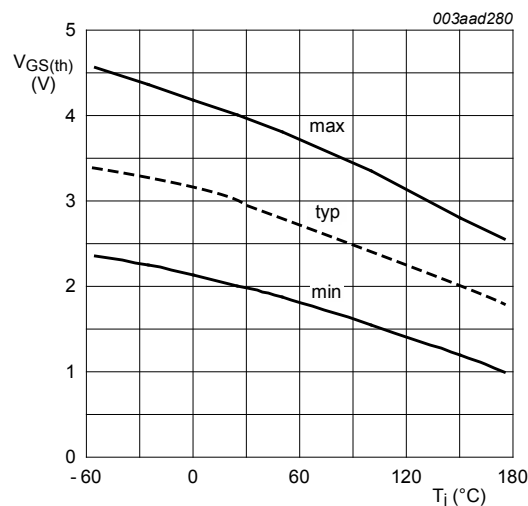


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1\text{ mA}; V_{DS} = V_{GS}$$

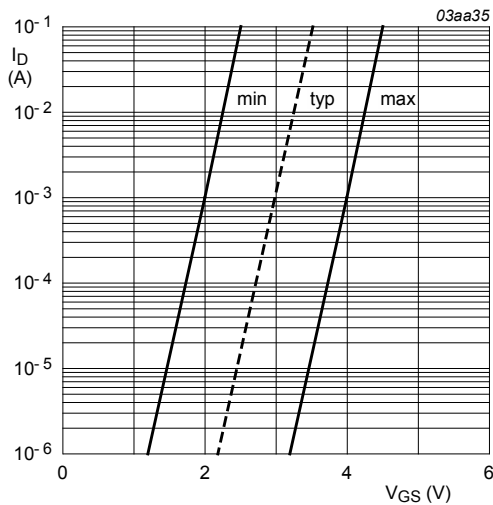


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25\text{ }^{\circ}\text{C}; V_{DS} = 5\text{ V}$

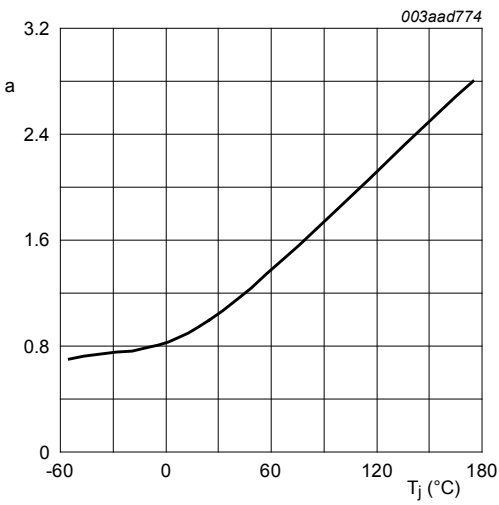


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25\text{ }^{\circ}\text{C})}}$$

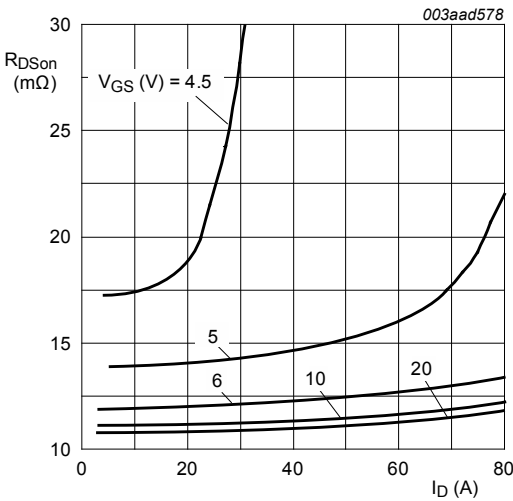


Fig. 13. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25\text{ }^{\circ}\text{C}$

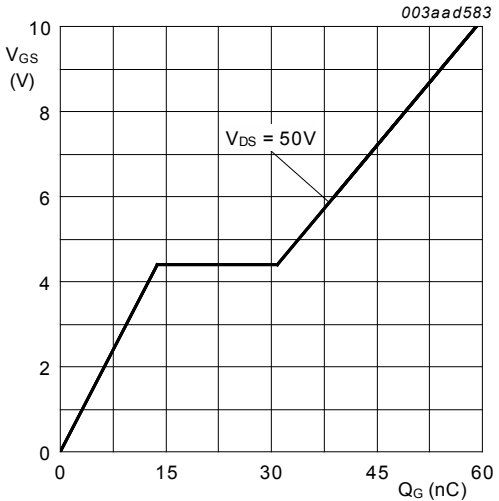


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$T_j = 25\text{ }^{\circ}\text{C}; I_D = 25\text{ A}$

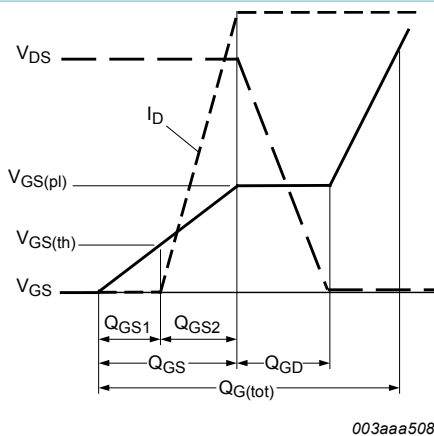


Fig. 15. Gate charge waveform definitions

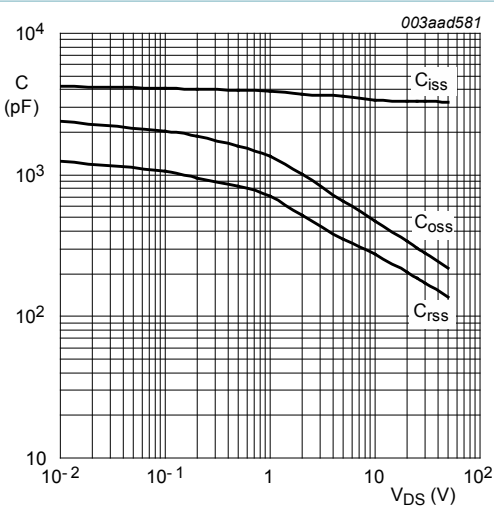


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0V; f = 1MHz$

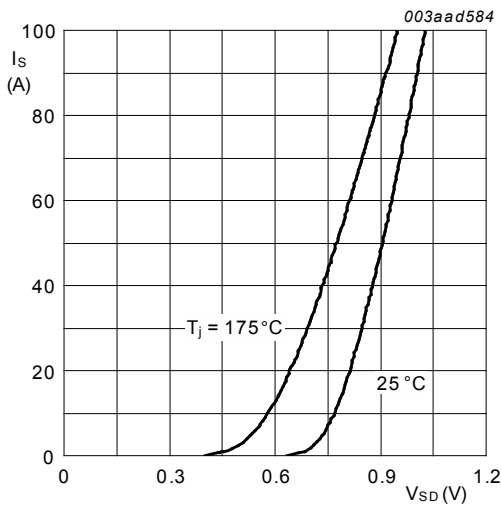


Fig. 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$V_{GS} = 0V$

11. Package outline

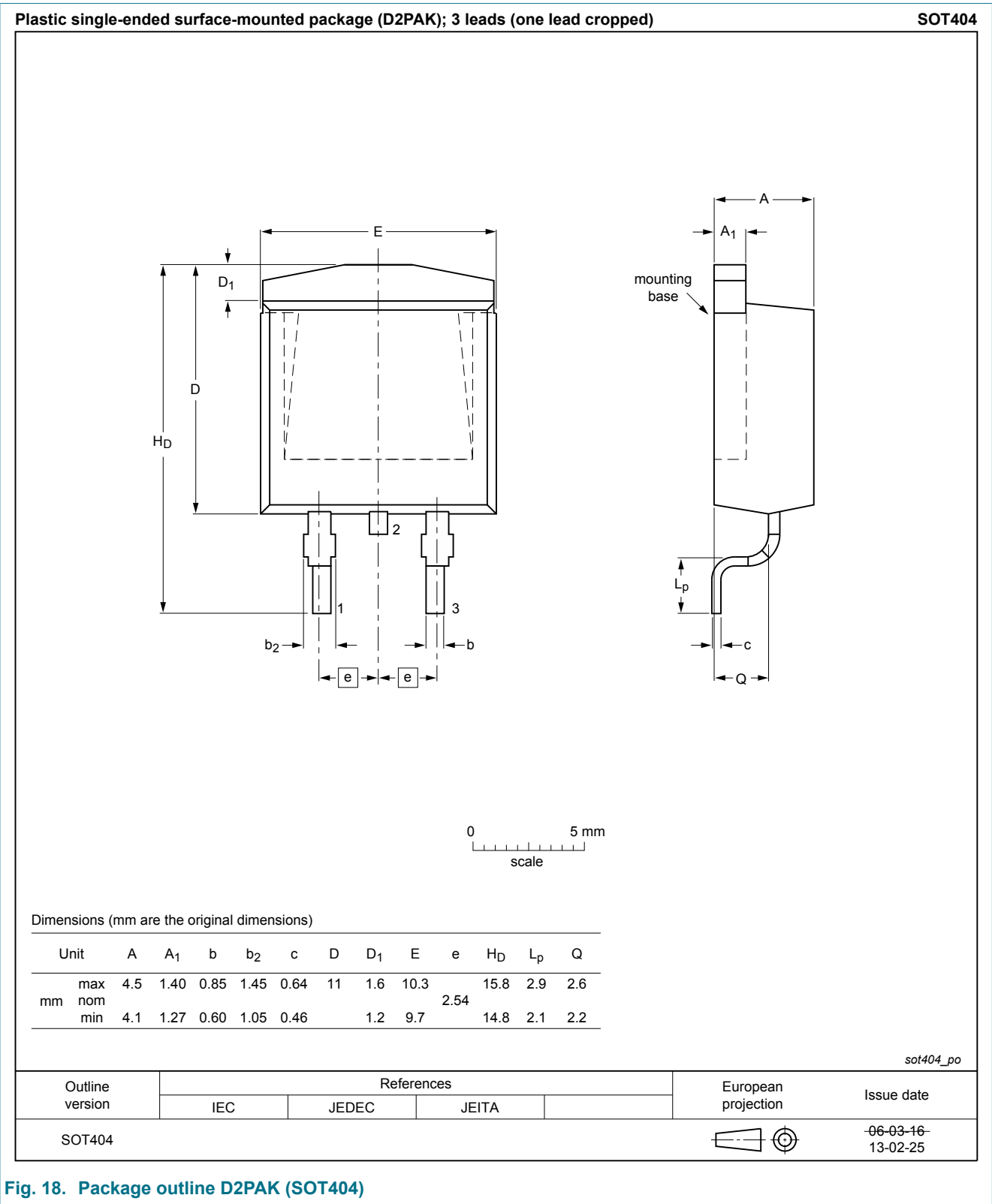


Fig. 18. Package outline D2PAK (SOT404)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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