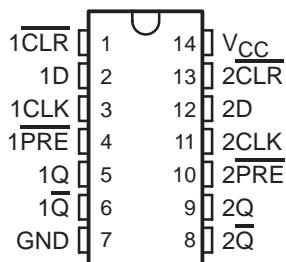


SN54ACT74, SN74ACT74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

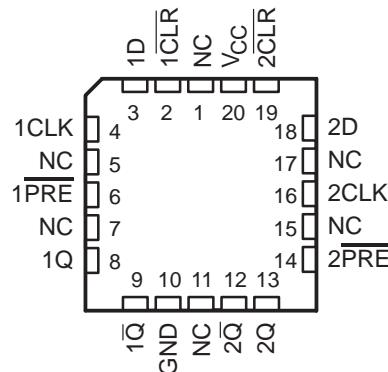
SCAS520H – AUGUST 1995 – REVISED OCTOBER 2003

- 4.5-V to 5.5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 10.5 ns at 5 V
- Inputs Are TTL-Voltage Compatible

SN54ACT74 . . . J OR W PACKAGE
SN74ACT74 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54ACT74 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'ACT74 dual positive-edge-triggered devices are D-type flip-flops.

A low level at the preset (PRE) or clear (CLR) input sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at D can be changed without affecting the levels at the outputs.

ORDERING INFORMATION

TA	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74ACT74N	SN74ACT74N
	SOIC – D	Tube	SN74ACT74D	ACT74
		Tape and reel	SN74ACT74DR	
	SOP – NS	Tape and reel	SN74ACT74NSR	ACT74
	SSOP – DB	Tape and reel	SN74ACT74DBR	AD74
	TSSOP – PW	Tube	SN74ACT74PW	AD74
		Tape and reel	SN74ACT74PWR	
-55°C to 125°C	CDIP – J	Tube	SNJ54ACT74J	SNJ54ACT74J
	CFP – W	Tube	SNJ54ACT74W	SNJ54ACT74W
	LCCC – FK	Tube	SNJ54ACT74FK	SNJ54ACT74FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**SN54ACT74, SN74ACT74
DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH CLEAR AND PRESET**

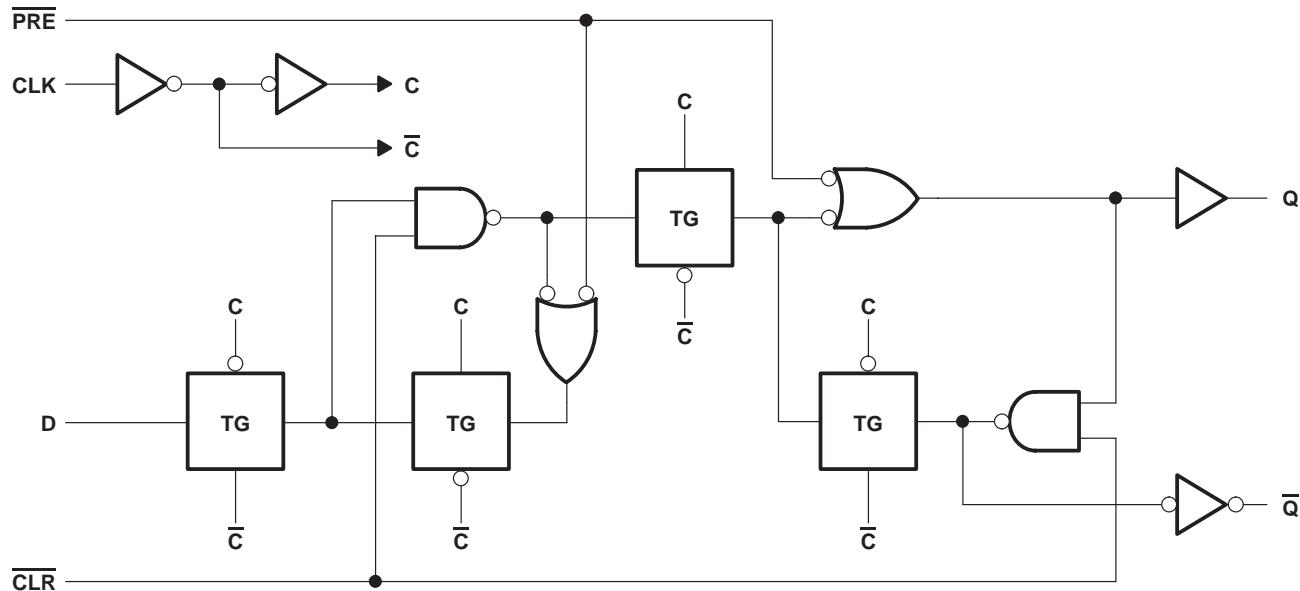
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FUNCTION TABLE
(each flip-flop)

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	\bar{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	\bar{Q}_0

† This configuration is nonstable; that is, it does not persist when either PRE or CLR returns to its inactive (high) level.

logic diagram, each flip-flop (positive logic)



SN54ACT74, SN74ACT74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN54ACT74		SN74ACT74		UNIT	
		MIN	MAX	MIN	MAX		
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V	
V _{IH}	High-level input voltage		2		2	V	
V _{IL}	Low-level input voltage			0.8		0.8	V
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V	
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V	
I _{OH}	High-level output current		-24		-24	mA	
I _{OL}	Low-level output current		24		24	mA	
Δt/Δv	Input transition rise or fall rate		8		8	ns/V	
T _A	Operating free-air temperature	-55	125	-40	85	°C	

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**SN54ACT74, SN74ACT74
DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH CLEAR AND PRESET**

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54ACT74	SN74ACT74	UNIT
			MIN	TYP	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	4.5 V	4.4	4.49		4.4	4.4	V
		5.5 V	5.4	5.49		5.4	5.4	
	I _{OH} = -24 mA	4.5 V	3.86			3.7	3.76	
		5.5 V	4.86			4.7	4.76	
	I _{OH} = -50 mA [†]	5.5 V				3.86		
V _{OL}	I _{OL} = 50 µA	4.5 V	0.001	0.1		0.1	0.1	V
		5.5 V	0.001	0.1		0.1	0.1	
	I _{OL} = 24 mA	4.5 V		0.36		0.5	0.44	
		5.5 V		0.36		0.5	0.44	
	I _{OL} = 50 mA [†]	5.5 V				1.65		
	I _{OL} = 75 mA [†]	5.5 V					1.65	
I _I	V _I = V _{CC} or GND	5.5 V		±0.1		±1	±1	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V		2		40	20	µA
ΔI _{CC} [‡]	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V		0.6		1.6	1.5	mA
C _i	V _I = V _{CC} or GND	5 V		3				pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

timing characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C		SN54ACT74	SN74ACT74	UNIT
			MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency			145	85	125	MHz
t _w	Pulse duration		PRE or CLR low	5	7	6	ns
			CLK	5	7	6	
t _{su}	Setup time, data before CLK↑		Data	3	4	3.5	ns
			PRE or CLR inactive	0	0.5	0	
t _h	Hold time, data after CLK↑			1	1	1	ns

switching characteristics over recommended operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ACT74			UNIT	
			T _A = 25°C				
			MIN	TYP	MAX		
f _{max}			145	210		85	MHz
t _{PLH}	PRE or CLR	Q or \bar{Q}	1	5.5	9.5	1	11.5
t _{PHL}			1	6	10	1	12.5
t _{PLH}	CLK	Q or \bar{Q}	1	7.5	11	1	14
t _{PHL}			1	6	10	1	12

SN54ACT74, SN74ACT74
DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH CLEAR AND PRESET

SCAS520H – AUGUST 1995 – REVISED OCTOBER 2003

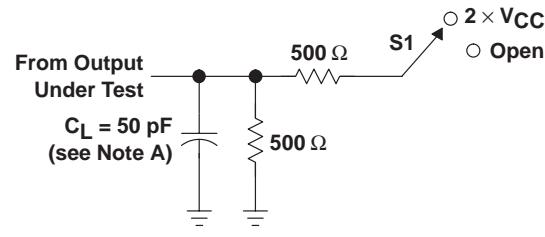
switching characteristics over recommended operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ACT74			UNIT
			TA = 25°C		MIN	MAX
			MIN	TYP		
f _{max}			145	210	125	MHz
t _{PLH}	PRE or CLR	Q or \bar{Q}	3	5.5	9.5	2.5
t _{PHL}			3	6	10	11.5
t _{PLH}	CLK	Q or \bar{Q}	4	7.5	11	4
t _{PHL}			3.5	6	10	11.5

operating characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$

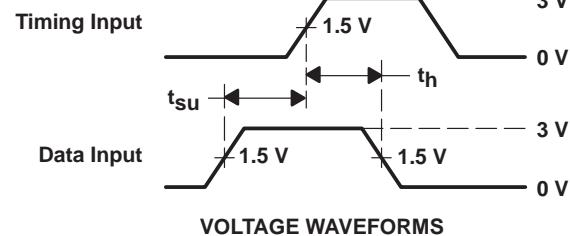
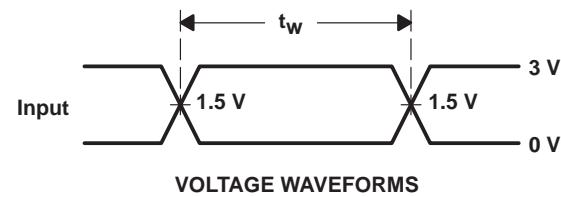
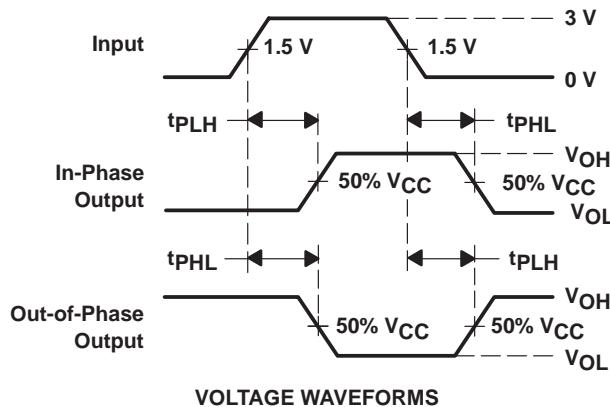
PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	$C_L = 50$ pF, $f = 1$ MHz	45	pF

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open

LOAD CIRCUIT



NOTES: A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O = 50$ Ω , $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8752501M2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 8752501M2A SNJ54ACT 74FK	Samples
5962-8752501MCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8752501MC A SNJ54ACT74J	Samples
5962-8752501MDA	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8752501MD A SNJ54ACT74W	Samples
SN74ACT74D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT74	Samples
SN74ACT74DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD74	Samples
SN74ACT74DE4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT74	Samples
SN74ACT74DG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT74	Samples
SN74ACT74DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT74	Samples
SN74ACT74DRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT74	Samples
SN74ACT74DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT74	Samples
SN74ACT74N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74ACT74N	Samples
SN74ACT74NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74ACT74N	Samples
SN74ACT74NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT74	Samples
SN74ACT74PW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD74	Samples
SN74ACT74PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD74	Samples
SN74ACT74PWRE4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD74	Samples
SNJ54ACT74FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 8752501M2A SNJ54ACT	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples									
										74FK										
SNJ54ACT74J	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8752501MC A SNJ54ACT74J	Samples									
SNJ54ACT74W	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8752501MD A SNJ54ACT74W	Samples									

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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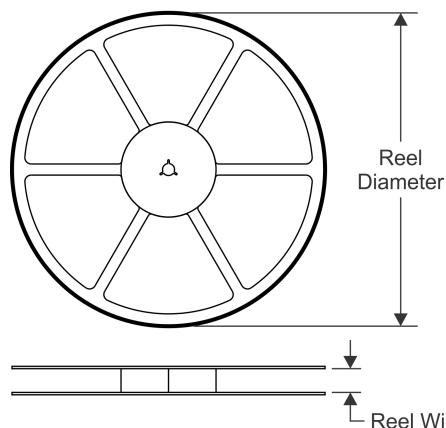
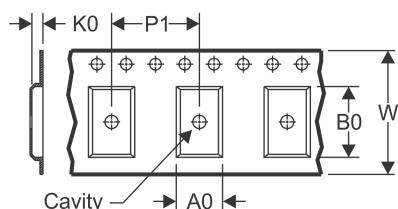
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54ACT74, SN74ACT74 :

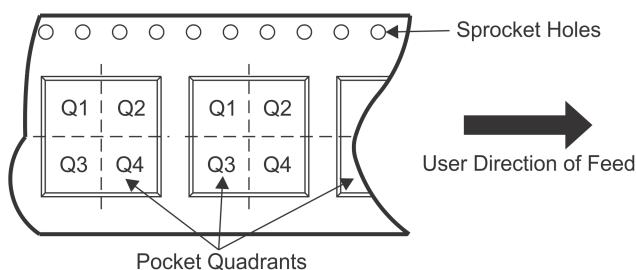
- Catalog : [SN74ACT74](#)
- Enhanced Product : [SN74ACT74-EP](#), [SN74ACT74-EP](#)
- Military : [SN54ACT74](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


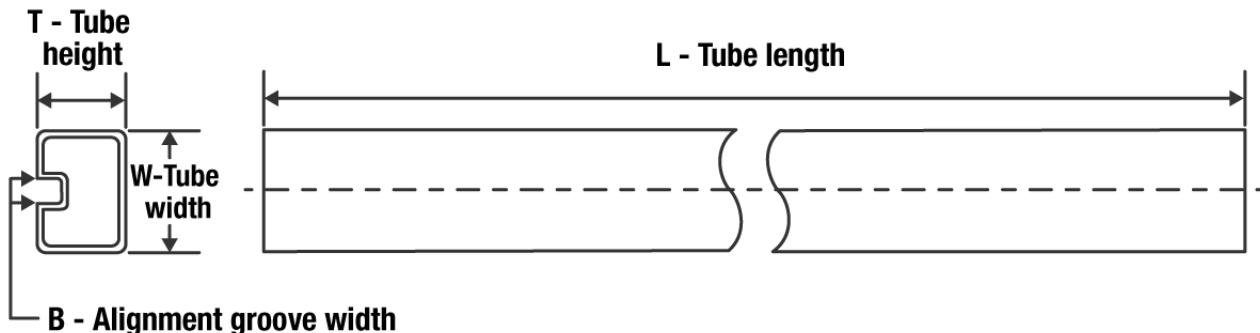
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT74DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74ACT74DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74ACT74NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74ACT74PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT74DBR	SSOP	DB	14	2000	853.0	449.0	35.0
SN74ACT74DR	SOIC	D	14	2500	853.0	449.0	35.0
SN74ACT74NSR	SO	NS	14	2000	853.0	449.0	35.0
SN74ACT74PWR	TSSOP	PW	14	2000	853.0	449.0	35.0

TUBE


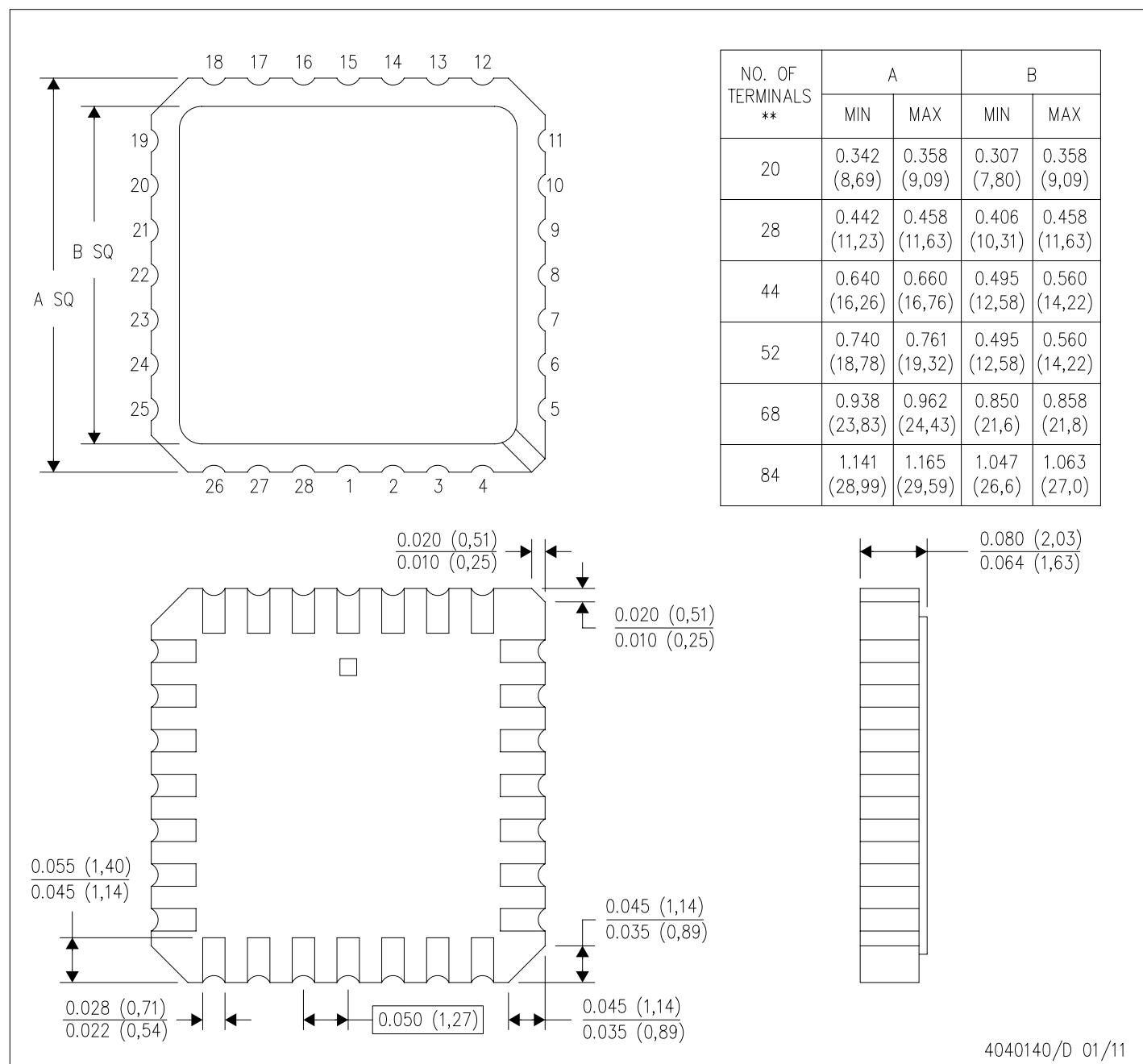
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-8752501M2A	FK	LCCC	20	1	506.98	12.06	2030	NA
SN74ACT74D	D	SOIC	14	50	506.6	8	3940	4.32
SN74ACT74DE4	D	SOIC	14	50	506.6	8	3940	4.32
SN74ACT74DG4	D	SOIC	14	50	506.6	8	3940	4.32
SN74ACT74N	N	PDIP	14	25	506	13.97	11230	4.32
SN74ACT74N	N	PDIP	14	25	506	13.97	11230	4.32
SN74ACT74NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74ACT74NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74ACT74PW	PW	TSSOP	14	90	530	10.2	3600	3.5
SNJ54ACT74FK	FK	LCCC	20	1	506.98	12.06	2030	NA

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

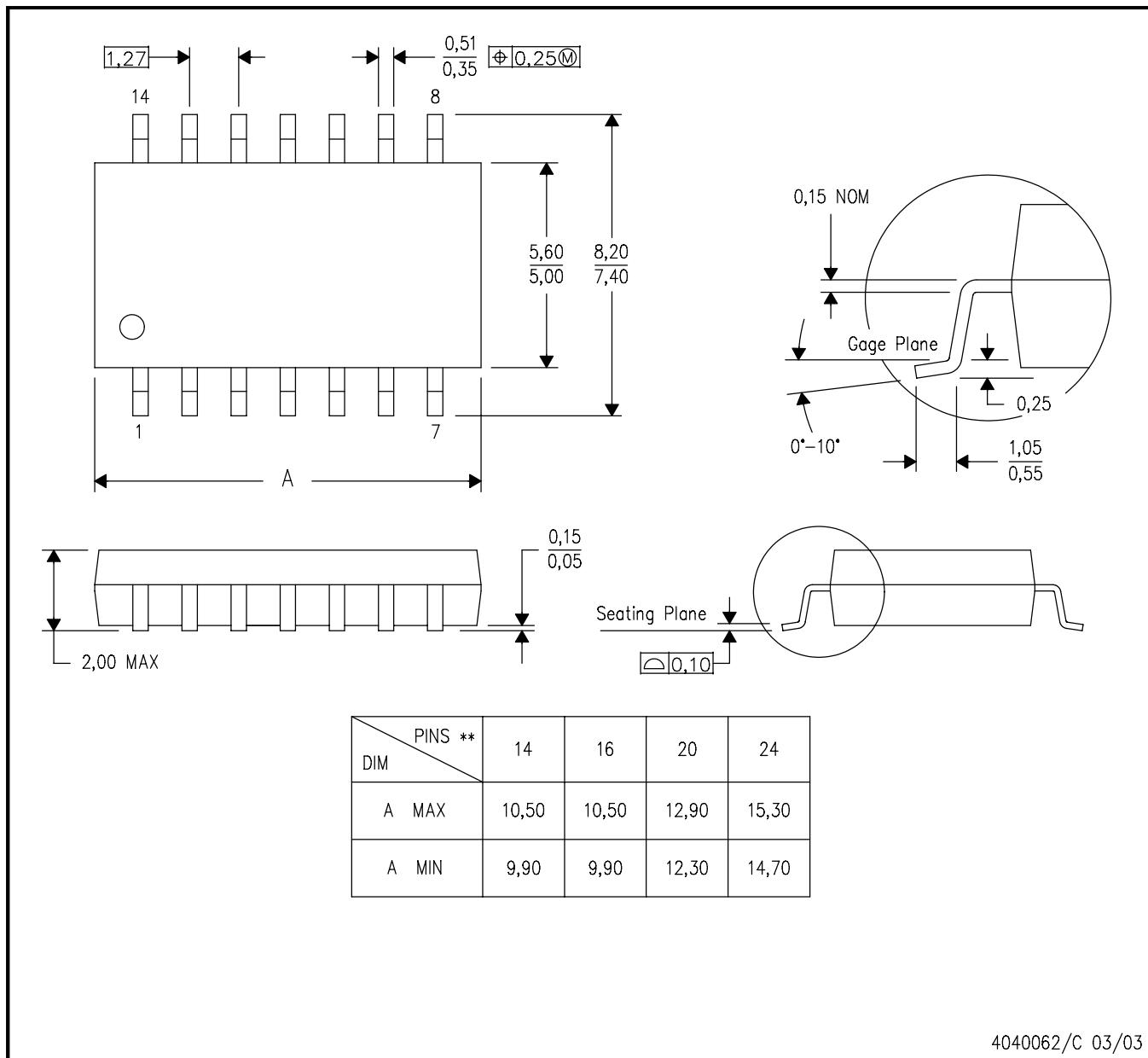
4040140/D 01/11

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

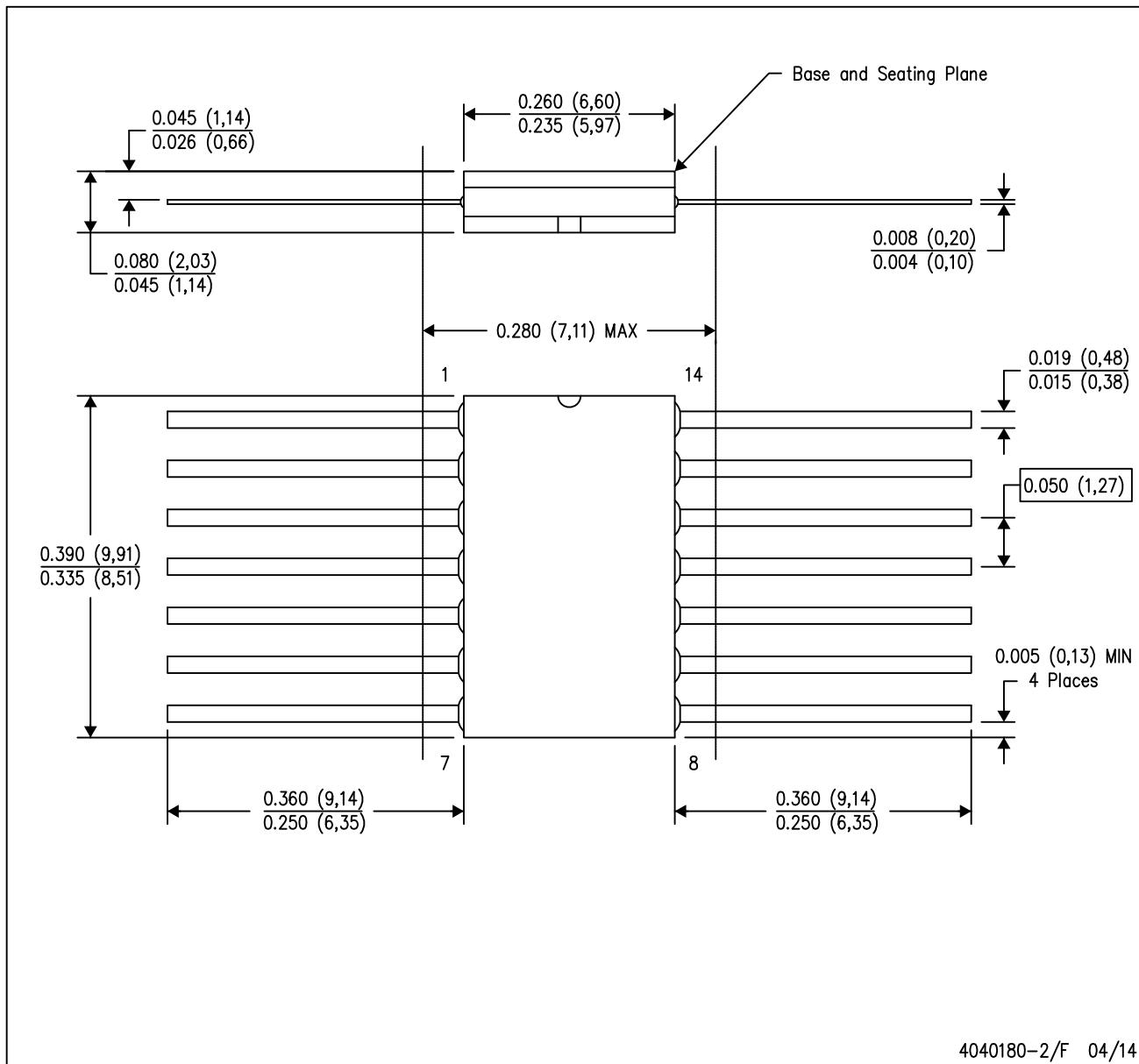


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



NOTES:

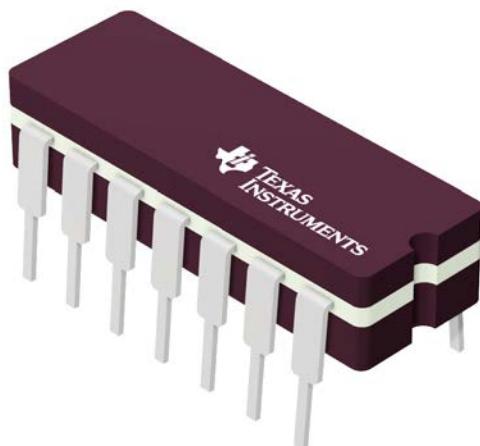
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL-STD 1835 GDFP1-F14

GENERIC PACKAGE VIEW

J 14

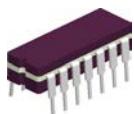
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

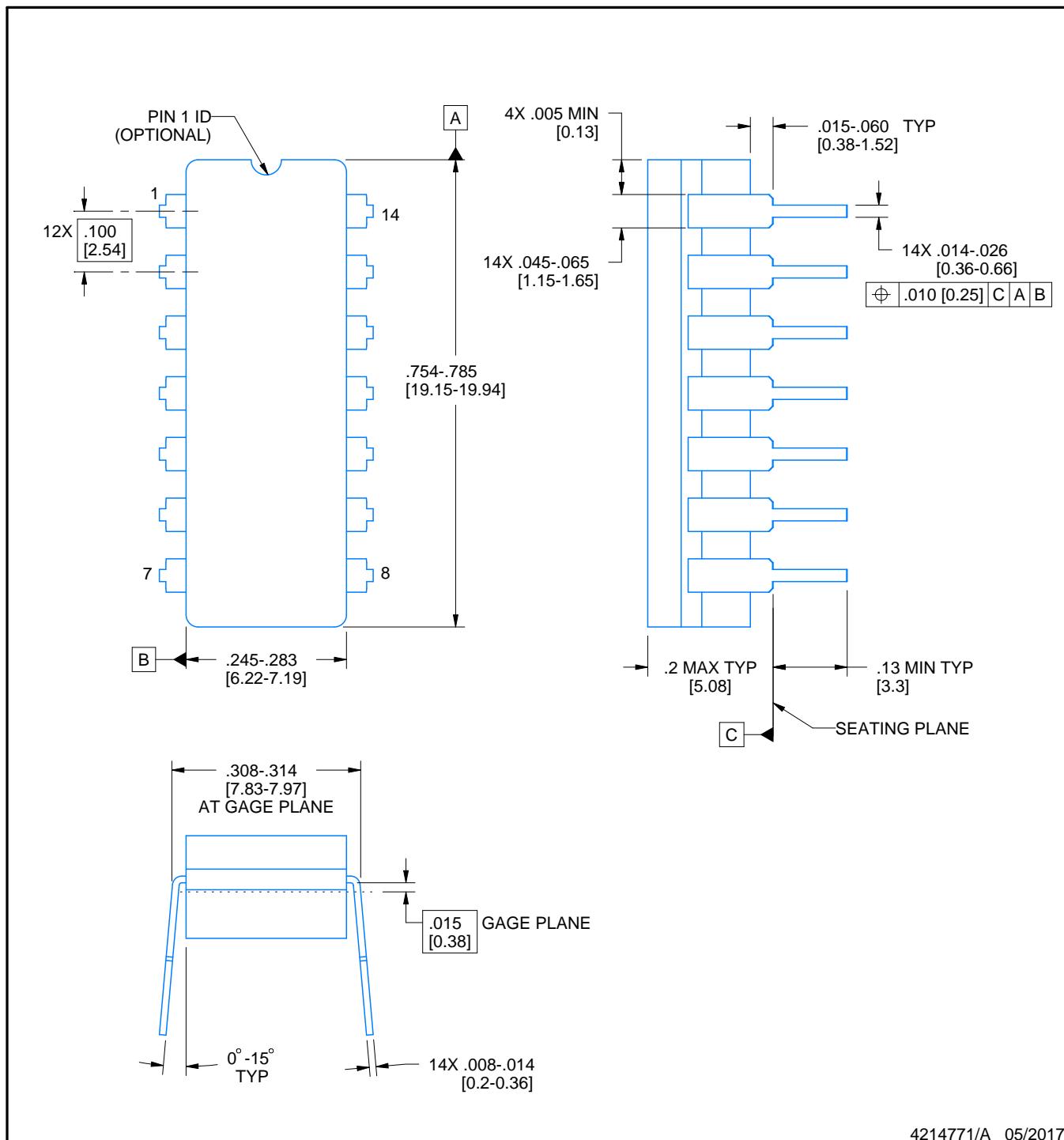


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

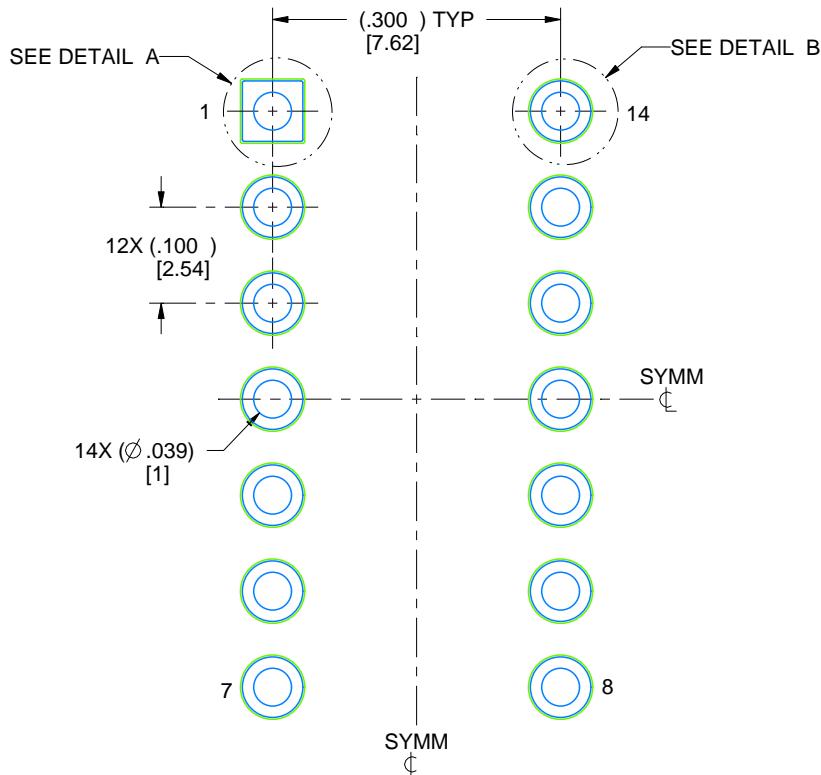
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

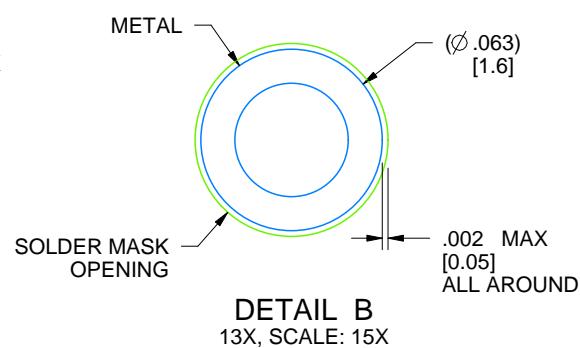
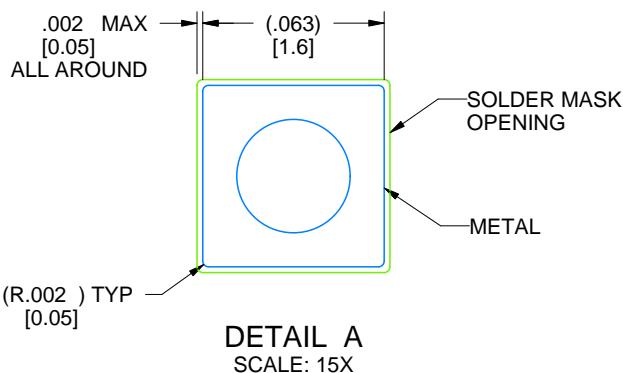
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



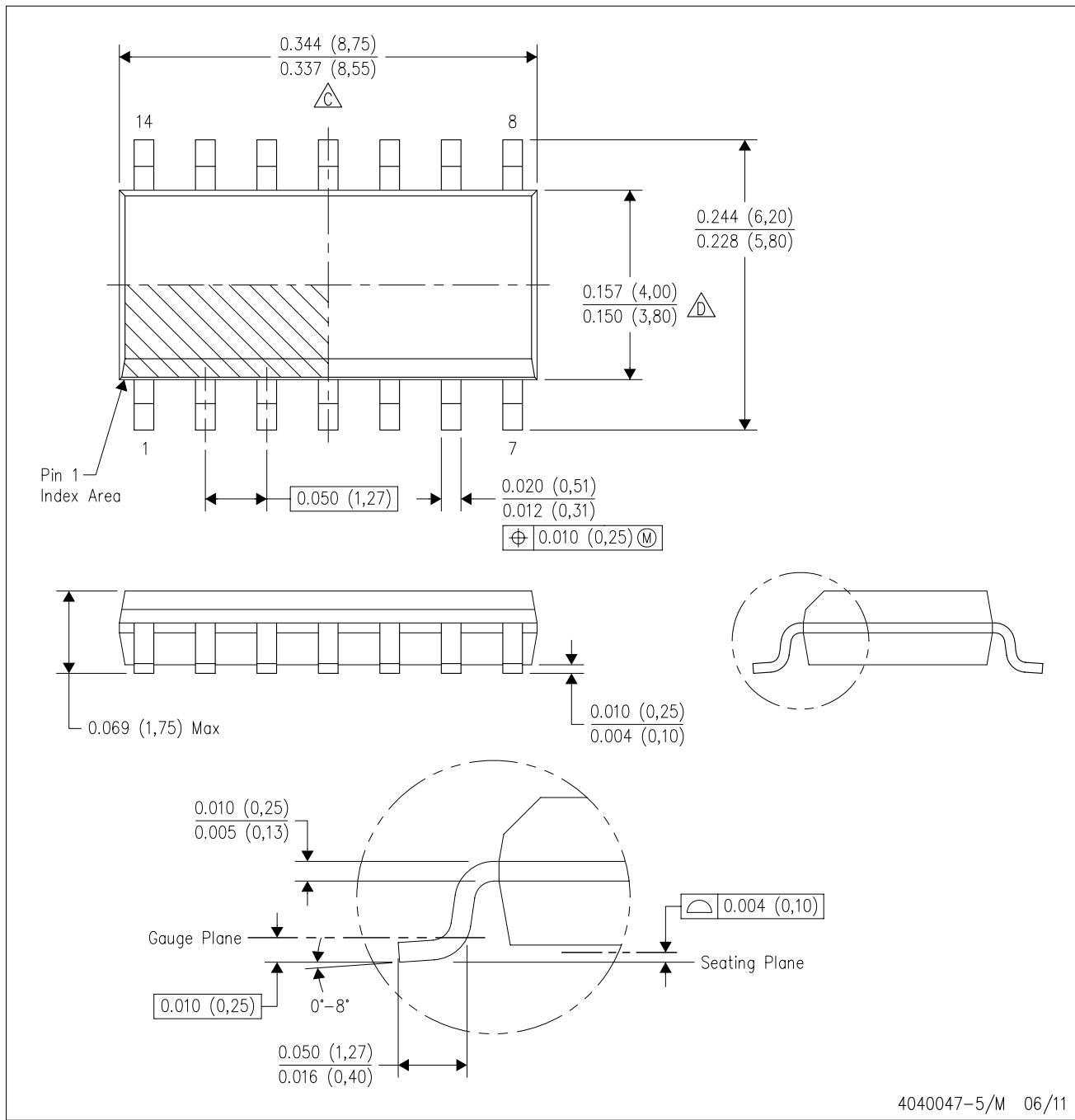
LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

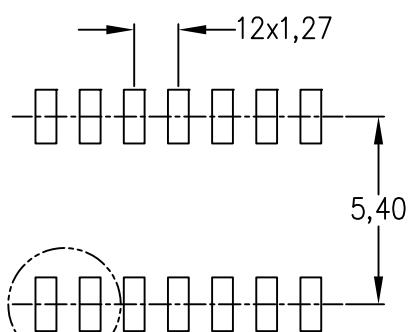
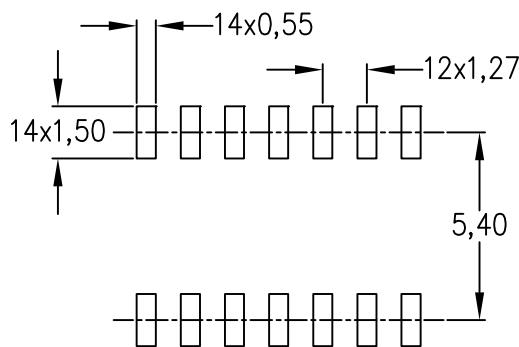
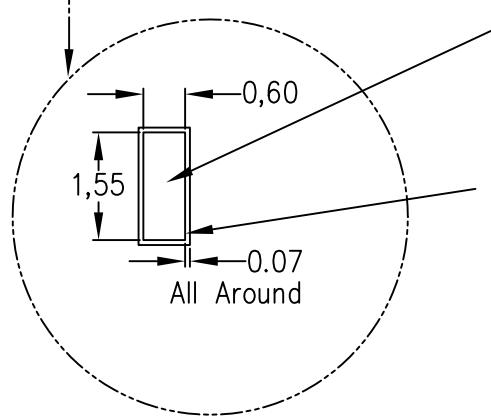
C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.

D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

E Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

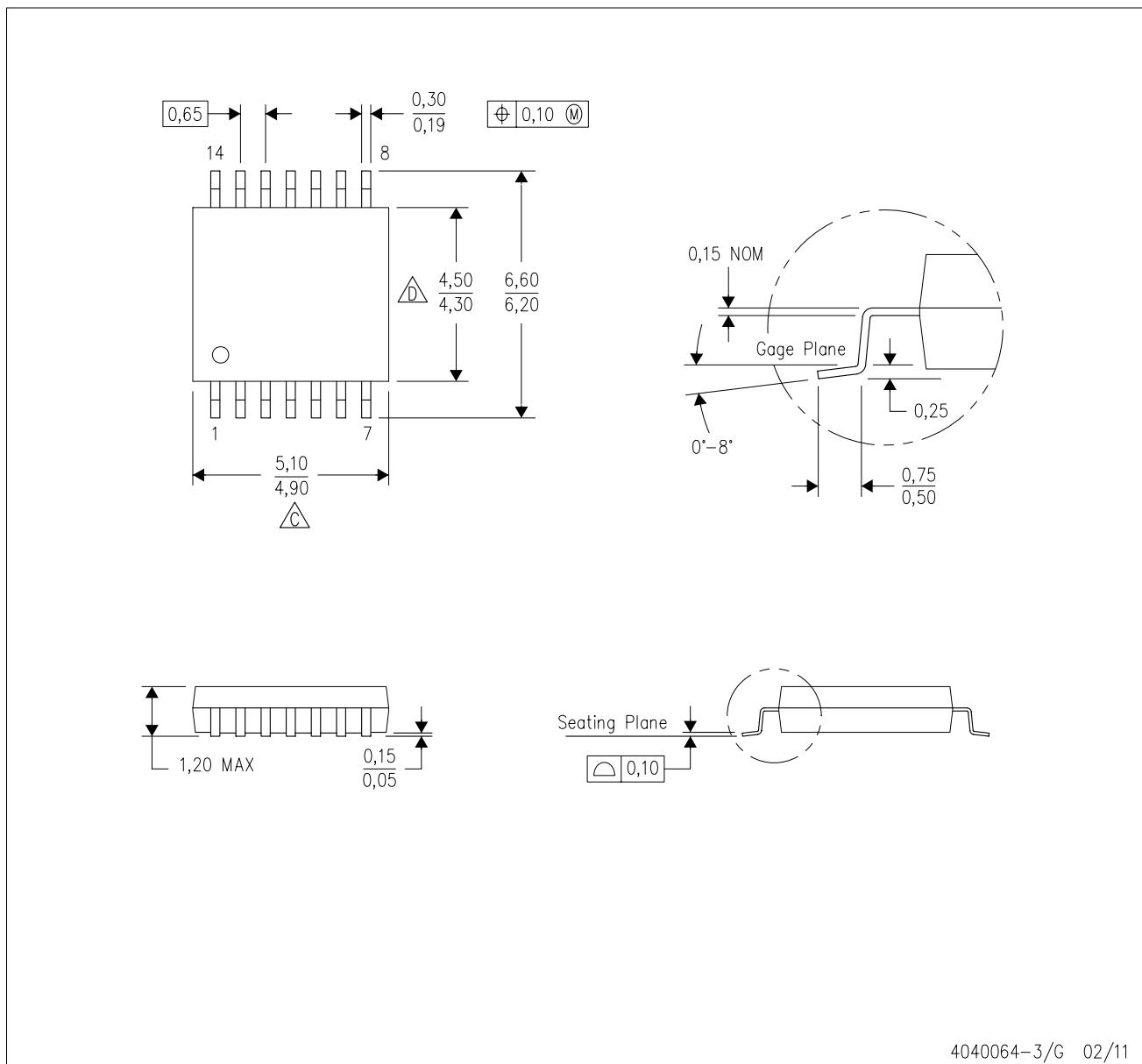
4211283-3/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

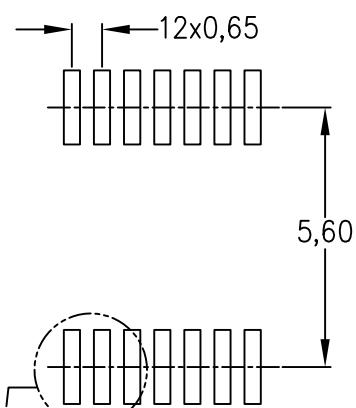
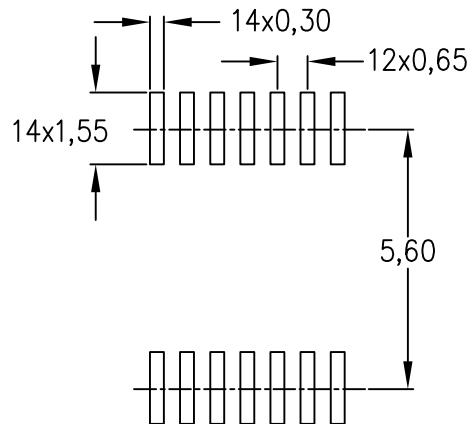
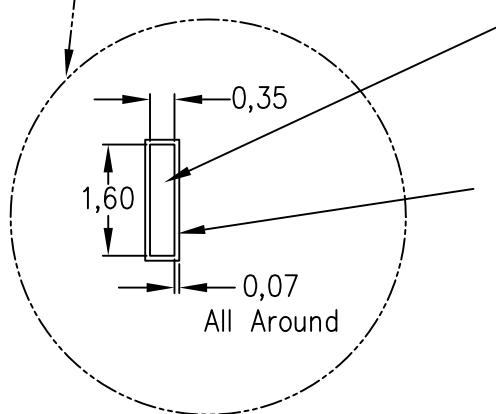
 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

 D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

4211284-2/G 08/15

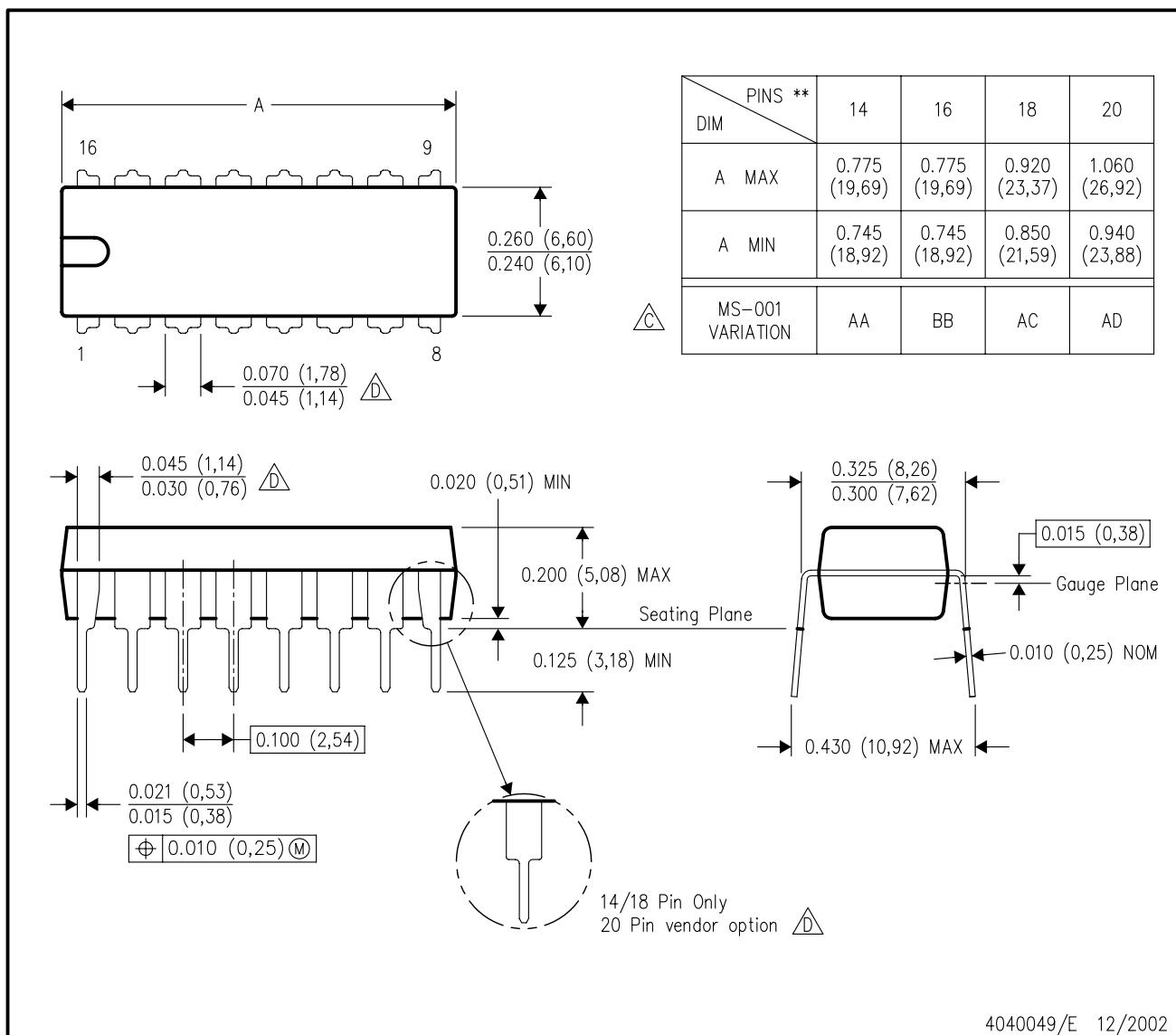
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

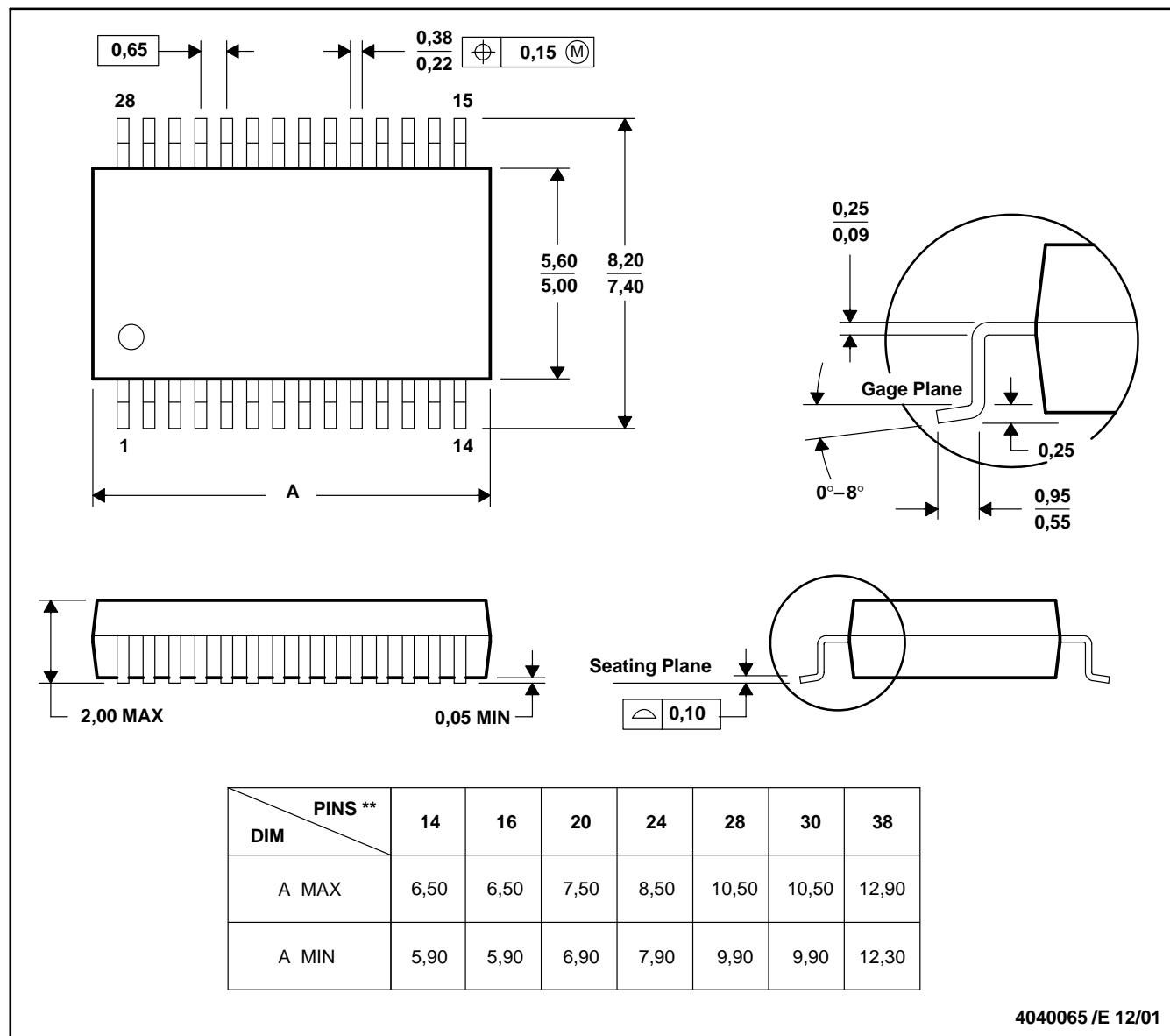
△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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