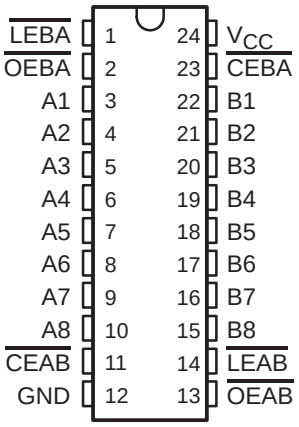
- **3-State True Outputs**
- **Back-to-Back Registers for Storage**
- **Package Options Include Plastic Small-Outline and Shrink Small-Outline Packages and Standard Plastic 300-mil DIPs**

DB, DW, OR NT PACKAGE
(TOP VIEW)



description

The SN74F543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable ($\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$) and output enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) inputs are provided for each register to permit independent control in either direction of data flow. The A outputs are characterized to sink 24 mA while the B outputs are characterized to sink 64 mA.

The A-to-B enable ($\overline{\text{CEAB}}$) input must be low in order to enter data from A or to output data from B. Having $\overline{\text{CEAB}}$ low and $\overline{\text{LEAB}}$ low makes the A-to-B latches transparent; a subsequent low-to-high transition of $\overline{\text{LEAB}}$ puts the A latches in the storage mode. With $\overline{\text{CEAB}}$ and $\overline{\text{OEAB}}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$ inputs.

The SN74F543 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

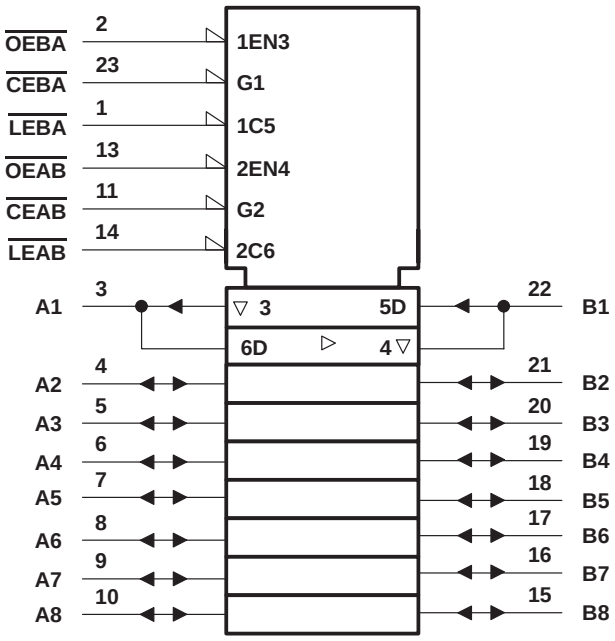
The SN74F543 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{\text{CEAB}}$	$\overline{\text{LEAB}}$	$\overline{\text{OEAB}}$	A	B
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0‡
L	L	L	L	L
L	L	L	H	H

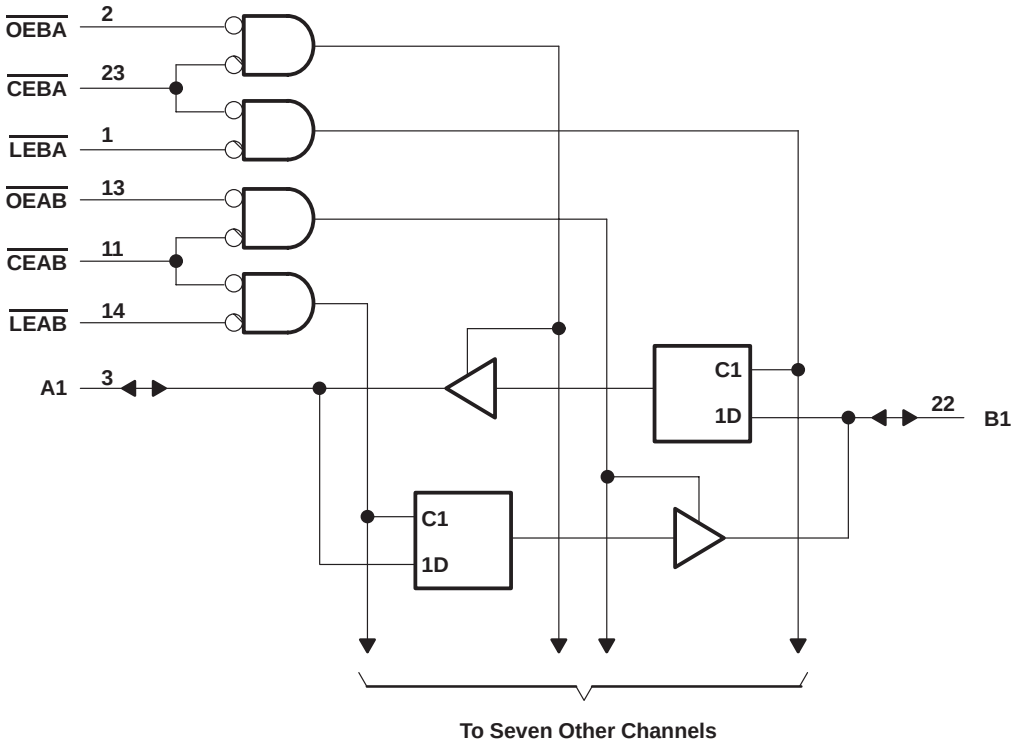
† A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$.
‡ Output level before the indicated steady-state input conditions were established.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (excluding I/O ports) (see Note 1) . . . . . –1.2 V to 7 V
Input current range, I_{IK} . . . . . –30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state . . . . . –0.5 V to 5.5 V
Voltage range applied to any output in the high state . . . . . –0.5 V to V_{CC}
Current into any output in the low state: A1–A8 . . . . . 48 mA
B1–B8 . . . . . 128 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded provided the input-current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A1–A8			–3	mA
		B1–B8			–15	
I_{OL}	Low-level output current	A1–A8			24	mA
		B1–B8			64	
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = – 18 mA			–1.2	V
V_{OH}	A1–A8	V_{CC} = 4.5 V	I_{OH} = – 1 mA	2.5	3.4		V
			I_{OH} = – 3 mA	2.4	3.3		
	B1–B8		I_{OH} = – 3 mA	2.4	3.3		
			I_{OH} = – 15 mA	2	3.1		
	Any output	V_{CC} = 4.75 V,	I_{OH} = – 1 mA to –3 mA	2.7			
V_{OL}	A1–A8	V_{CC} = 4.5 V	I_{OL} = 24 mA		0.3	0.5	V
	B1–B8		I_{OL} = 64 mA		0.42	0.55	
I_I	$\overline{OE}$, $\overline{LE}$, and $\overline{CE}$	V_{CC} = 5.5 V	V_I = 7 V			0.1	mA
	A and B ports		V_I = 5.5 V			1	
I_{IH}‡	$\overline{OE}$, $\overline{LE}$, and $\overline{CE}$	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
	A and B ports					70	
I_{IL}‡	$\overline{OE}$, $\overline{LE}$, and $\overline{CE}$	V_{CC} = 5.5 V,	V_I = 0.5 V			–1.2	mA
	A and B ports					–0.65	
I_{OS}§	A1–A8	V_{CC} = 5.5 V,	V_O = 0	–60		–150	mA
	B1–B8			–100		–225	
I_{CCH}		V_{CC} = 5.5 V			67	100	mA
I_{CCL}		V_{CC} = 5.5 V			83	125	mA
I_{CCZ}		V_{CC} = 5.5 V			83	125	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

timing requirements

			V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX¶		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration		5		5		ns
t_{su}	Setup time, data before latch enable	High or low	3		3.5		ns
t_h	Hold time, data after latch enable	High or low	3		3.5		ns

¶ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2.2	5.1	7.5	2.2	8.5	ns
t_{PHL}			2.2	4.6	6.5	2.2	7.5	
t_{PLH}	$\overline{LEBA}$	A	3.7	8.1	11	4.1	12.5	ns
t_{PHL}			3.7	8.1	11	4.1	12.5	
t_{PLH}	$\overline{LEAB}$	B	3.7	8.1	11	4.1	12.5	ns
t_{PHL}			3.7	8.1	11	4.1	12.5	
t_{PZH}	$\overline{OE}$ or $\overline{CE}$	A or B	2.2	6.6	9	2.2	10	ns
t_{PZL}			3.2	7.1	10.5	3.2	12	
t_{PHZ}	$\overline{OE}$ or $\overline{CE}$	A or B	1.7	5.6	8	1.7	9	ns
t_{PLZ}			1.7	5.1	7.5	1.7	8.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74F543DBR	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	F543	Samples
SN74F543DW	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	F543	Samples
SN74F543DWG4	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	F543	Samples
SN74F543DWR	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	F543	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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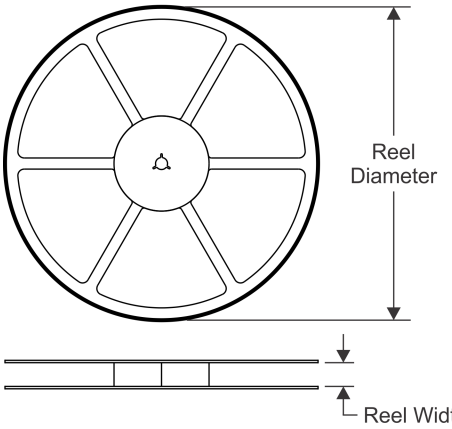
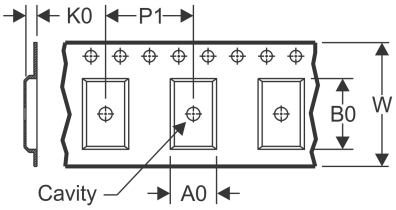
TAPE AND REEL INFORMATION

REEL DIMENSIONS

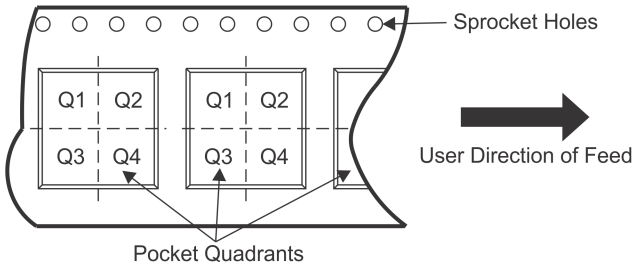


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

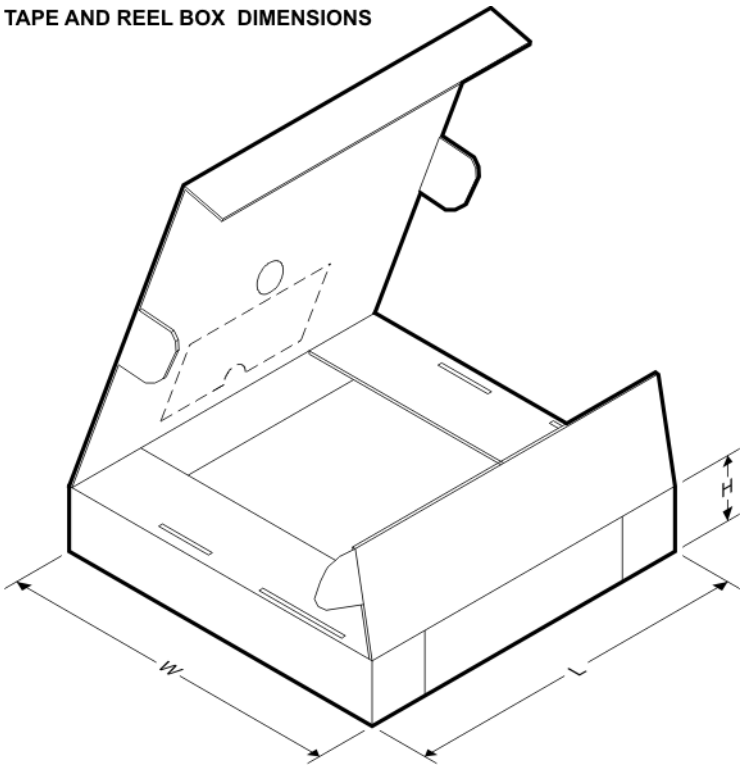
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F543DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74F543DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

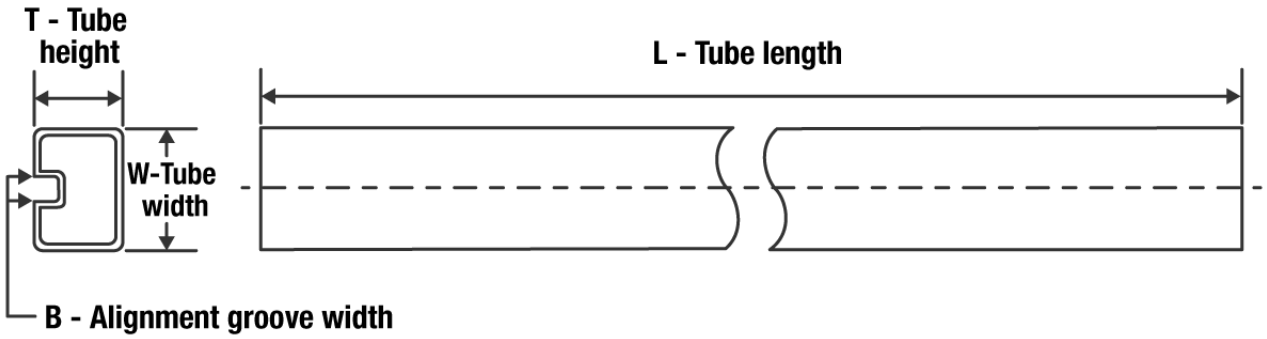
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F543DBR	SSOP	DB	24	2000	853.0	449.0	35.0
SN74F543DWR	SOIC	DW	24	2000	350.0	350.0	43.0

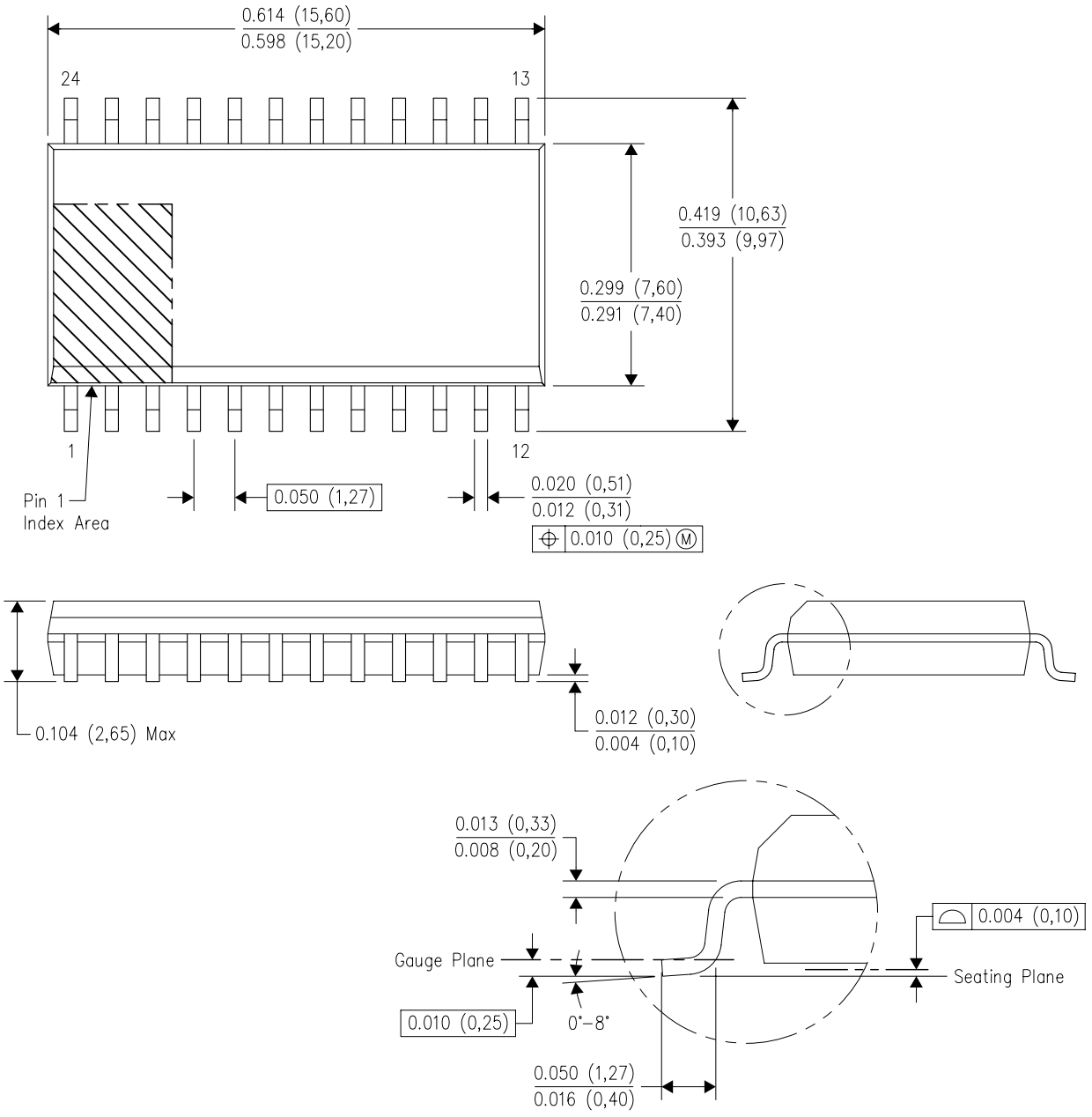
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74F543DW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74F543DWG4	DW	SOIC	24	25	506.98	12.7	4826	6.6

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE

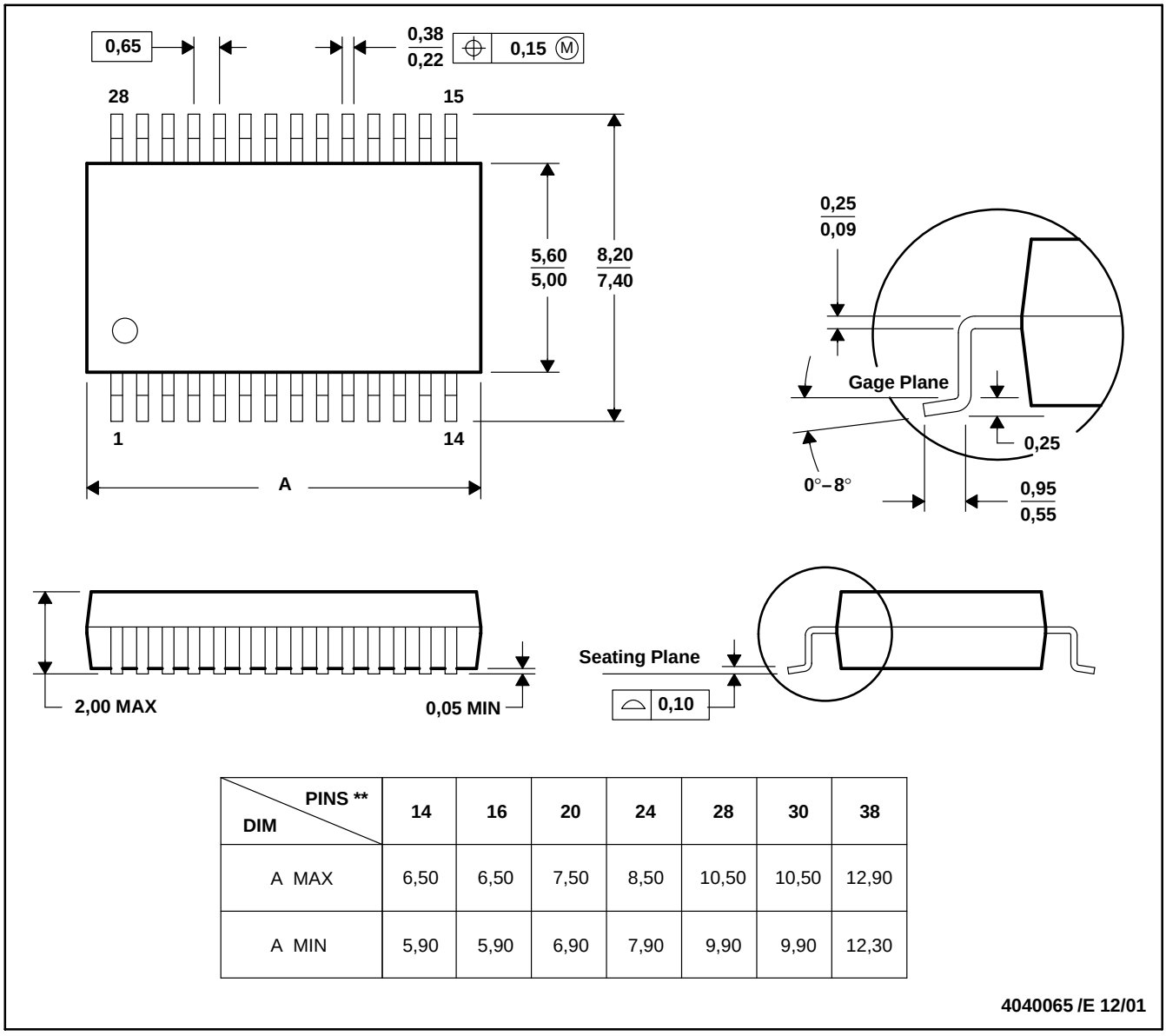


NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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