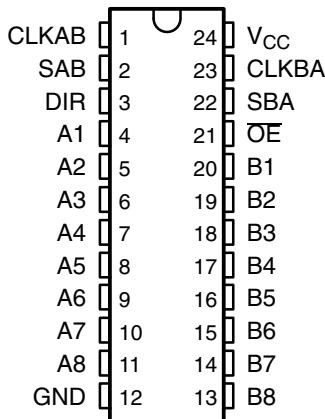


# SN54BCT646, SN74BCT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

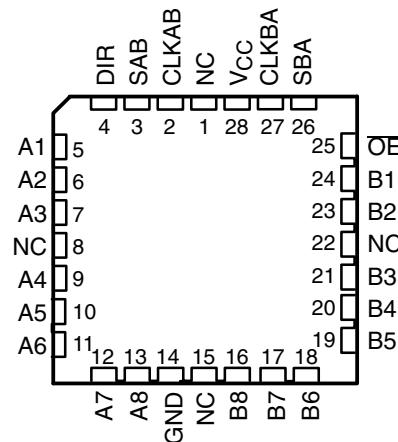
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- State-of-the-Art BiCMOS Design  
Significantly Reduces  $I_{CCZ}$
- Bus Transceivers/Registers
- Independent Registers and Enables for  
A and B Buses

SN54BCT646 . . . JT OR W PACKAGE  
SN74BCT646 . . . DW OR NT PACKAGE  
(TOP VIEW)



SN54BCT646 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'BCT646 devices.

Output-enable ( $\overline{OE}$ ) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port can be stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus will receive data when  $\overline{OE}$  is low. In the isolation mode ( $\overline{OE}$  high), A data can be stored in one register and/or B data can be stored in the other register.

## ORDERING INFORMATION

| $T_A$                          | PACKAGE <sup>†</sup> |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|--------------------------------|----------------------|---------------|-----------------------|------------------|
| $0^\circ C$ to $70^\circ C$    | PDIP – NT            | Tube          | SN74BCT646NT          | SN74BCT646NT     |
|                                | SOIC – DW            | Tube          | SN74BCT646DW          | BCT646           |
|                                |                      | Tape and reel | SN74BCT646DWR         |                  |
| $-55^\circ C$ to $125^\circ C$ | CDIP – JT            | Tube          | SNJ54BCT646JT         | SNJ54BCT646JT    |
|                                | CFP – W              | Tube          | SNJ54BCT646W          | SNJ54BCT646W     |
|                                | LCCC – FK            | Tube          | SNJ54BCT646FK         | SNJ54BCT646FK    |

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**SN54BCT646, SN74BCT646  
OCTAL BUS TRANSCEIVERS AND REGISTERS  
WITH 3-STATE OUTPUTS**

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**description/ordering information(continued)**

When an output function is disabled, the input function still is enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

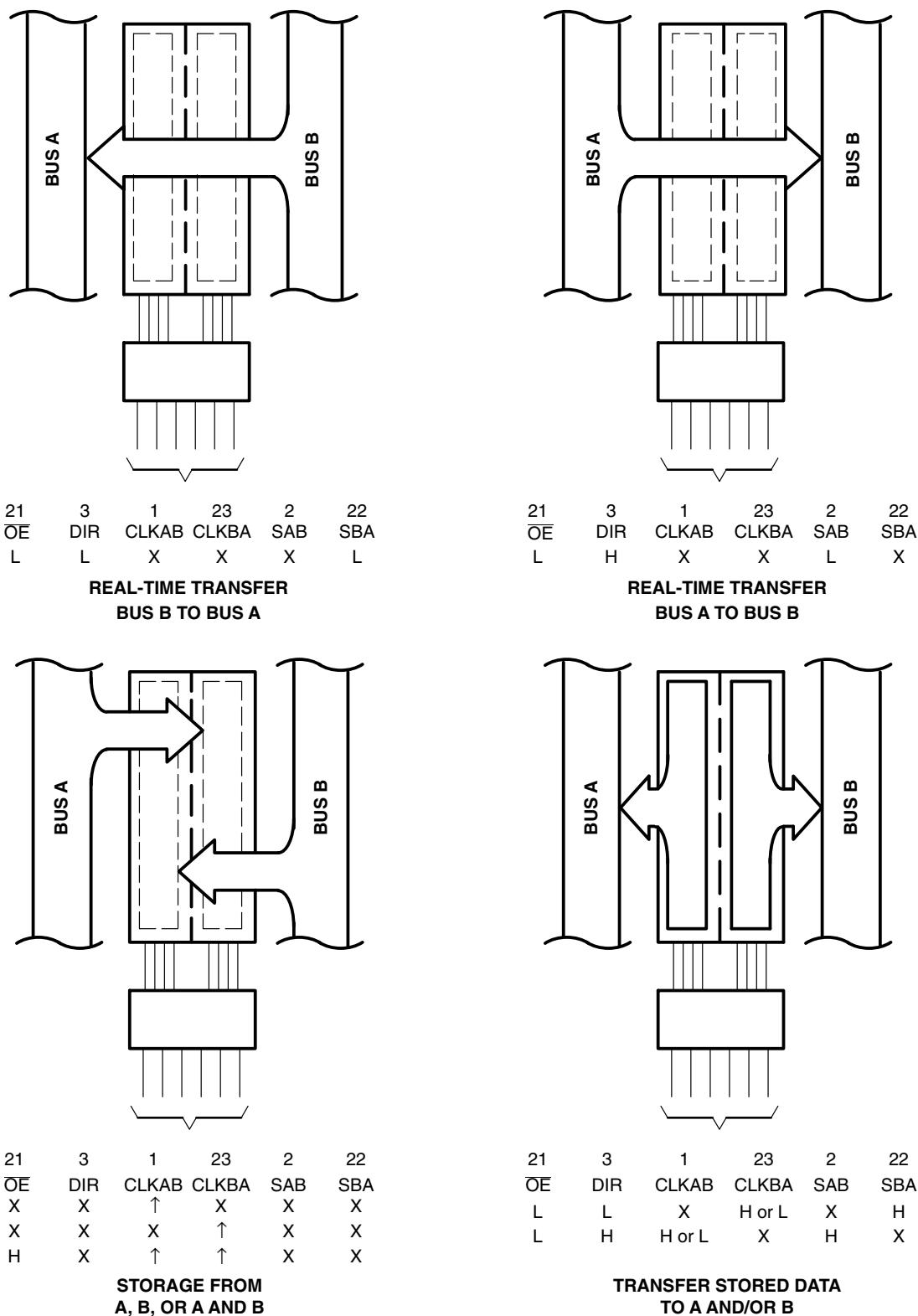
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



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Pin numbers shown are for the DW, JT, NT, and W packages.

**Figure 1. Bus-Management Functions**

# SN54BCT646, SN74BCT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

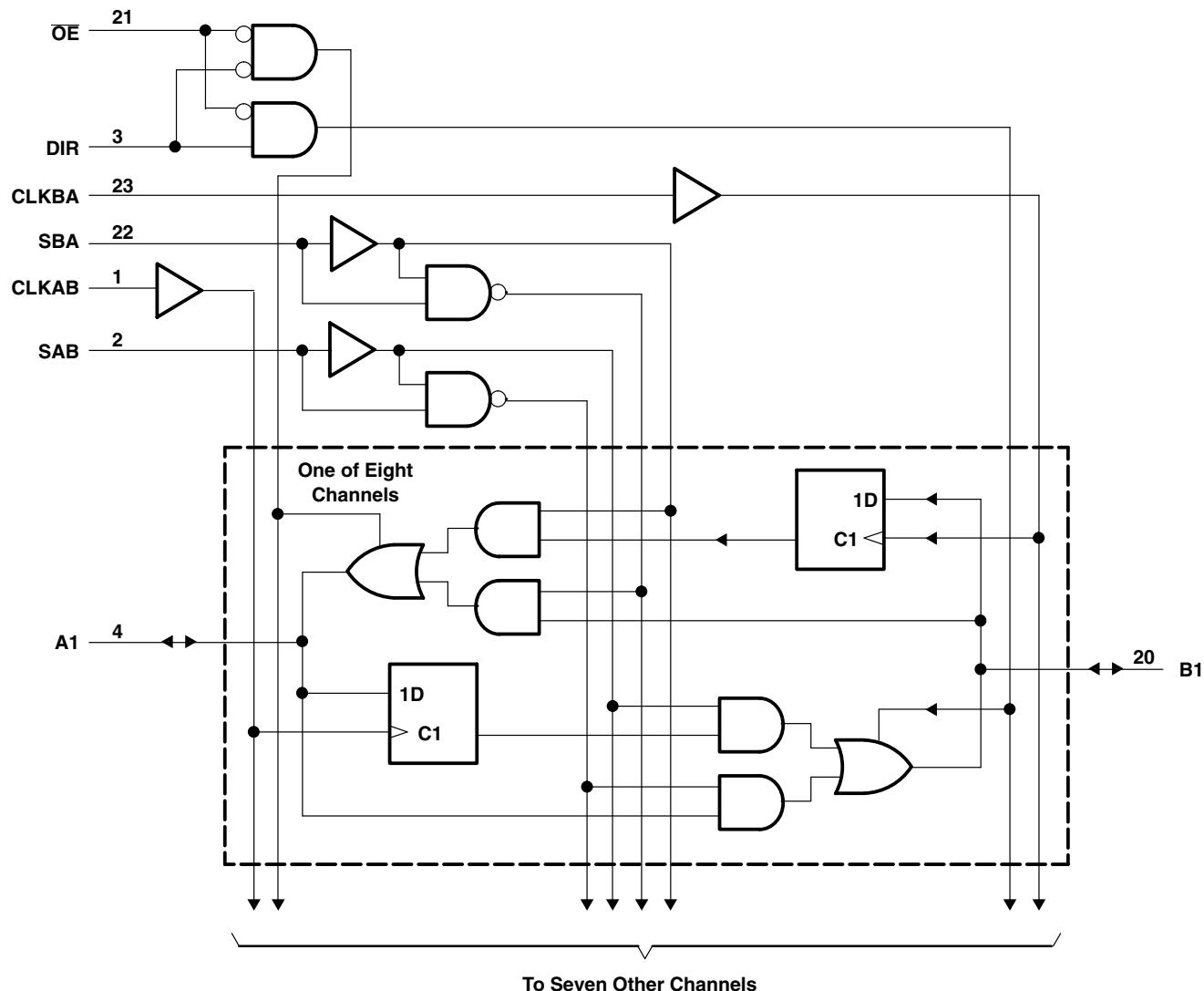
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FUNCTION TABLE

| INPUTS |     |        |        |     |     | DATA I/O       |                | OPERATION OR FUNCTION     |
|--------|-----|--------|--------|-----|-----|----------------|----------------|---------------------------|
| OE     | DIR | CLKAB  | CLKBA  | SAB | SBA | A1 THRU A8     | B1 THRU B8     |                           |
| X      | X   | ↑      | X      | X   | X   | Input          | Unspecified†   | Store A, B unspecified†   |
| X      | X   | X      | ↑      | X   | X   | Unspecified†   | Input          | Store B, A unspecified†   |
| H      | X   | ↑      | ↑      | X   | X   | Input          | Input          | Store A and B data        |
| H      | X   | H or L | H or L | X   | X   | Input disabled | Input disabled | Isolation, hold storage   |
| L      | L   | X      | X      | X   | L   | Output         | Input          | Real-time B data to A bus |
| L      | L   | X      | H or L | X   | H   | Output         | Input          | Stored B data to A bus    |
| L      | H   | X      | X      | L   | X   | Input          | Output         | Real-time A data to B bus |
| L      | H   | H or L | X      | H   | X   | Input          | Output         | Stored A data to B bus    |

† The data output functions can be enabled or disabled by various signals at the OE and DIR inputs. Data input functions always are enabled, i.e., data at the bus pins is stored on every low-to-high transition of the clock inputs.

## logic diagram (positive logic)



Pin numbers shown are for the DW, JT, NT, and W packages.

# SN54BCT646, SN74BCT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.  
3. The package thermal impedance is calculated in accordance with JESD 51-3.

#### **recommended operating conditions (see Note 4)**

|                 |                                | SN54BCT646 |     |     | SN74BCT646 |     |     | UNIT |
|-----------------|--------------------------------|------------|-----|-----|------------|-----|-----|------|
|                 |                                | MIN        | NOM | MAX | MIN        | NOM | MAX |      |
| V <sub>CC</sub> | Supply voltage                 | 4.5        | 5   | 5.5 | 4.5        | 5   | 5.5 | V    |
| V <sub>IH</sub> | High-level input voltage       |            | 2   |     | 2          |     |     | V    |
| V <sub>IL</sub> | Low-level input voltage        |            |     | 0.8 |            |     | 0.8 | V    |
| I <sub>IK</sub> | Input clamp current            |            |     | -18 |            |     | -18 | mA   |
| I <sub>OH</sub> | High-level output current      |            |     | -12 |            |     | -15 | mA   |
| I <sub>OL</sub> | Low-level output current       |            |     | 48  |            |     | 64  | mA   |
| T <sub>A</sub>  | Operating free-air temperature | -55        |     | 125 | 0          |     | 70  | °C   |

NOTE 4: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**SN54BCT646, SN74BCT646  
OCTAL BUS TRANSCEIVERS AND REGISTERS  
WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER         | TEST CONDITIONS                                  | SN54BCT646   |      |      | SN74BCT646 |      |           | UNIT |
|-------------------|--|--|------|------|------------|------|-----------|------|
|                   |  | MIN  | TYP† | MAX  | MIN        | TYP† | MAX       |      |
| V <sub>IK</sub>   | V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA |  |      | -1.2 |            |      | -1.2      | V    |
| V <sub>OH</sub>   | V <sub>CC</sub> = 4.5 V                          | I <sub>OH</sub> = -3 mA                                | 2.4  | 3.3  | 2.4        | 3.3  |           | V    |
|                   |  | I <sub>OH</sub> = -12 mA                               | 2    | 3.2  |            |      |           |      |
|                   |  | I <sub>OH</sub> = -15 mA                               |      |      | 2          | 3.1  |           |      |
| V <sub>OL</sub>   | V <sub>CC</sub> = 4.5 V                          | I <sub>OL</sub> = 48 mA                                | 0.38 | 0.55 |            |      |           | V    |
|                   |  | I <sub>OL</sub> = 64 mA                                |      |      |            |      | 0.42 0.55 |      |
| I <sub>I</sub>    | A or B port<br>Control inputs                    | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 5.5 V        |      | 1    |            |      | 1         | mA   |
|                   |  |  |      | 1    |            |      | 1         |      |
| I <sub>IH</sub> ‡ | A or B port<br>Control inputs                    | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V        |      | 70   |            |      | 70        | µA   |
|                   |  |  |      | 20   |            |      | 20        |      |
| I <sub>IL</sub> ‡ | A or B port<br>Control inputs                    | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.5 V        |      | -0.7 |            |      | -0.7      | mA   |
|                   |  |  |      | -0.7 |            |      | -0.7      |      |
| I <sub>OS</sub> § | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0      |  | -100 | -225 | -100       | -225 | -100 -225 | mA   |
| I <sub>CCL</sub>  | A or B port                                      | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = GND          | 42   | 67   | 42         | 67   | 42 67     | mA   |
| I <sub>CCH</sub>  | A or B port                                      | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 4.5 V        | 5.6  | 9    | 5.6        | 9    | 5.6 9     | mA   |
| I <sub>CCZ</sub>  | A or B port                                      | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = GND          | 10   | 16   | 10         | 16   | 10 16     | mA   |
| C <sub>i</sub>    | Control inputs                                   | V <sub>CC</sub> = 5 V, V <sub>I</sub> = 2.5 V or 0.5 V | 6    |      | 6          |      | 6         | pF   |
| C <sub>io</sub>   | A or B port                                      | V <sub>CC</sub> = 5 V, V <sub>O</sub> = 2.5 V or 0.5 V | 12   |      | 12         |      | 14        | pF   |

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ For I/O ports, the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

|                    |  | V <sub>CC</sub> = 5 V,<br>T <sub>A</sub> = 25°C | SN54BCT646 |     | SN74BCT646 |     | UNIT   |
|--------------------|--|---|------------|-----|------------|-----|--------|
|                    |  |   | MIN        | MAX | MIN        | MAX |        |
| f <sub>clock</sub> | Clock frequency                            |   | 83         |     | 83         |     | 83 MHz |
| t <sub>w</sub>     | Pulse duration, CLK high or low            |   | 6          |     | 6          |     | 6 ns   |
| t <sub>su</sub>    | Setup time, A or B before CLKAB↑ or CLKBA↑ |   | 6          |     | 7          |     | 6 ns   |
| t <sub>h</sub>     | Hold time, A or B after CLKAB↑ or CLKBA↑   |   | 0.5        |     | 0.5        |     | 0.5 ns |

**SN54BCT646, SN74BCT646**  
**OCTAL BUS TRANSCEIVERS AND REGISTERS**  
**WITH 3-STATE OUTPUTS**

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**switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 2)**

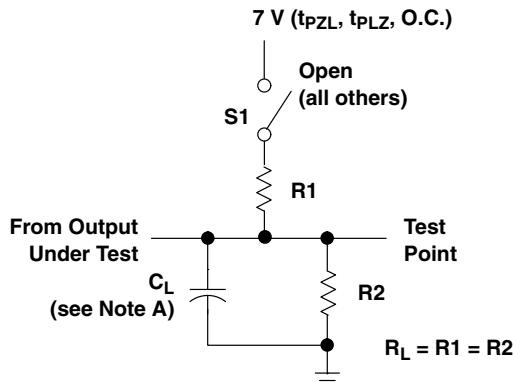
| PARAMETER | FROM<br>(INPUT)                               | TO<br>(OUTPUT) | $V_{CC} = 5 \text{ V}$ ,<br>$T_A = 25^\circ\text{C}$ |     |      | SN54BCT646 | SN74BCT646 | UNIT |
|-----------|---|----------------|--|-----|------|------------|------------|------|
|           |   |                | MIN  | TYP | MAX  | MIN        | MAX        |      |
| $f_{max}$ |   |                | 83   |     |      | 83         | 83         | MHz  |
| $t_{PLH}$ | CLKBA or CLKAB                                | A or B         | 3.6  | 7   | 9.4  | 3.6        | 12.4       | 3.6  |
| $t_{PHL}$ |   |                | 3.9  | 7   | 9.2  | 3.9        | 11.5       | 11.2 |
| $t_{PLH}$ | A or B  | B or A         | 3.1  | 6   | 8.1  | 3.1        | 11.1       | 9.5  |
| $t_{PHL}$ |   |                | 3.7  | 6.8 | 8.9  | 3.7        | 12.1       | 10.5 |
| $t_{PLH}$ | SAB or SBA <sup>†</sup><br>(with A or B high) | A or B         | 4.5  | 8.8 | 11.2 | 4.5        | 15.2       | 13.8 |
| $t_{PHL}$ |   |                | 3.3  | 6   | 8.1  | 3.3        | 9.8        | 9.1  |
| $t_{PLH}$ | SAB or SBA <sup>†</sup><br>(with A or B low)  | A or B         | 3.9  | 7.7 | 10.2 | 3.9        | 13.3       | 12   |
| $t_{PHL}$ |   |                | 4.7  | 8.3 | 10.8 | 4.7        | 13.7       | 12.9 |
| $t_{PZH}$ | $\overline{OE}$                               | A or B         | 4  | 7.9 | 10.7 | 4          | 14         | 13.2 |
| $t_{PZL}$ |   |                | 4.6  | 8.8 | 11.8 | 4.6        | 15.4       | 14.4 |
| $t_{PHZ}$ | $\overline{OE}$                               | A or B         | 4  | 7.2 | 9.4  | 4          | 12         | 10.9 |
| $t_{PLZ}$ |   |                | 3.4  | 7   | 9.3  | 3.4        | 11.6       | 10.5 |
| $t_{PZH}$ | DIR   | A or B         | 2.8  | 7.8 | 10.7 | 2.8        | 14         | 13.1 |
| $t_{PZL}$ |   |                | 3.8  | 8.9 | 11.9 | 3.8        | 15.6       | 14.6 |
| $t_{PHZ}$ | DIR   | A or B         | 3.8  | 8.4 | 10.7 | 3.8        | 13.2       | 12.6 |
| $t_{PLZ}$ |   |                | 3.2  | 7.3 | 9.9  | 3.2        | 12.6       | 11.8 |

<sup>†</sup> These parameters are measured with the internal output state of the storage register opposite that of the bus input.

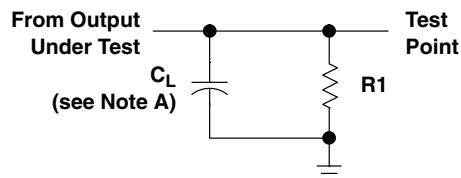
# SN54BCT646, SN74BCT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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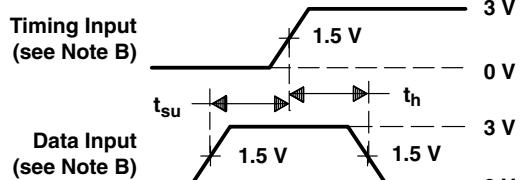
## PARAMETER MEASUREMENT INFORMATION



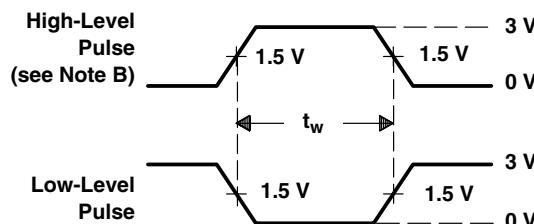
LOAD CIRCUIT FOR  
3-STATE AND OPEN-COLLECTOR OUTPUTS



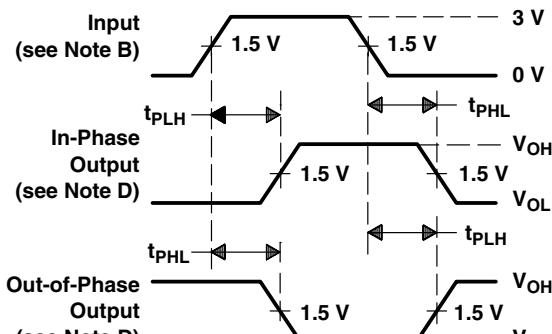
LOAD CIRCUIT FOR  
TOTEM-POLE OUTPUTS



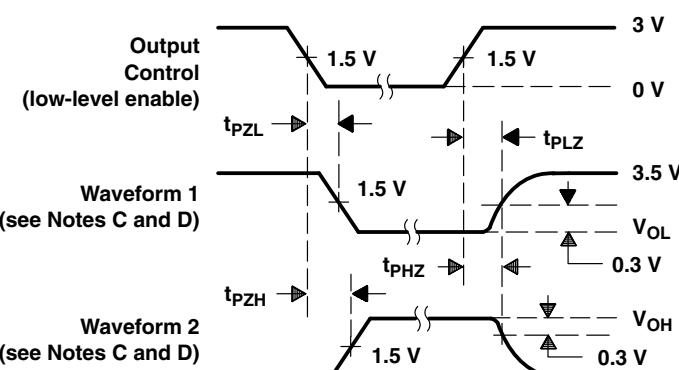
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES (see Note D)



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $t_r = t_f \leq 2.5$  ns, duty cycle = 50%.  
 C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.  
 Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E. When measuring propagation delay times of 3-state outputs, switch S1 is open.  
 F. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)  | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)              | Samples   |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|--------------------------------------|---|
| 5962-9155501M3A  | ACTIVE        | LCCC         | FK              | 28   | 1           | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9155501M3A<br>SNJ54BCT<br>646FK | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| 5962-9155501MLA  | ACTIVE        | CDIP         | JT              | 24   | 1           | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9155501MLA<br>SNJ54BCT646JT     | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN74BCT646DW     | ACTIVE        | SOIC         | DW              | 24   | 25          | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | BCT646                               | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN74BCT646DWE4   | ACTIVE        | SOIC         | DW              | 24   | 25          | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | BCT646                               | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SNJ54BCT646FK    | ACTIVE        | LCCC         | FK              | 28   | 1           | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9155501M3A<br>SNJ54BCT<br>646FK | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SNJ54BCT646JT    | ACTIVE        | CDIP         | JT              | 24   | 1           | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9155501MLA<br>SNJ54BCT646JT     | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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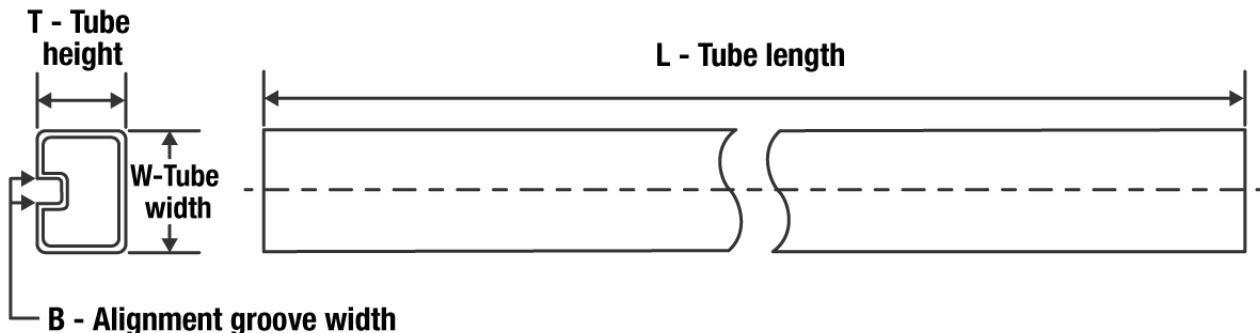
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54BCT646, SN74BCT646 :**

- Catalog : [SN74BCT646](#)
- Military : [SN54BCT646](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TUBE**


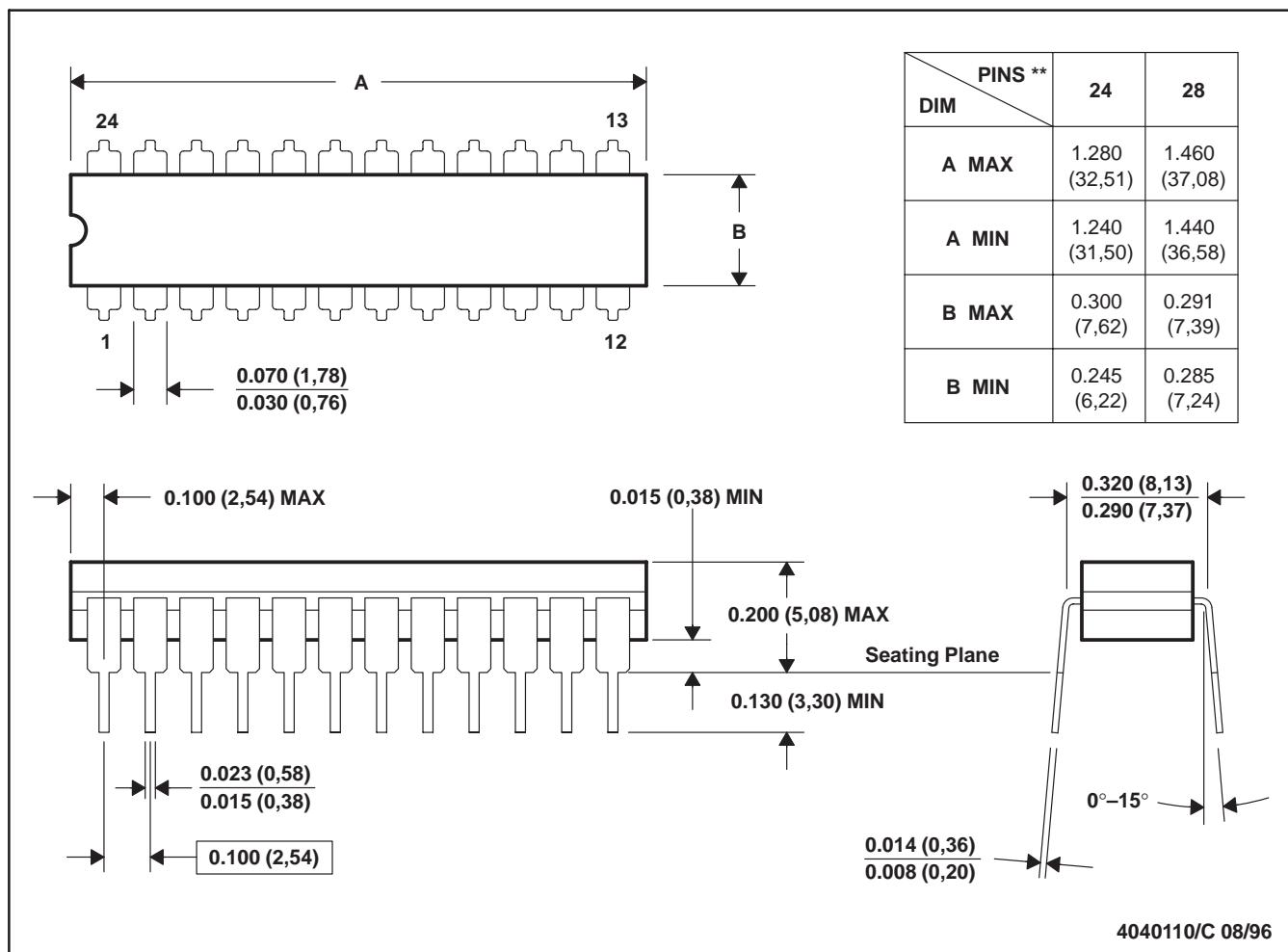
\*All dimensions are nominal

| Device         | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T ( $\mu$ m) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------------|--------|
| SN74BCT646DW   | DW           | SOIC         | 24   | 25  | 506.98 | 12.7   | 4826         | 6.6    |
| SN74BCT646DWE4 | DW           | SOIC         | 24   | 25  | 506.98 | 12.7   | 4826         | 6.6    |

## JT (R-GDIP-T\*\*)

24 LEADS SHOWN

## CERAMIC DUAL-IN-LINE



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

FK (S-CQCC-N\*\*)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



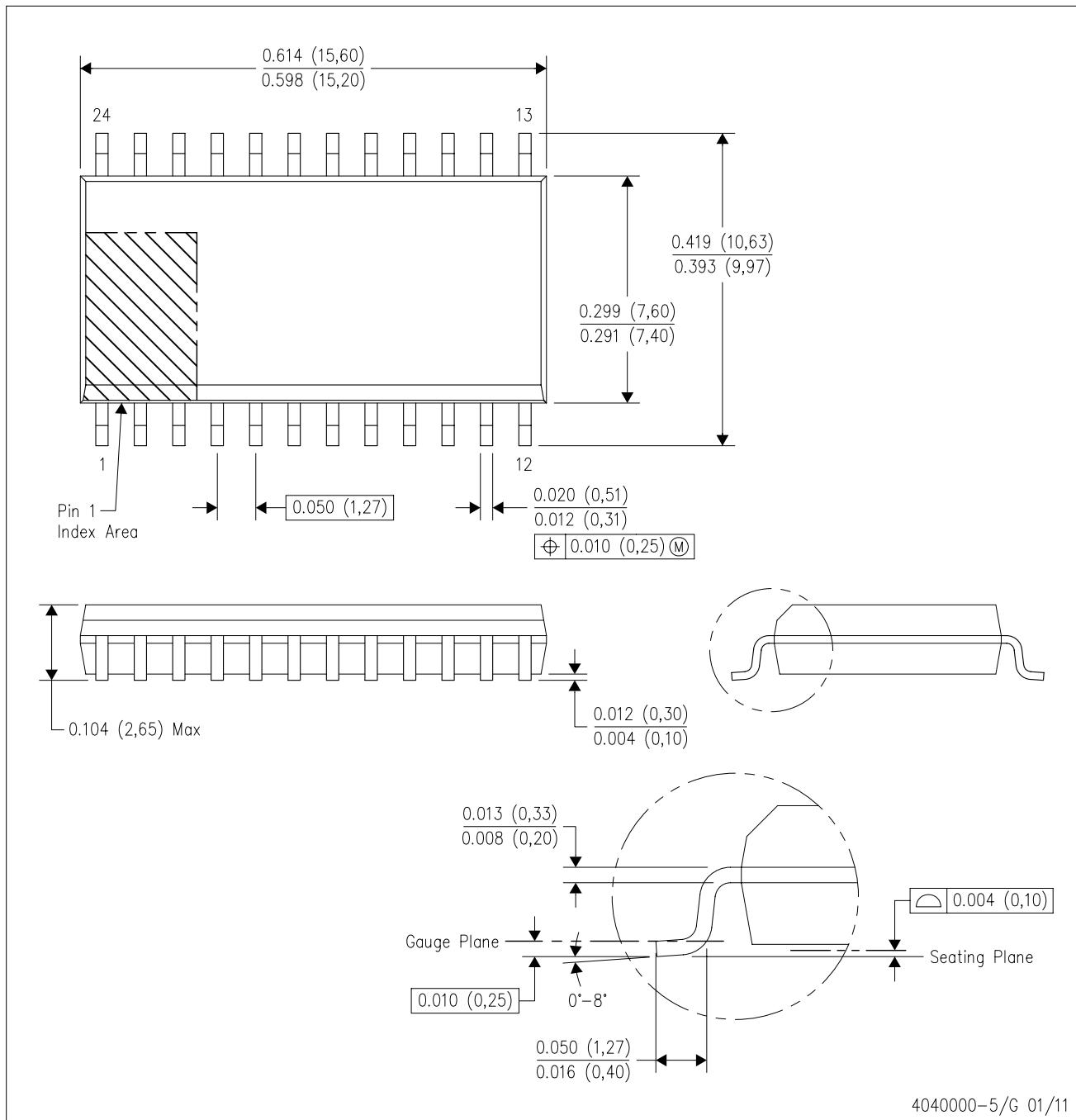
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

4040140/D 01/11

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES:

- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-013 variation AD.

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