



PESD5V0F1BSH

Ultra low capacitance bidirectional ESD protection diode

24 March 2016

Product data sheet

1. General description

Ultra low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode designed to protect one signal line from the damage caused by ESD and other transients. The device is housed in a leadless super small DSN0402-2 (SOD992) Surface-Mounted Device (SMD) package.

2. Features and benefits

- Bidirectional ESD protection of one line
- Extremely low diode capacitance $C_d = 0.2$ pF
- Ultra flat package: 0.12 mm high
- Ultra low leakage current: $I_{RM} < 1$ nA
- IEC 61000-4-2, level 4

3. Applications

ESD and surge protection for:

- ultra high-speed datalines
- generic interface lines

in portable electronics, communication, consumer and computing devices.

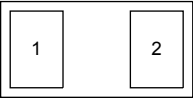
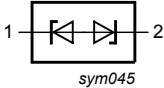
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_d	diode capacitance	$f = 1$ MHz; $V_R = 0$ V; $T_j = 25$ °C	-	0.2	0.3	pF
V_{RWM}	reverse standoff voltage	$T_j = 25$ °C	-	-	5	V

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode	 Transparent top view DSN0402-2 (SOD992)	 <i>sym045</i>
2	K2	cathode		

6. Ordering information

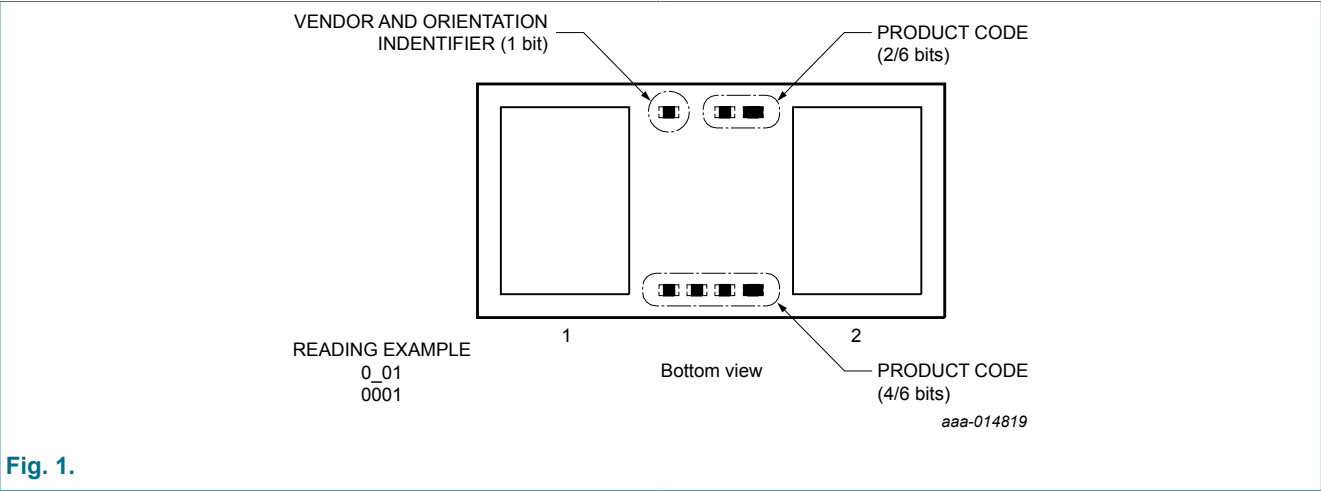
Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD5V0F1BSH	DSN0402-2	DSN0402-2, leadless tiny package; 2 terminals	SOD992

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD5V0F1BSH	0_00 0010

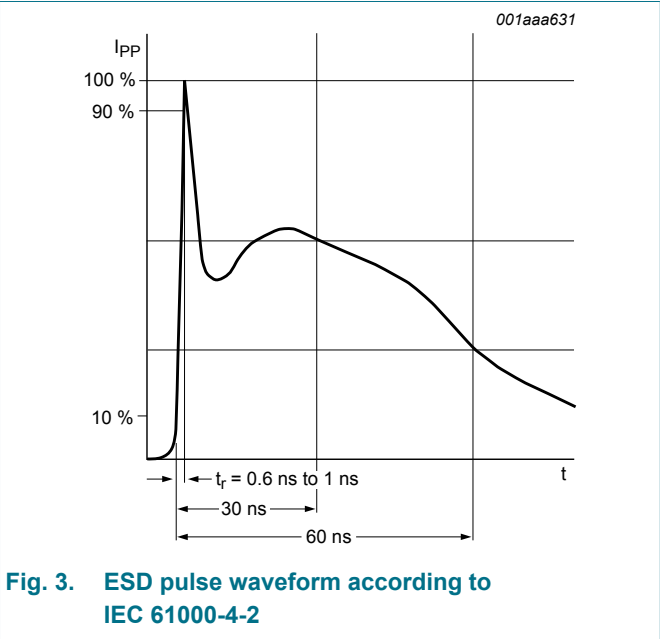
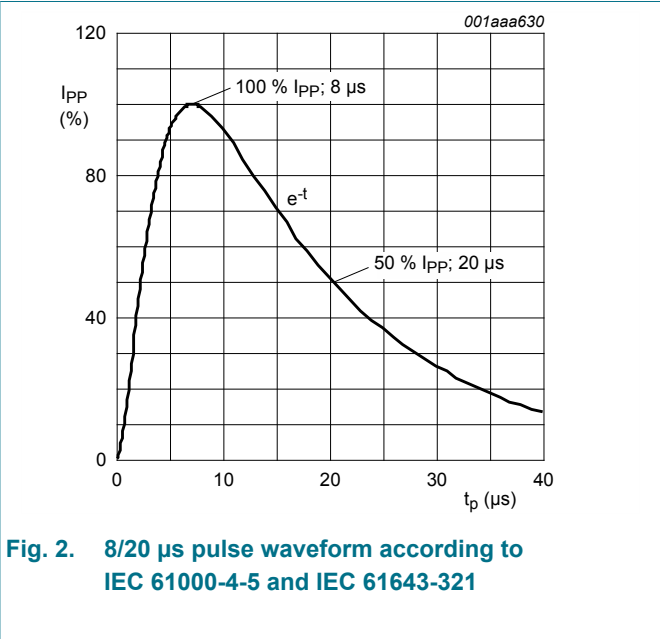


8. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
I _{PPM}	peak pulse current	t _p = 8/20 μs	[1]	-	2.5	A
T _{amb}	ambient temperature			-55	125	°C
T _{stg}	storage temperature			-55	150	°C
ESD maximum ratings						
V _{ESD}	electrostatic discharge voltage	contact discharge	[2]	-	8	kV
		air discharge	[2]	-	15	kV

- [1] Device stressed with non-repetitive current pulses (8/20 μs exponential decay waveform according to IEC 61000-4-5 and IEC 61643-321).
- [2] Device stressed with ten non-repetitive ESD pulses.

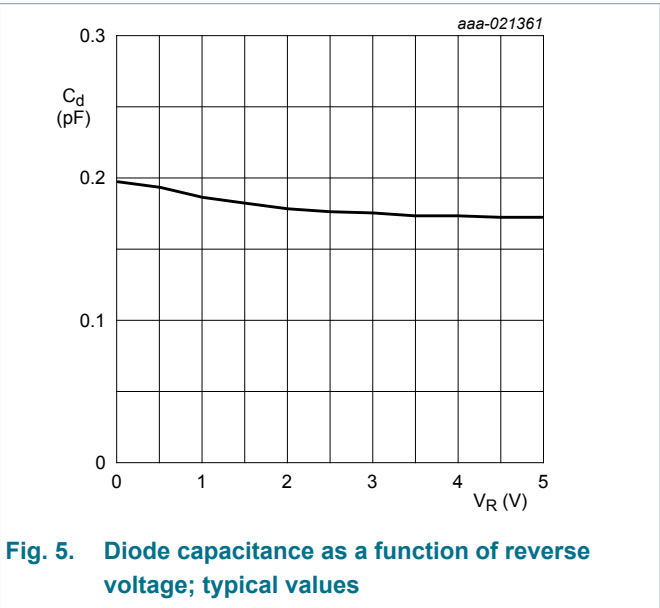
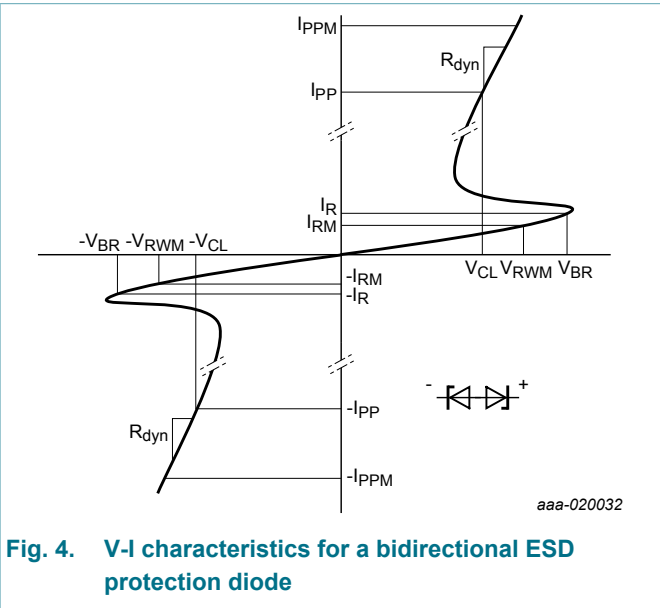


9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	$T_j = 25\text{ }^{\circ}\text{C}$		-	-	5	V
V_{BR}	breakdown voltage	$I_R = 1\text{ mA}; T_j = 25\text{ }^{\circ}\text{C}$		7.2	9.2	11.2	V
I_{RM}	reverse leakage current	$V_R = 5\text{ V}; T_j = 25\text{ }^{\circ}\text{C}$		-	1	25	nA
C_d	diode capacitance	$f = 1\text{ MHz}; V_R = 0\text{ V}; T_j = 25\text{ }^{\circ}\text{C}$		-	0.2	0.3	pF
V_{CL}	clamping voltage	$I_{PP} = 2.5\text{ A}; T_j = 25\text{ }^{\circ}\text{C}$	[1]	-	4.5	6	V
R_{dyn}	dynamic resistance	$I_R = 10\text{ A}; T_j = 25\text{ }^{\circ}\text{C}$	[2]	-	0.45	-	Ω

- [1] Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5 and IEC 61643-321.
- [2] Non-repetitive current pulse, Transmission Line Pulse (TLP) $t_p = 100\text{ ns}$; square pulse; ANSI / ESD STM5.1-2008



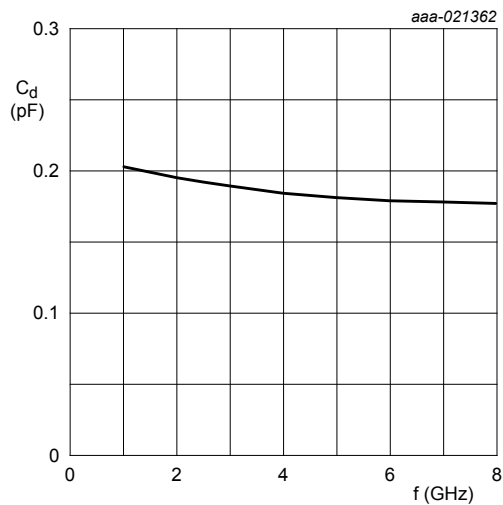


Fig. 6. Diode capacitance as a function of frequency; typical values

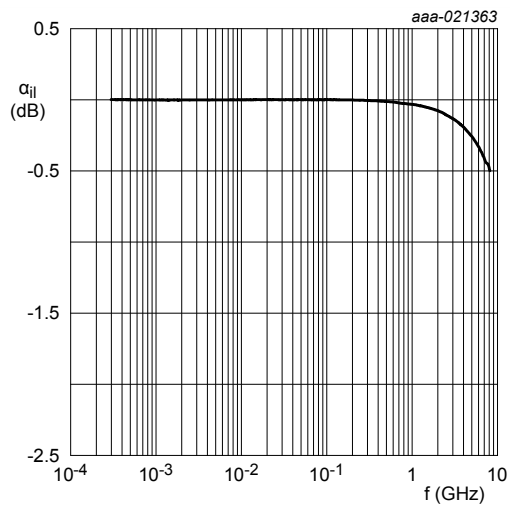
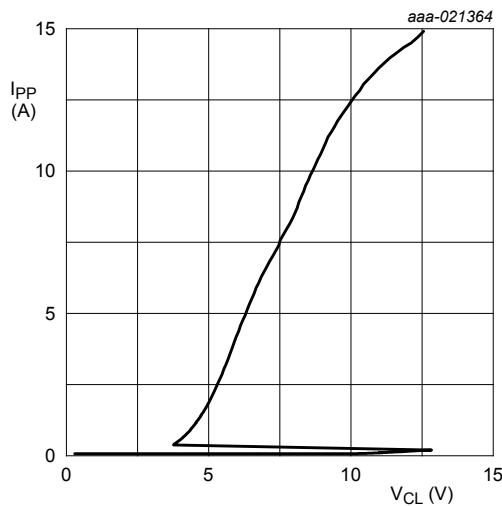


Fig. 7. Insertion loss; typical values



t_p = 100 ns; Transmission Line Pulse (TLP)

Fig. 8. Dynamic resistance with positive clamping voltage

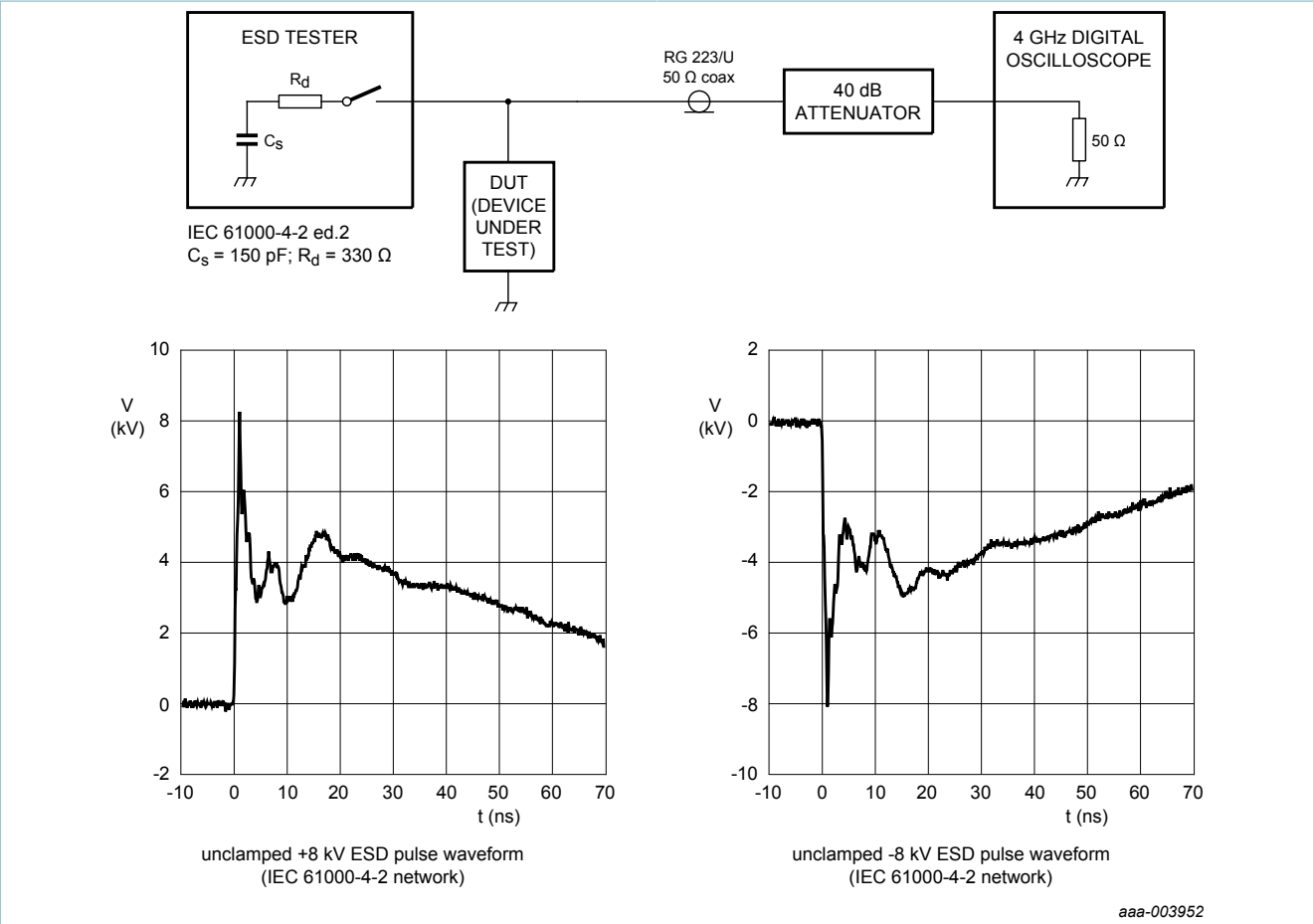


Fig. 9. ESD clamping test setup and waveforms

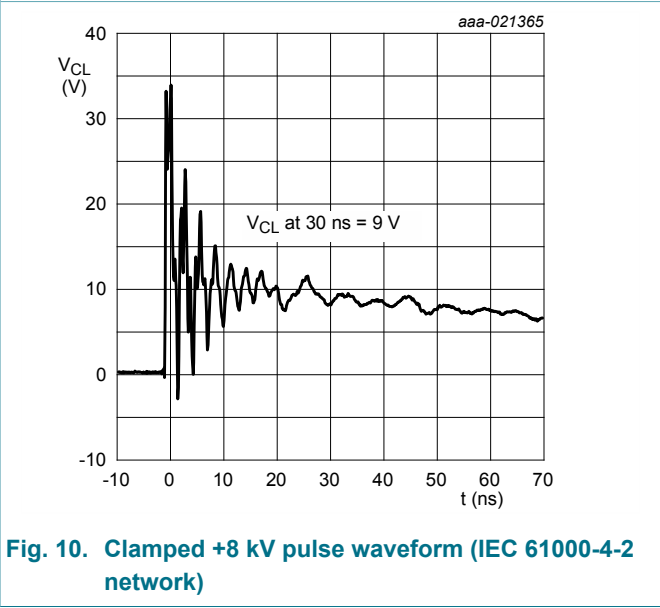


Fig. 10. Clamped +8 kV pulse waveform (IEC 61000-4-2 network)

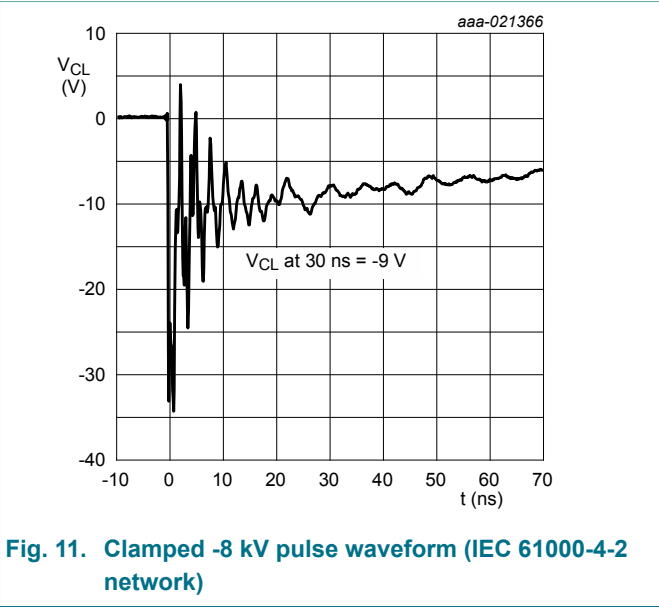


Fig. 11. Clamped -8 kV pulse waveform (IEC 61000-4-2 network)

10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground. The device is not designed to be used on lines connected to a DC supply.

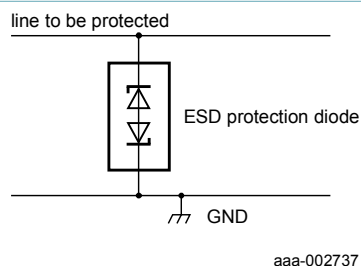


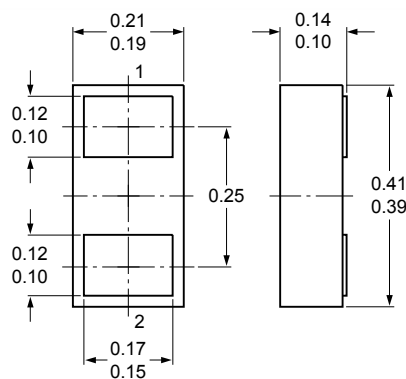
Fig. 12. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Package outline



Dimensions in mm

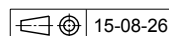


Fig. 13. Package outline DSN0402-2 (SOD992)

12. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0F1BSH v.2	20160324	Product data sheet	-	PESD5V0F1BSH v.1
Modification:	Section limiting values: updated ambient temperature			
PESD5V0F1BSH v.1	20151218	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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