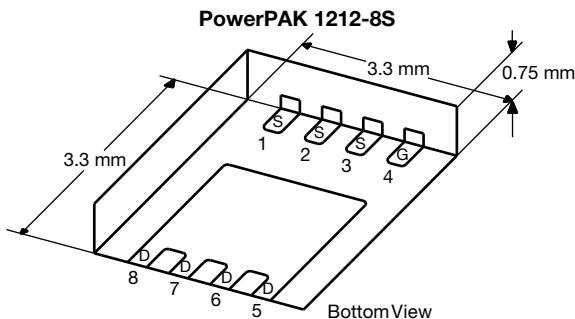


N-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω) (Max.)	I_D (A) ^f	Q_g (Typ.)
100	0.0210 at $V_{GS} = 10$ V	36.5	10 nC
	0.0230 at $V_{GS} = 7.5$ V	35	
	0.0260 at $V_{GS} = 6$ V	32	


Ordering Information:

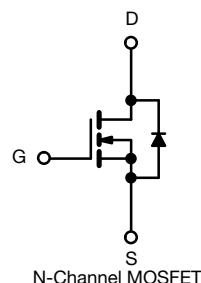
SiSS40DN-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- ThunderFET® Technology Optimizes Balance of $R_{DS(on)}$, Q_g , Q_{sw} and Q_{oss}
- 100 % R_g and UIS Tested
- Material categorization:
For definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT
HALOGEN
FREE
APPLICATIONS

- Primary side switch
- Synchronous Rectification
- DC/DC Conversion
- Load Switching
- Boost Converters
- DC/AC Inverters



ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	100	V	
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current ($T_J = 150$ °C)	I_D	36.5	A	
		29		
		9.7 ^{a, b}		
		7.8 ^{a, b}		
Pulsed Drain Current ($t = 300$ µs)	I_{DM}	60	A	
Continuous Source-Drain Diode Current	I_S	40 ^g		
		3.1 ^{a, b}		
Single Pulse Avalanche Current	I_{AS}	20	mJ	
Single Pulse Avalanche Energy	E_{AS}	20		
Maximum Power Dissipation	P_D	52	W	
		33		
		3.7 ^{a, b}		
		2.4 ^{a, b}		
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) ^{c, d}		260		

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, e}	R_{thJA}	26	33	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	1.9	2.4	

Notes:

- Surface mounted on 1" x 1" FR4 board.
- $t = 10$ s.
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 81 °C/W.
- Based on $T_C = 25$ °C.
- Package limited.

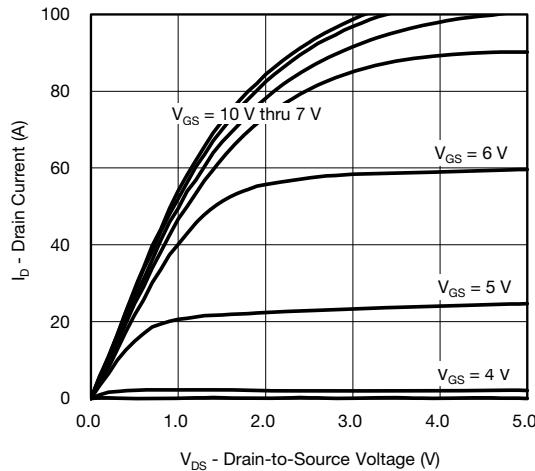
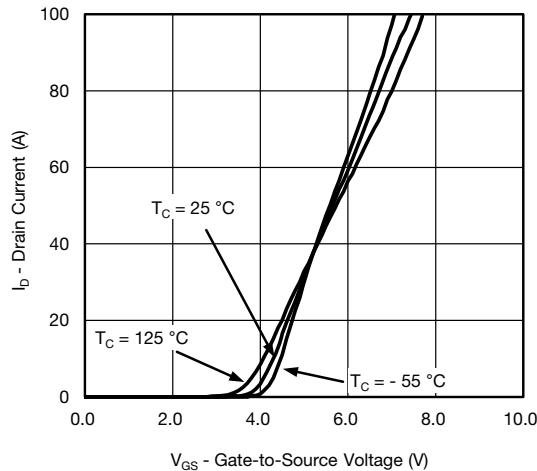
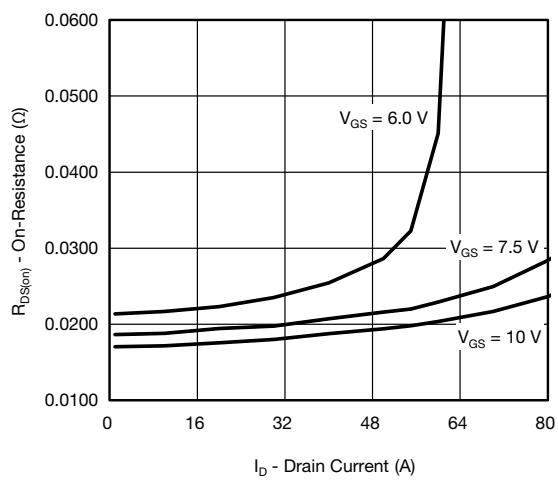
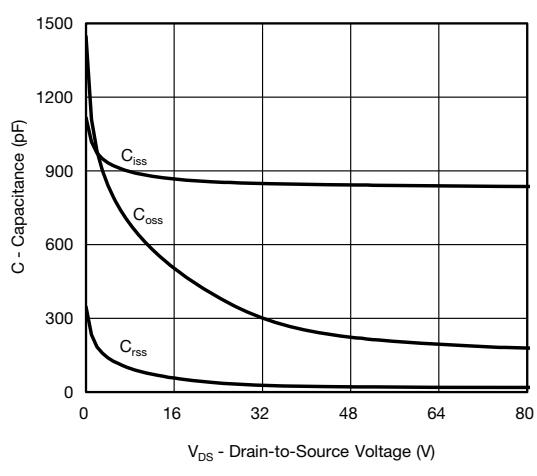
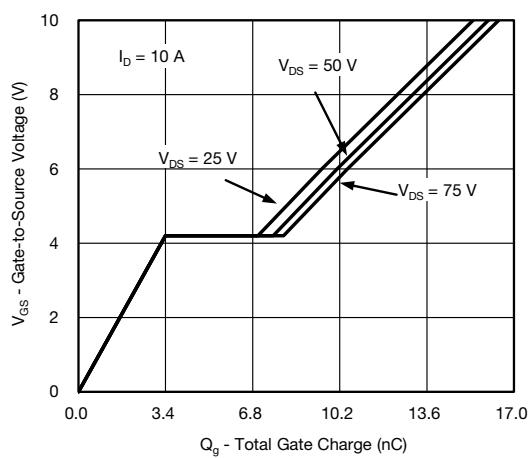
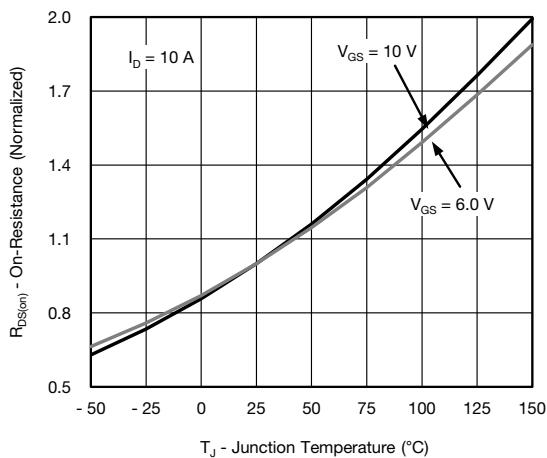
SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$	100			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250 \mu\text{A}$		61		mV/°C
$V_{GS(\text{th})}$ Temperature Coefficient	$\Delta V_{GS(\text{th})}/T_J$			- 6.8		
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	2.3		3.5	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100 \text{ V}$, $V_{GS} = 0 \text{ V}$			1	μA
		$V_{DS} = 100 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 55^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{DS} \geq 5 \text{ V}$, $V_{GS} = 10 \text{ V}$	20			A
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}$, $I_D = 10 \text{ A}$		0.0176	0.0210	Ω
		$V_{GS} = 7.5 \text{ V}$, $I_D = 7 \text{ A}$		0.0190	0.0230	
		$V_{GS} = 6 \text{ V}$, $I_D = 5 \text{ A}$		0.0216	0.0260	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15 \text{ V}$, $I_D = 10 \text{ A}$		25		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 50 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$		845		pF
Output Capacitance	C_{oss}			220		
Reverse Transfer Capacitance	C_{rss}			21.5		
Total Gate Charge	Q_g	$V_{DS} = 50 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_D = 10 \text{ A}$		16	24	nC
		$V_{DS} = 50 \text{ V}$, $V_{GS} = 7.5 \text{ V}$, $I_D = 10 \text{ A}$		12.2	18.5	
Gate-Source Charge	Q_{gs}	$V_{DS} = 50 \text{ V}$, $V_{GS} = 6 \text{ V}$, $I_D = 10 \text{ A}$		10	15	
Gate-Drain Charge	Q_{gd}			3.4		
Output Charge	Q_{oss}	$V_{DS} = 50 \text{ V}$, $V_{GS} = 0 \text{ V}$		23	35	
Gate Resistance	R_g	$f = 1 \text{ MHz}$	0.2	0.9	1.5	Ω
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = 50 \text{ V}$, $R_L = 5 \Omega$ $I_D \geq 10 \text{ A}$, $V_{GEN} = 6 \text{ V}$, $R_g = 1 \Omega$		14	28	ns
Rise Time	t_r			5	10	
Turn-Off Delay Time	$t_{d(\text{off})}$			14	28	
Fall Time	t_f			5	10	
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = 50 \text{ V}$, $R_L = 5 \Omega$ $I_D \geq 10 \text{ A}$, $V_{GEN} = 10 \text{ V}$, $R_g = 1 \Omega$		12	24	
Rise Time	t_r			5	10	
Turn-Off Delay Time	$t_{d(\text{off})}$			19	38	
Fall Time	t_f			5	10	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$			40	A
Pulse Diode Forward Current ^a	I_{SM}				60	
Body Diode Voltage	V_{SD}	$I_S = 4 \text{ A}$, $V_{GS} = 0 \text{ V}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $T_J = 25^\circ\text{C}$		39	75	ns
Body Diode Reverse Recovery Charge	Q_{rr}			49	95	nC
Reverse Recovery Fall Time	t_a			24		ns
Reverse Recovery Rise Time	t_b			15		

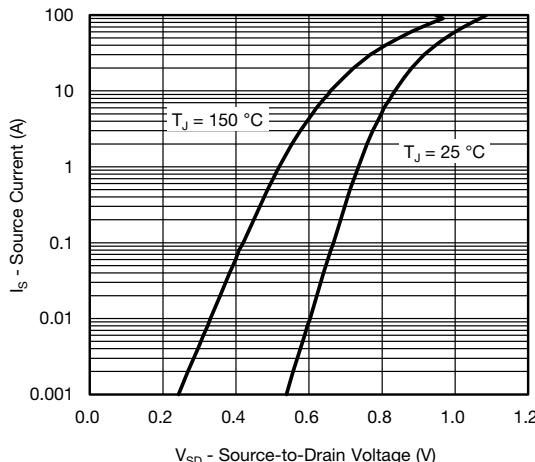
Notes:

a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

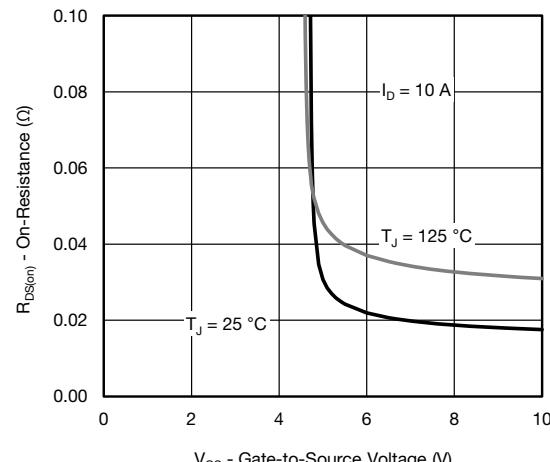
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

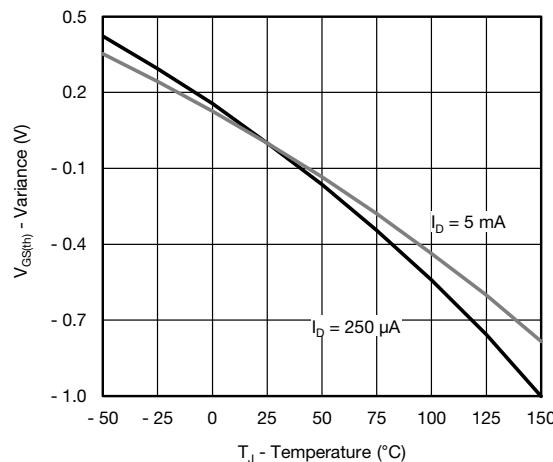
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



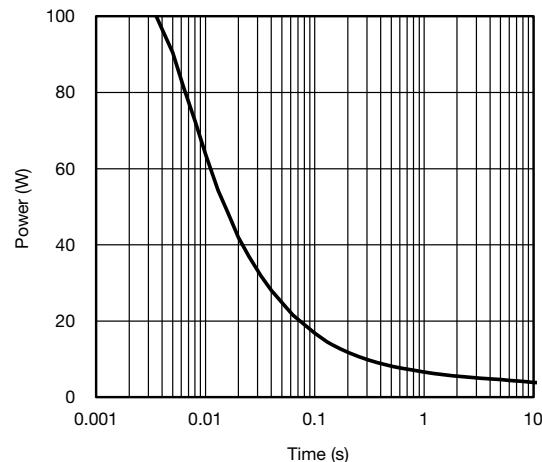
Source-Drain Diode Forward Voltage



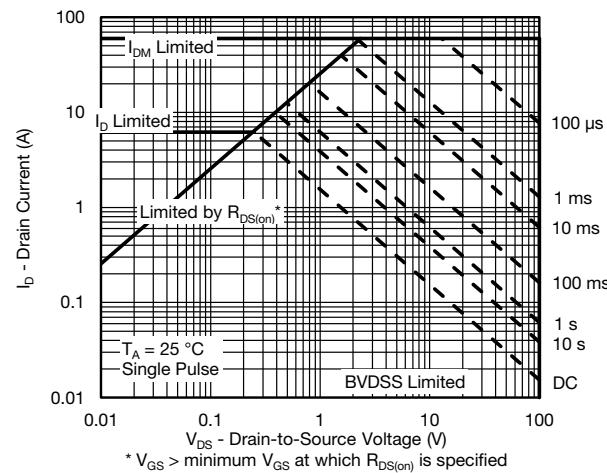
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

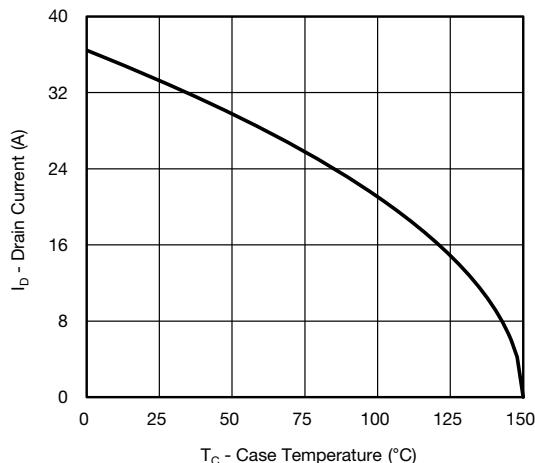


Single Pulse Power, Junction-to-Ambient

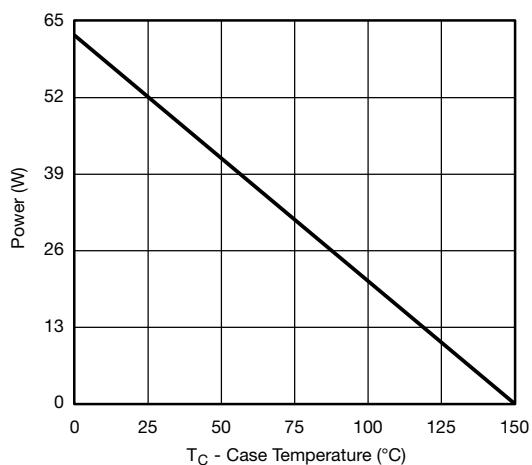


Safe Operating Area, Junction-to-Ambient

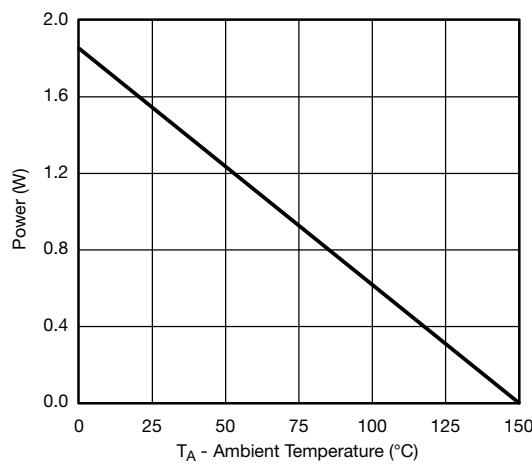
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*

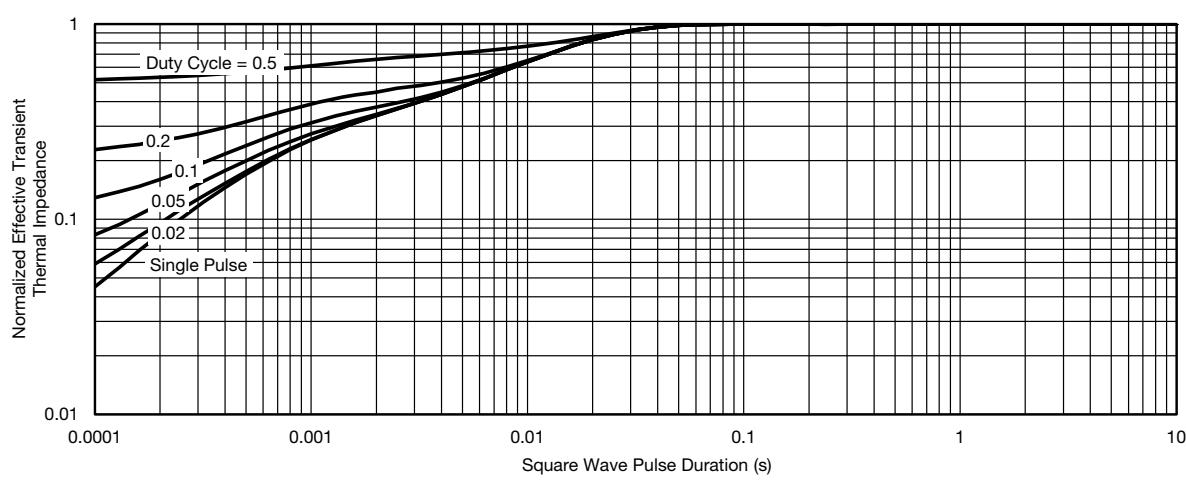
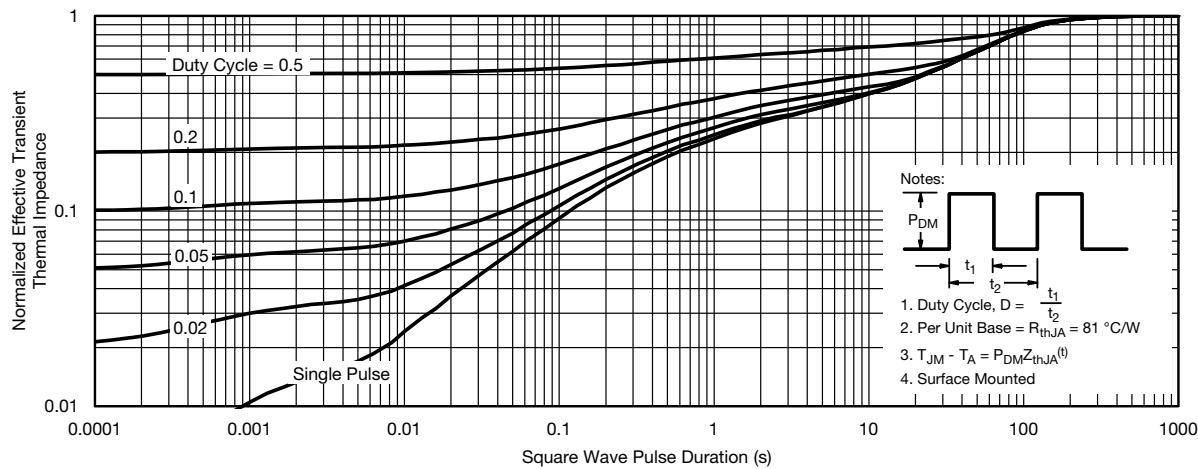


Power, Junction-to-Case



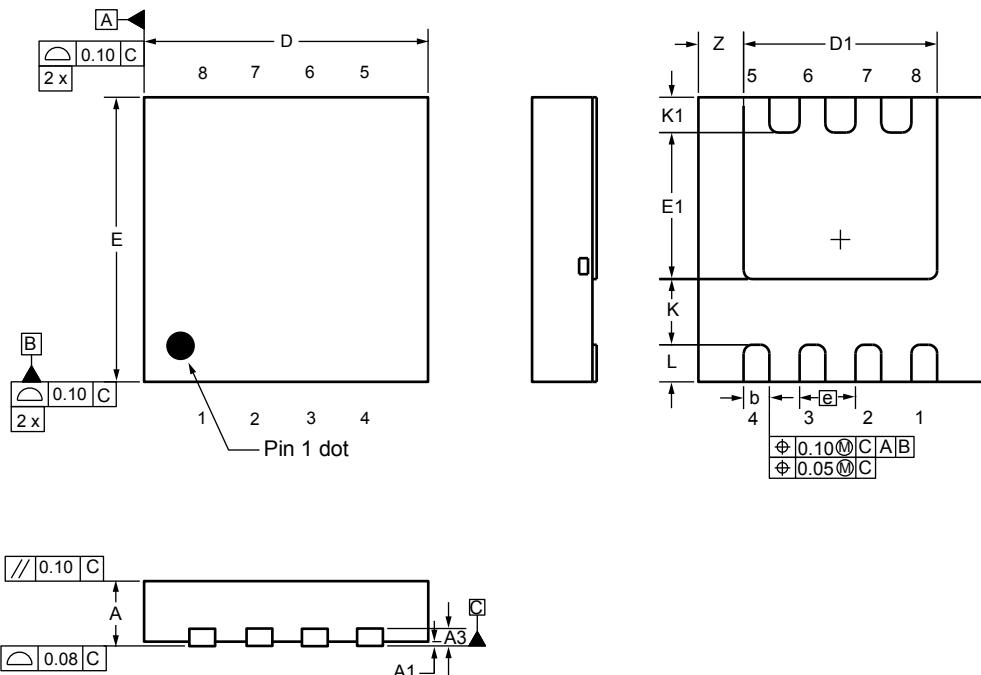
Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(\max.)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


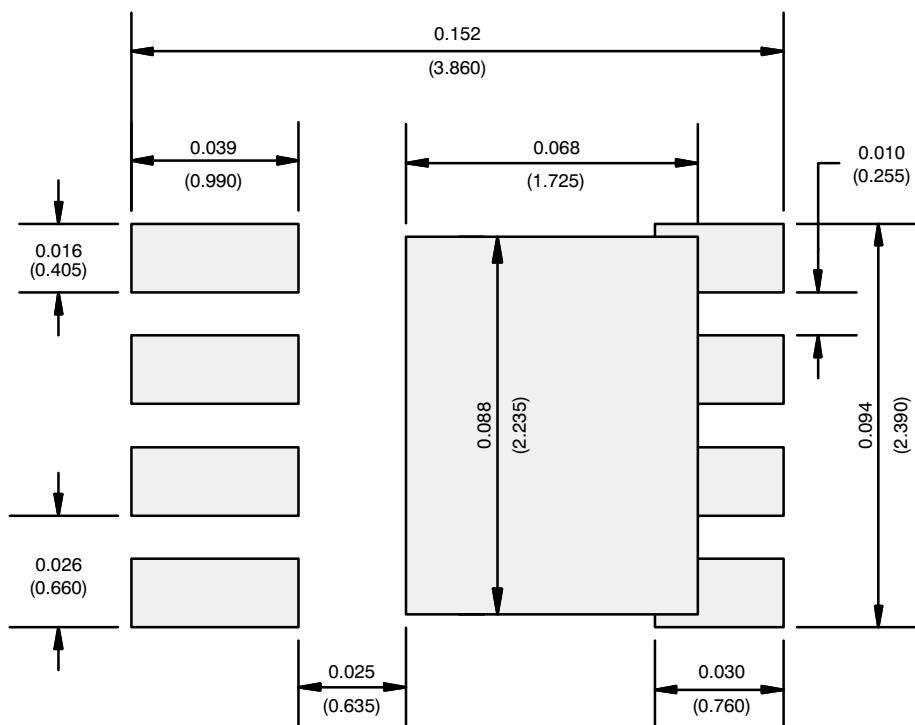
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Case Outline for PowerPAK® 1212-8S



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.67	0.75	0.83	0.026	0.030	0.033
A1	0.00	-	0.05	0.000	-	0.002
A3	0.20 ref.			0.008 ref		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.15	2.25	2.35	0.085	0.089	0.093
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	1.60	1.70	1.80	0.063	0.067	0.071
e	0.65 bsc.			0.026 bsc.		
K	0.76 ref.			0.030 ref.		
K1	0.41 ref.			0.016 ref.		
L	0.33	0.43	0.53	0.013	0.017	0.021
Z	0.525 ref.			0.021 ref.		

ECN: C20-0862-Rev. B, 20-Jul-2020
DWG: 6008

RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single

Recommended Minimum Pads
Dimensions in Inches/(mm)

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