

0.2 GHz to 8 GHz, GaAs, HBT MMIC, Divide by 8 Prescaler

Data Sheet HMC434

FEATURES

Ultralow SSB phase noise: -150 dBc/Hz typical

Single-ended input/outputs Output power: -2 dBm typical Single supply operation: 3 V

Ultrasmall, surface-mount, 2.90 mm \times 2.80 mm, 6-lead SOT-23

package

APPLICATIONS

DC to C band PLL prescalers

Very small aperture terminal (VSAT) radios

Unlicensed national information infrastructure (UNII) and point to point radios

IEEE 802.11a and high performance radio local area network (HiperLAN) WLAN

Fiber optics

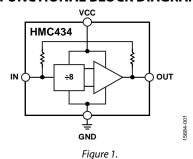
Cellular/3G infrastructure

GENERAL DESCRIPTION

The HMC434 is a low noise, static, divide by 8 prescaler monolithic microwave integrated circuit (MMIC) utilizing indium gallium phosphide/gallium arsenide (InGaP/GaAs) heterojunction bipolar transistor (HBT) technology in an ultrasmall surface-mount 6-lead SOT-23 package.

The HMC434 operates from near dc (square wave) or 200 MHz (sine wave) to 8 GHz input frequency with a single 3 V dc supply.

FUNCTIONAL BLOCK DIAGRAM



The HMC434 features single-ended inputs and outputs for reduced component count and cost. The low additive single sideband (SSB) phase noise of -150 dBc/Hz at 100 kHz offset helps the user maintain optimal system noise performance.

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REVISION HISTORY
4/2019—Rev. F to Rev. G
Change to Figure 116
Changes to Ordering Guide
8/2017—Rev. E to Rev. F
Added Endnote 2, Table 1

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This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

3/2017—Rev. 04.0410 to Rev. E

Updated Format
Changes to Features Section, Figure 1, and General Description
Section1
Changes to Table 13
Changes to Table 24
Added Thermal Resistance Section and Table 3; Renumbered
Sequentially4
Added Figure 2; Renumbered Sequentially5
Changes to Table 4, Figure 4, Figure 5, and Figure 65
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Added Applications Information Section7
Changes to Evaluation Board PCB Section, Table 5, and
Figure 13, and Figure 147
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SPECIFICATIONS

 V_{CC} = 3 V, T_A = 25°C, 50 Ω system, unless otherwise noted. P_{IN} is input power.

Table 1.

Parameter	Min	Тур	Max	Unit	Test Conditions / Comments
RADIO FREQUENCY (RF) INPUT					
Frequency 1, 2	0.2		8	GHz	Sine wave input
Power	-10	0	+10	dBm	$f_{IN} = 1.0 \text{ GHz to } 3.0 \text{ GHz}$
	0	0	10	dBm	$f_{IN} = 3.0 \text{ GHz to } 8.0 \text{ GHz}$
RF OUTPUT					
SSB Phase Noise		-150		dBc/Hz	100 kHz offset, $P_{IN} = 0$ dBm, $f_{IN} = 4.0$ GHz
Power	-5	-2		dBm	$f_{IN} = 1.0 \text{ GHz to } 8.0 \text{ GHz}$
REVERSE LEAKAGE		-25		dBm	$P_{IN} = 0$ dBm, $f_{IN} = 4.0$ GHz, output terminated
SUPPLY					
Voltage (Vcc)	2.85	3	3.15	V	
Current (Icc)		62	83	mA	

¹ Below 200 MHz, a square wave input is required. ² For stable operation without an input signal, refer to AN-1463.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (Vcc)	−0.3 V to +3.5 V
RF Input Power ($V_{CC} = 3 \text{ V}$)	13 dBm
Temperature	
Operating	−40°C to +85°C
Storage	−65°C to +125°C
Junction, T _J	135°C
Nominal ($T_A = 85^{\circ}C$)	99°C
Reflow	260°C
ESD Sensitivity	
Human Body Model (HBM)	Class 0

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

 θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JA}^1	θ_{JC}^2	Unit
RJ-6	359	70	°C/W

¹ Simulated values per JEDEC JESD51-12 standards.

ESD CAUTION

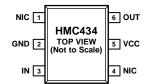


ESD (electrostatic discharge) sensitive device.Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

² Junction to GND package pin.

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES

1. NOT INTERNALLY CONNECTED. THESE PINS CAN BE CONNECTED TO RF AND DC GROUND WITHOUT AFFECTING PERFORMANCE. THE NIC PINS ARE TYPICALLY TIED TO GND FOR ENHANCED THERMAL PERFORMANCE (BUT NOT REQUIRED).

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4	NIC	Not Internally Connected. These pins can be connected to RF and dc ground without affecting performance. The NIC pins are typically tied to GND for enhanced thermal performance (but not required).
2	GND	Ground. This pin must be connected to both RF and dc ground.
3	IN	RF Input. This pin must be dc blocked.
5	VCC	Supply Voltage (3 V).
6	OUT	RF Output. This pin must be dc blocked.

INTERFACE SCHEMATICS



Figure 3. GND Interface Schematic

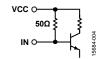


Figure 4. IN Interface Schematic



Figure 5. OUT Interface Schematic



Figure 6. VCC Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

In Figure 9, PFEEDTHROUGH is the power of the output spectrum at the input frequency.

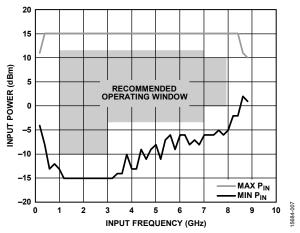


Figure 7. Input Sensitivity Window

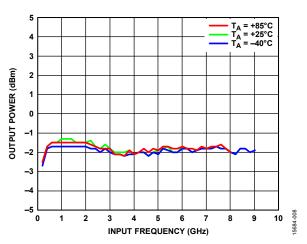


Figure 8. Output Power vs. Frequency at Various Temperatures

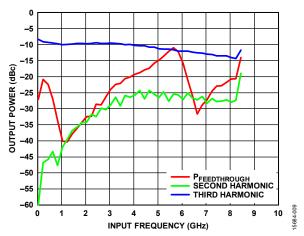


Figure 9. Output Harmonic Content ($P_{IN} = 0 dBm$)

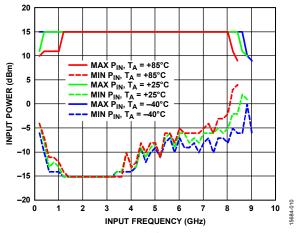


Figure 10. Input Sensitivity Window at Various Temperatures

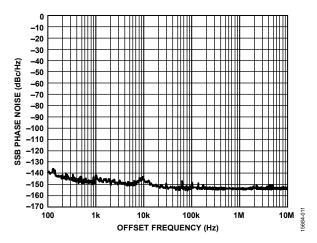


Figure 11. Residual SSB Phase Noise (Carrier Frequency = 320 MHz, $P_{IN} = 0 \text{ dBm}$)

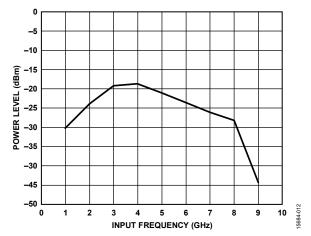


Figure 12. Reverse Leakage ($P_{IN} = 0 dBm$)

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APPLICATIONS INFORMATION EVALUATION BOARD PCB

Use RF circuit design techniques for the PCB used in the application. Ensure that signal lines have 50 Ω impedance when the package ground leads are connected directly to the ground plane (see Figure 14). Use a sufficient number of via holes to connect the top and bottom ground planes.

The evaluation board has two connectors, as shown in Figure 14. The RF input connector (J1) and the RF output connector (J2) are PCB mount SMA connectors.

The evaluation board is powered from a single 3 V supply; connect this supply using the J3 (VCC) and J4 (GND) test points.

See Figure 13 and Table 5 for the evaluation board schematic and the bill of materials, respectively.

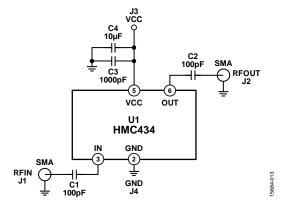


Figure 13. Evaluation Board Schematic

Table 5. List of Materials for Evaluation PCB 105675-HMC4341

Item	Description
J1, J2	PCB mount SMA RF connectors
J3, J4	DC pins
C1, C2	100 pF capacitors, 0402 package
C3	1000 pF capacitors, 0402 package
C4	10 μF tantalum capacitors, 1206 package
U1	HMC434/HMC434E, divide by 8
PCB ²	105199 evaluation board

¹ 105199 is the raw bare PCB identifier. Reference 105675-HMC434 when ordering the complete evaluation PCB.

² Circuit board material: Arlon 25FR or Rogers RO4350B.

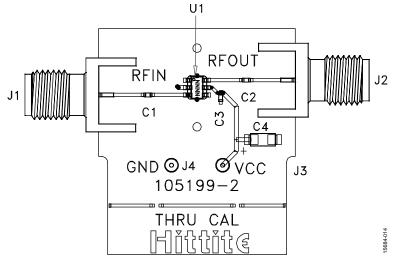


Figure 14. Evaluation Board—Top View

PCB MATERIAL STACKUP

The evaluation board is built using Arlon 25FR or Rogers RO4350B and standard FR4 materials. RF trace widths are designed to achieve a controlled 50 Ω characteristic impedance. The complete PCB stackup is shown in Figure 15.

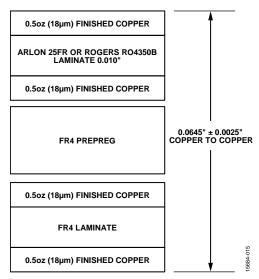


Figure 15. Evaluation Board PCB Stackup

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OUTLINE DIMENSIONS

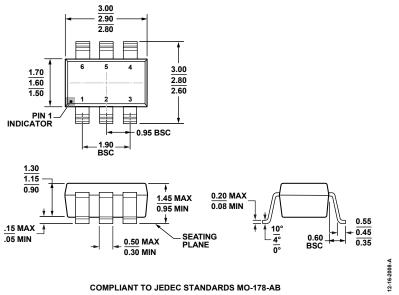


Figure 16. 6-Lead Small Outline Transistor Package [SOT-23] (RJ-6) Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
HMC434	-40°C to +85°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6
HMC434TR	-40°C to +85°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6
HMC434E	-40°C to +85°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6
HMC434ETR	-40°C to +85°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6
105675-HMC434		Evaluation Board	

¹ The HMC434E and HMC434ETR are RoHS compliant parts.