

Ultra Low Noise, High Current

E-PHEMT Transistor

TAV1-541+

50Ω 0.045 to 6 GHz

The Big Deal

- Low Noise Figure, 0.4 dB
- Gain, 24 dB typ. at 0.9 GHz
- High OIP3, +32 dBm



CASE STYLE: TE2769

Product Overview

TAV1-541+ is a low noise, high IP3 transistor device manufactured using E-PHEMPT* technology enabling it to work with a single positive supply voltage. It has outstanding Noise figure, particularly below 2.5 GHz, and when combining this noise figure with IP3 performance in a single device it makes it an ideal amplifier for multiple applications.

Key Features

Feature	Advantages
Wideband, 0.045 to 6 GHz	Use in multiple applications: UHF, VHF, communication infrastructure
High Gain, Low noise figure	High Gain limits the effect of noise figure due to previous stages
Small size, 1.18 x 1.42 x 0.85 mm, MCLP package	Small foot print saves space in dense layouts while providing low inductance, repeatable transitions, and excellent thermal contact to the PCB.

* Enhancement mode Pseudomorphic High Electron Mobility Transistor.



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E-PHEMT Transistor

0.045-6 GHz

Product Features

- Low Noise Figure, 0.4 dB
- Gain, 24 dB typ. at 0.9 GHz
- High Output IP3, +32 dBm at 2 GHz, 60mA, 4V
- Output Power at 1dB compression, +21dBm, 60mA, 4V
- Wide bandwidth
- External biasing and matching required



TAV1-541+

CASE STYLE: TE2769

Typical Applications

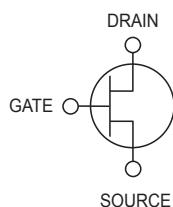
- Cellular
- ISM
- GSM
- WCDMA
- WiMax
- WLAN
- UNII and HIPERLAN

+RoHS Compliant
The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

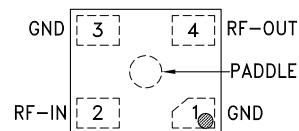
General Description

TAV1-541+ is a low noise, high IP3 transistor device manufactured using E-PHEMPT* technology enabling it to work with a single positive supply voltage. It has outstanding Noise figure, particularly below 2.5 GHz, and when combining this noise figure with IP3 performance in a single device it makes it an ideal amplifier for multiple applications.

simplified schematic and pin description



TOP VIEW



Function	Pad Number	Description
RF-IN	2	Gate used for RF input
RF-OUT	4	Drain used for RF output
GND	1,3 and Paddle	Source terminal and Paddle, normally connected to ground.

* Enhancement mode Pseudomorphic High Electron Mobility Transistor.

REV. OR
ECO-001761
TAV1-541+
OM/C/P/AM
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Electrical Specifications at $T_{AMB}=25^{\circ}\text{C}$, Frequency 0.045 to 6 GHz

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
DC Specifications						
V_{GS}	Operational Gate Voltage	$V_{DS}=3\text{V}$, $I_{DS}=60\text{ mA}$	0.37	0.48	0.69	V
V_{TH}	Threshold Voltage	$V_{DS}=3\text{V}$, $I_{DS}=4\text{ mA}$	0.18	0.26	0.38	V
I_{DSS}	Saturated Drain Current	$V_{DS}=3\text{V}$, $V_{GS}=0\text{ V}$	—	1.0	5.0	uA
G_M	Transconductance	$=3$, $=\Delta / \Delta$ $\Delta = \frac{2}{1}$ $\frac{1}{1} = 60$ $\frac{2}{1} = +0.05$	230	392	560	mS
I_{GSS}	Gate leakage Current	$V_{GD}=V_{GS}=-3\text{V}$	—	—	200	μA
RF Specifications ¹ , $Z_0=50\text{ Ohms}$ (Figure 1)						
NF	Noise Figure	$V_{DS}=3\text{V}$, $I_{DS}=60\text{ mA}$	$f=0.9\text{ GHz}$	—	0.4	dB
			$f=2.0\text{ GHz}$		0.6	
Gain	Gain		$f=3.9\text{ GHz}$		0.9	
		$V_{DS}=4\text{V}$, $I_{DS}=60\text{ mA}$	$f=5.8\text{ GHz}$		1.4	
			$f=2.0\text{ GHz}$		0.7	
		$V_{DS}=3\text{V}$, $I_{DS}=60\text{ mA}$	$f=0.9\text{ GHz}$	16.4	24.1	dB
			$f=2.0\text{ GHz}$		18.6	
OIP3	Output IP3		$f=3.9\text{ GHz}$		13.3	
		$V_{DS}=4\text{V}$, $I_{DS}=60\text{ mA}$	$f=5.8\text{ GHz}$		9.3	
			$f=2.0\text{ GHz}$		18.6	
		$V_{DS}=3\text{V}$, $I_{DS}=60\text{ mA}$	$f=0.9\text{ GHz}$		32	dBm
			$f=2.0\text{ GHz}$		31.4	
P1dB ²	Power output at 1 dB Compression		$f=3.9\text{ GHz}$		31.7	
		$V_{DS}=3\text{V}$, $I_{DS}=60\text{ mA}$	$f=5.8\text{ GHz}$		31.9	
			$f=2.0\text{ GHz}$		33.9	
		$V_{DS}=4\text{V}$, $I_{DS}=60\text{ mA}$	$f=0.9\text{ GHz}$		18.2	dBm
			$f=2.0\text{ GHz}$		18.4	
			$f=3.9\text{ GHz}$		18.6	
			$f=5.8\text{ GHz}$		18.3	
			$f=2.0\text{ GHz}$		20.7	

Absolute Maximum Ratings³

Symbol	Parameter	Max.	Units
$V_{DS}^{(4)}$	Drain-Source Voltage	5	V
$V_{GS}^{(4)}$	Gate-Source Voltage	-5 to 0.7	V
$V_{GD}^{(4)}$	Gate-Drain Voltage	-5 to 0.7	V
$I_{DS}^{(4)}$	Drain Current	120	mA
I_{GS}	Gate Current	2	mA
P_{DISS}	Total Dissipated Power	360	mW
$P_{IN}^{(5)}$	RF Input Power	17	dBm
T_{CH}	Channel Temperature	150	$^{\circ}\text{C}$
T_{OP}	Operating Temperature	-40 to 85	$^{\circ}\text{C}$
T_{STD}	Storage Temperature	-65 to 150	$^{\circ}\text{C}$
Θ_{JC}	Thermal Resistance	160	$^{\circ}\text{C}/\text{W}$

Notes:

2. Drain current bias is allowed to increase during compression measurement.
3. Operation of this device above any one of these parameters may cause permanent damage.
4. Assumes DC quiescent conditions
5. I_{GS} is limited to 2 mA during test.

Characterization Test Circuit

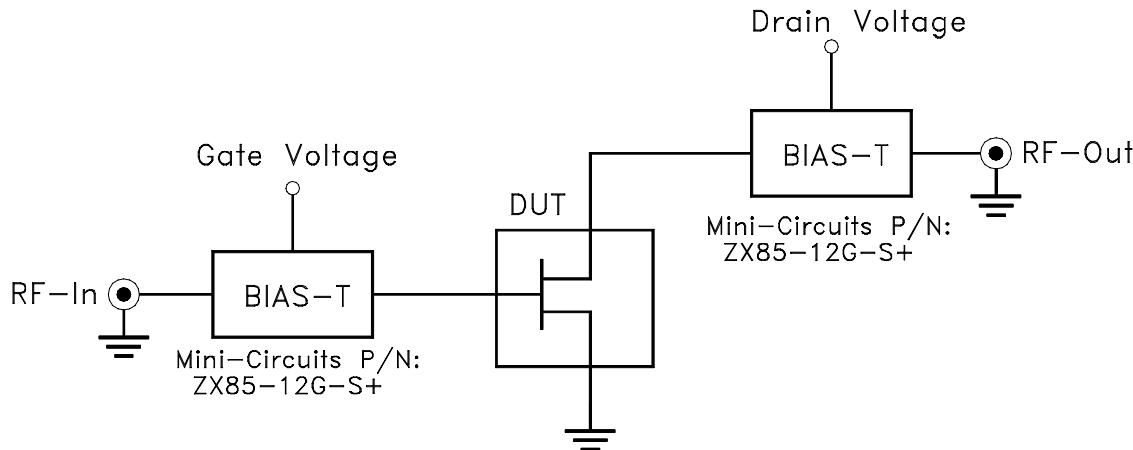
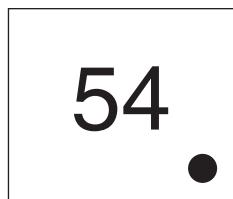


Fig 1. Block Diagram of Test Circuit used for characterization. (DUT soldered on Mini-Circuits Test Board TB-TAV1-541+)
 Gain, Output power at 1dB compression (P1 dB), Noise Figure and output IP3 (OIP3) are measured using Keysight/Agilent Network Analyzer PNA-X.

Conditions:

1. Drain voltage (with reference to source, V_{DS}) = 3 or 4V as shown.
2. Gate Voltage (with reference to source, V_{GS}) is set to obtain desired Drain-Source current (IDS) as shown in specification table.
3. Gain: Pin = -25dBm
4. Output IP3 (OIP3): Two tones, spaced 1 MHz apart, 0 dBm/tone at output.
5. No external matching components used.

Product Marking

Additional Detailed Technical Information

additional information is available on our dash board. To access this information [click here](#)

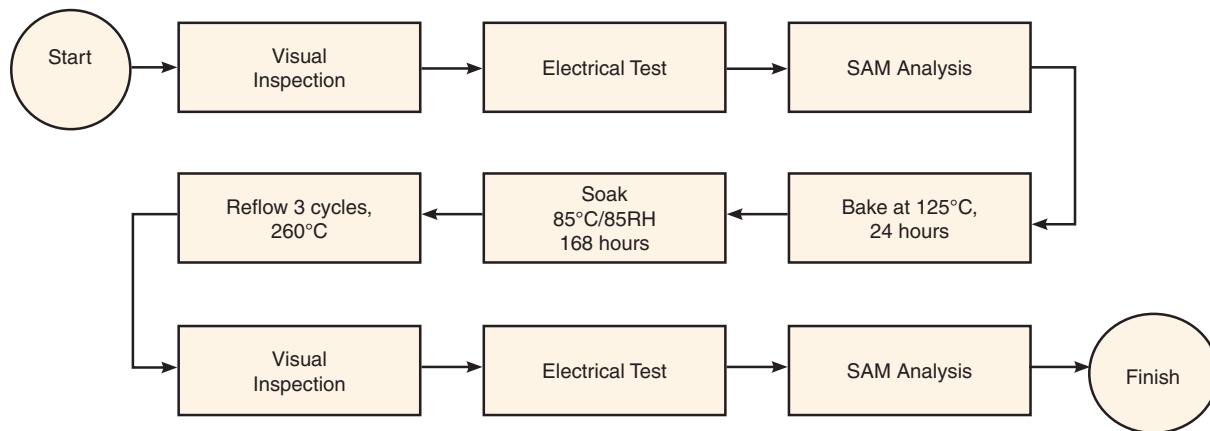
Performance Data	Data Table
	Swept Graphs
	S-Parameter (S2P Files) Data Set (.zip file)
Case Style	TE2769 Plastic package, exposed paddle, lead finish: Matte-Tin plated
Tape & Reel Standard quantities available on reel	F90 7" reels with 20, 50, 100, 200, 500, 1K, 2K or 3K devices
Suggested Layout for PCB Design	98-PL-665
Evaluation Board	TB-TAV1-541+
Environmental Ratings	ENV08T2

ESD Rating

Human Body Model (HBM): Class 1A (250V to <500V) in accordance with ANSI/ESD STM 5.1 - 2001

MSL Rating

Moisture Sensitivity: MSL1 in accordance with IPC/JEDEC J-STD-020D

MSL Test Flow Chart**Additional Notes**

- A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.
- B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.
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