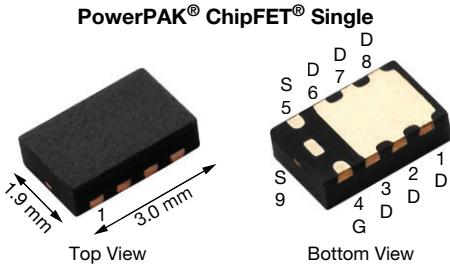


N-Channel 60 V (D-S) MOSFET


Marking code: AA

PRODUCT SUMMARY	
V_{DS} (V)	60
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.034
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.041
Q_g typ. (nC)	10.5
I_D (A) ^a	12
Configuration	Single

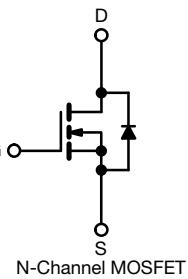
FEATURES

- TrenchFET® power MOSFET
- Thermally enhanced PowerPAK ChipFET package
 - Small footprint area
 - Low on-resistance
 - Thin 0.8 mm profile
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Load switch for portable applications
- DC/DC switch for low power synchronous rectification
- Intermediate switch driver for DC/DC applications



ORDERING INFORMATION

Package	PowerPAK ChipFET
Lead (Pb)-free and halogen-free	Si5476DU-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	60	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current ($T_J = 150$ °C)	$T_C = 25$ °C	12 ^a	A
	$T_C = 70$ °C	12 ^a	
	$T_A = 25$ °C	7 ^{b, c}	
	$T_A = 70$ °C	5.6 ^{b, c}	
Pulsed drain current	I_{DM}	25	A
Continuous source-drain diode current	$T_C = 25$ °C	12 ^a	
	$T_A = 25$ °C	2.6 ^{b, c}	
Avalanche current	I_{AS}	15	mJ
Single pulse avalanche energy	E_{AS}	11.2	
Maximum power dissipation	$T_C = 25$ °C	31	W
	$T_C = 70$ °C	20	
	$T_A = 25$ °C	3.1 ^{b, c}	
	$T_A = 70$ °C	2 ^{b, c}	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^{b, f}	$t \leq 5$ s	R_{thJA}	34	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	3	

Notes

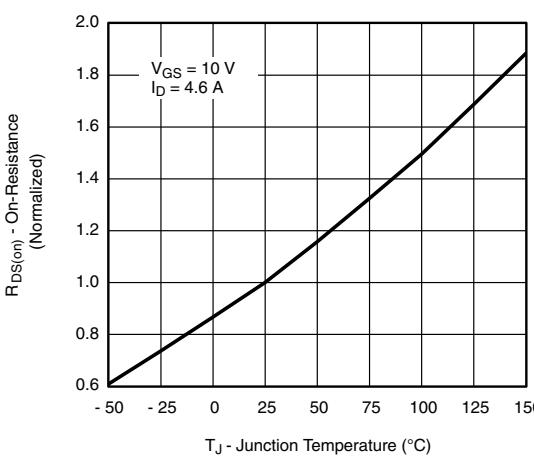
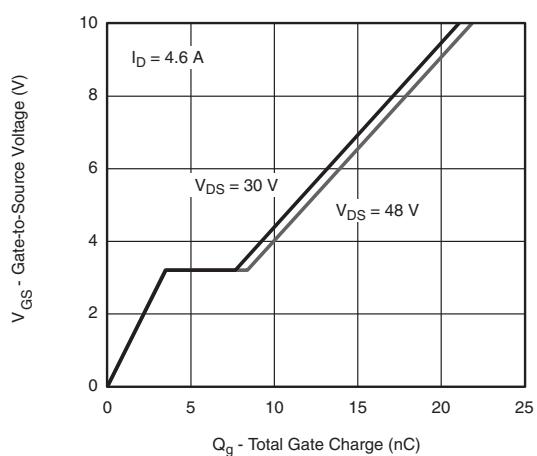
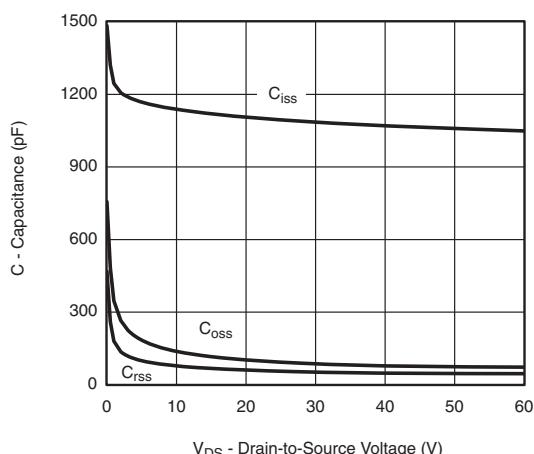
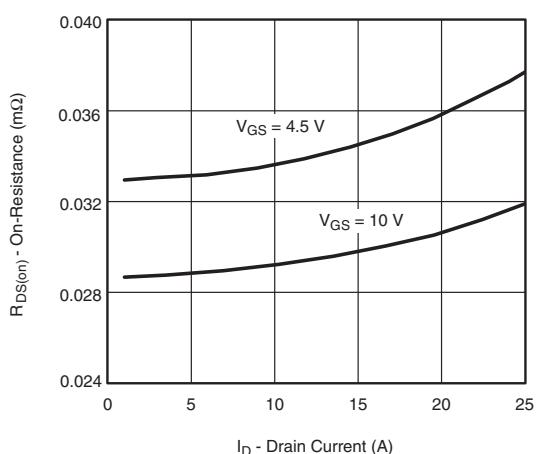
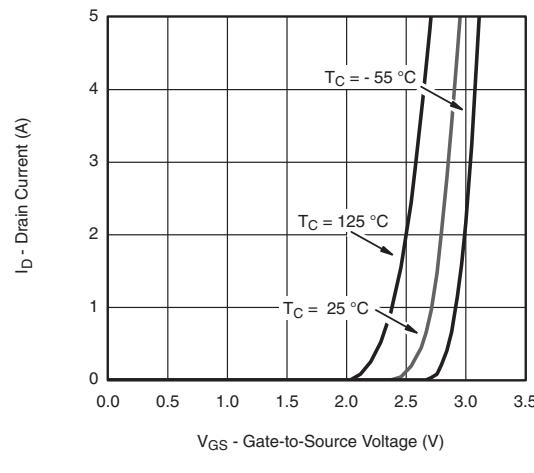
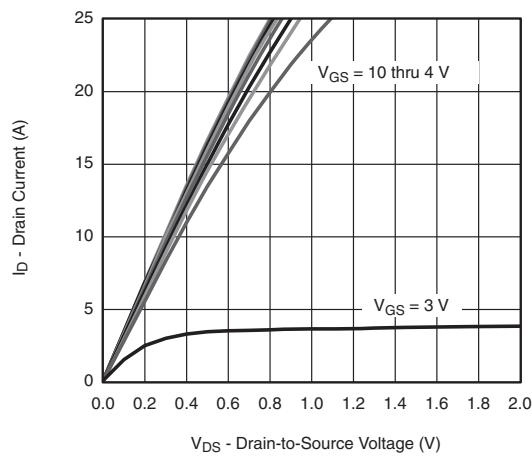
- Package limited
- Surface mounted on 1" x 1" FR4 board
- $t = 5$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 90 °C/W

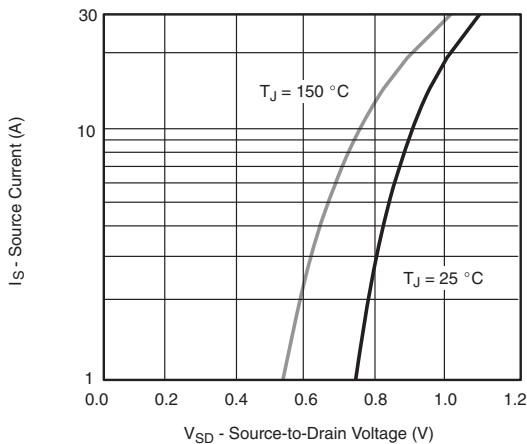
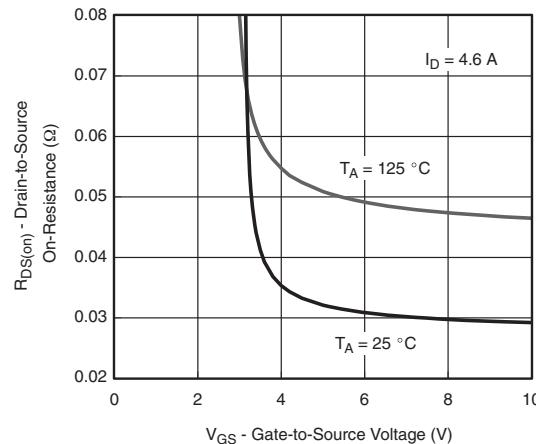
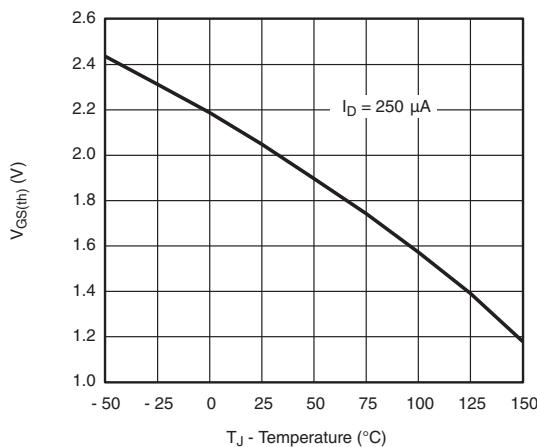
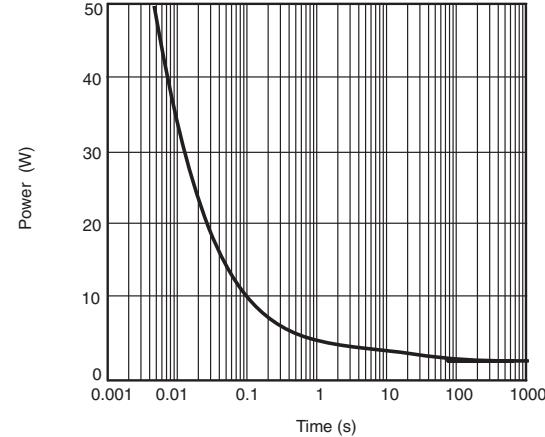
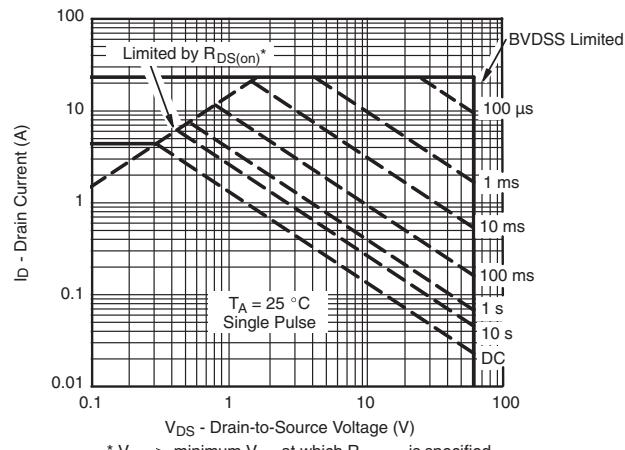
SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = 1 \text{ mA}$	60	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = 250 \mu\text{A}$	-	55	-	$\text{mV}/^\circ\text{C}$
$V_{GS(\text{th})}$ temperature coefficient	$\Delta V_{GS(\text{th})}/T_J$		-	-6.3	-	
Gate-source threshold voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	1	-	3	V
Gate-source leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 60 \text{ V}$, $V_{GS} = 0 \text{ V}$	-	-	1	μA
		$V_{DS} = 60 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 55^\circ\text{C}$	-	-	10	
On-state drain current ^a	$I_{D(\text{on})}$	$V_{DS} \geq 5 \text{ V}$, $V_{GS} = 10 \text{ V}$	25	-	-	A
Drain-source on-state resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}$, $I_D = 4.6 \text{ A}$	-	0.028	0.034	Ω
		$V_{GS} = 4.5 \text{ V}$, $I_D = 4.2 \text{ A}$	-	0.033	0.041	
Forward transconductance ^a	g_{fs}	$V_{DS} = 15 \text{ V}$, $I_D = 4.6 \text{ A}$	-	20	-	S
Dynamic ^b						
Input capacitance	C_{iss}	$V_{DS} = 30 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$	-	1100	-	pF
Output capacitance	C_{oss}		-	90	-	
Reverse transfer capacitance	C_{rss}		-	55	-	
Total gate charge	Q_g	$V_{DS} = 30 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_D = 4.6 \text{ A}$	-	21	32	nC
Gate-source charge	Q_{gs}	$V_{DS} = 30 \text{ V}$, $V_{GS} = 4.5 \text{ V}$, $I_D = 4.6 \text{ A}$	-	10.5	16	
Gate-drain charge	Q_{gd}		-	3.5	-	
Gate resistance	R_g		-	4.2	-	
Turn-on delay time	$t_{d(\text{on})}$	$V_{DD} = 30 \text{ V}$, $R_L = 5.4 \Omega$, $I_D \geq 5.6 \text{ A}$, $V_{GEN} = 4.5 \text{ V}$, $R_g = 1 \Omega$	-	3.3	-	Ω
Rise time	t_r		-	20	30	ns
Turn-off delay time	$t_{d(\text{off})}$		-	150	225	
Fall time	t_f		-	20	30	
Turn-on delay time	$t_{d(\text{on})}$		-	60	90	
Rise time	t_r		-	10	15	
Turn-off delay time	$t_{d(\text{off})}$	$V_{DD} = 30 \text{ V}$, $R_L = 5.4 \Omega$, $I_D \geq 5.6 \text{ A}$, $V_{GEN} = 10 \text{ V}$, $R_g = 1 \Omega$	-	15	25	ns
Fall time	t_f		-	22	40	
			-	10	15	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	$T_C = 25^\circ\text{C}$	-	-	12	A
Pulse diode forward current	I_{SM}		-	-	25	
Body diode voltage	V_{SD}	$I_S = 5.5 \text{ A}$, $V_{GS} = 0 \text{ V}$	-	0.85	1.2	V
Body diode reverse recovery time	t_{rr}	$I_F = 5.5 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $T_J = 25^\circ\text{C}$	-	25	50	ns
Body diode reverse recovery charge	Q_{rr}		-	25	50	nC
Reverse recovery fall time	t_a		-	19	-	ns
Reverse recovery rise time	t_b		-	6	-	

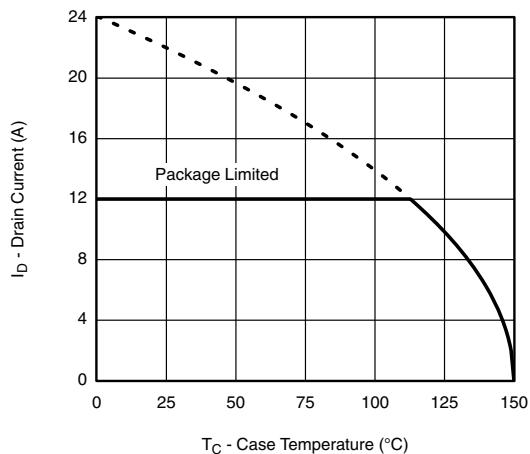
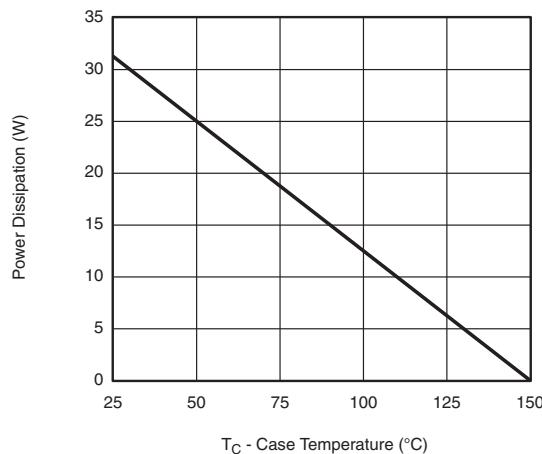
Notes

- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2 \%$
- b. Guaranteed by design, not subject to production testing

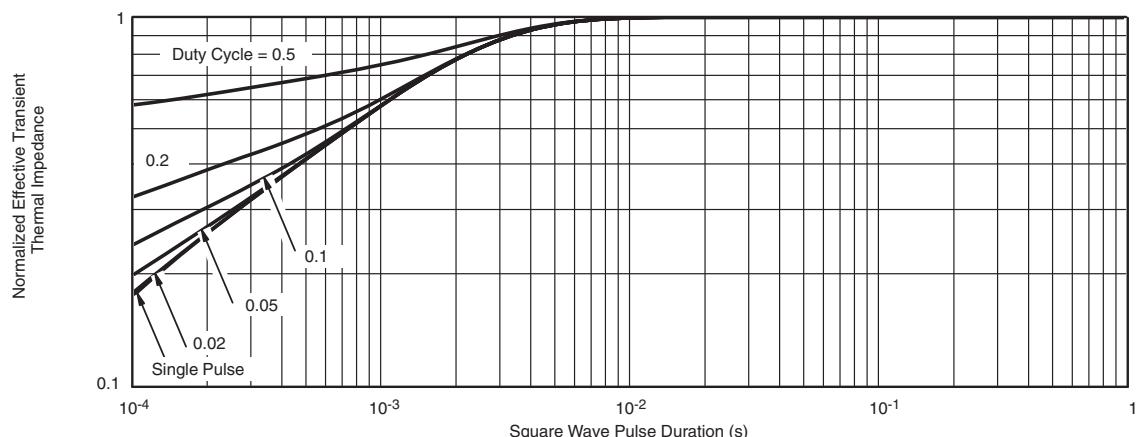
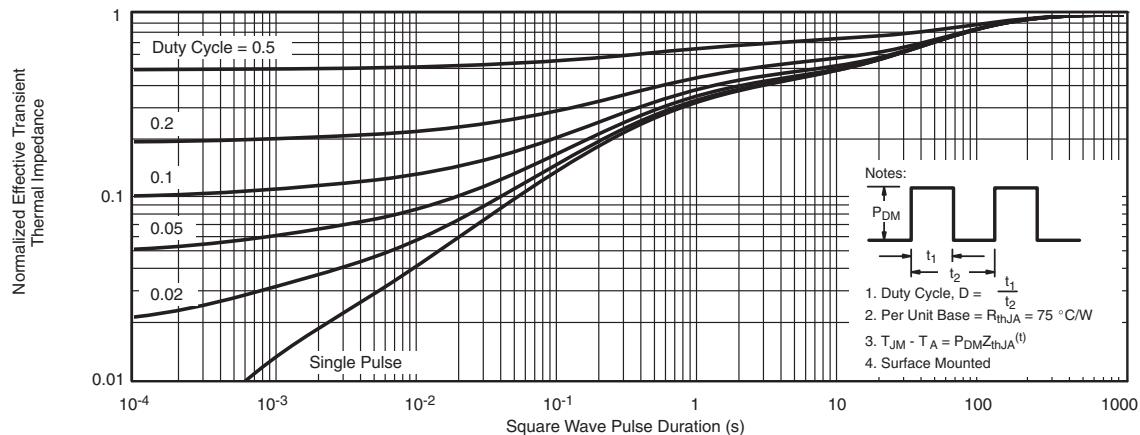
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Single Pulse Power, Junction-to-Ambient

Safe Operating Area, Junction-to-Ambient

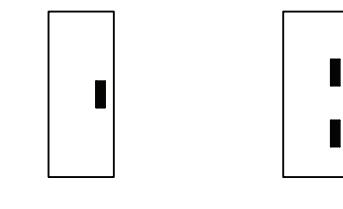
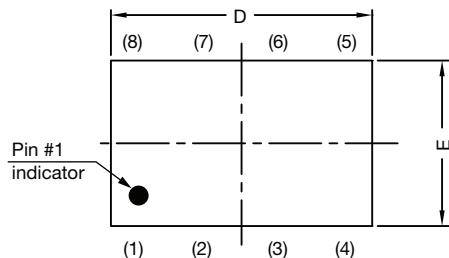
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating ^a

Power Derating
Note

- The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

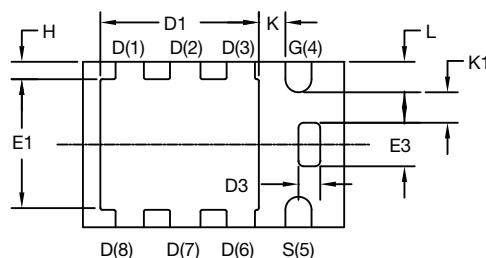
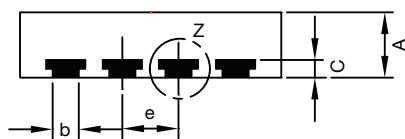
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?73663.

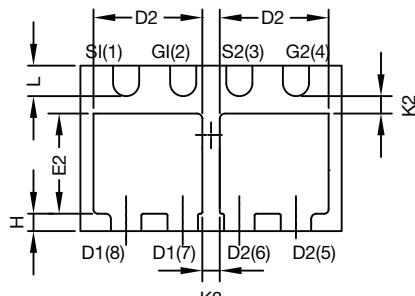
PowerPAK® ChipFET® Case Outline



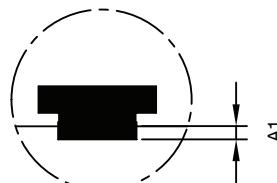
Side view of single Side view of dual



Backside view of single pad



Backside view of dual pad



Detail Z

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.85	0.028	0.030	0.033
A1	0	-	0.05	0	-	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
C	0.15	0.20	0.25	0.006	0.008	0.010
D	2.92	3.00	3.08	0.115	0.118	0.121
D1	1.75	1.87	2.00	0.069	0.074	0.079
D2	1.07	1.20	1.32	0.042	0.047	0.052
D3	0.20	0.25	0.30	0.008	0.010	0.012
E	1.82	1.90	1.98	0.072	0.075	0.078
E1	1.38	1.50	1.63	0.054	0.059	0.064
E2	0.92	1.05	1.17	0.036	0.041	0.046
E3	0.45	0.50	0.55	0.018	0.020	0.022
e	0.65 BSC			0.026 BSC		
H	0.15	0.20	0.25	0.006	0.008	0.010
K	0.25	-	-	0.010	-	-
K1	0.30	-	-	0.012	-	-
K2	0.20	-	-	0.008	-	-
K3	0.20	-	-	0.008	-	-
L	0.30	0.35	0.40	0.012	0.014	0.016

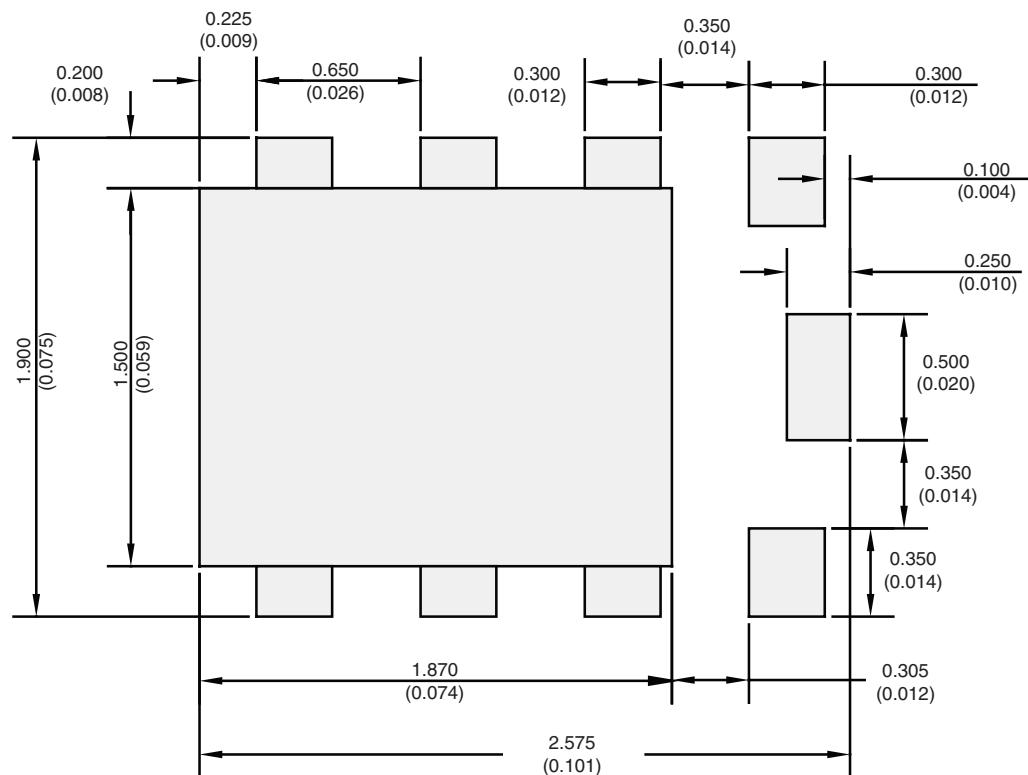
C14-0630-Rev. E, 21-Jul-14

DWG: 5940

Note

- Millimeters will govern

RECOMMENDED MINIMUM PADS FOR PowerPAK® ChipFET® Single



Recommended Minimum Pads Dimensions in mm/(Inches)

[Return to Index](#)

APPLICATION NOTE

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