

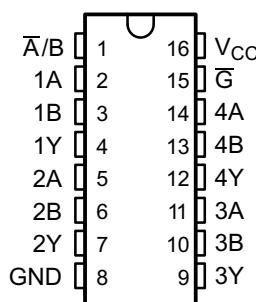
## QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MUXES

Check for Samples: [SN54AHC157](#), [SN74AHC157](#)

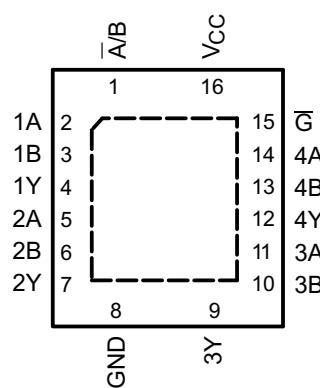
### FEATURES

- Operating Range 2-V to 5.5-V
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

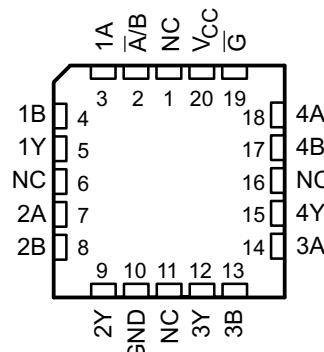
SN54AHC157 . . . J or W PACKAGE  
SN74AHC157 . . . D, DB, DGV, N, NS,  
OR PW PACKAGE  
(TOP VIEW)



SN74AHC157 . . . RGY PACKAGE  
(TOP VIEW)



SN54AHC157 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

### DESCRIPTION

These quadruple 2-line to 1-line data selectors/multiplexers are designed for 2-V to 5.5-V  $V_{CC}$  operation.

The 'AHC157 devices feature a common strobe ( $\bar{G}$ ) input. When the strobe is high, all outputs are low. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The devices provide true data.

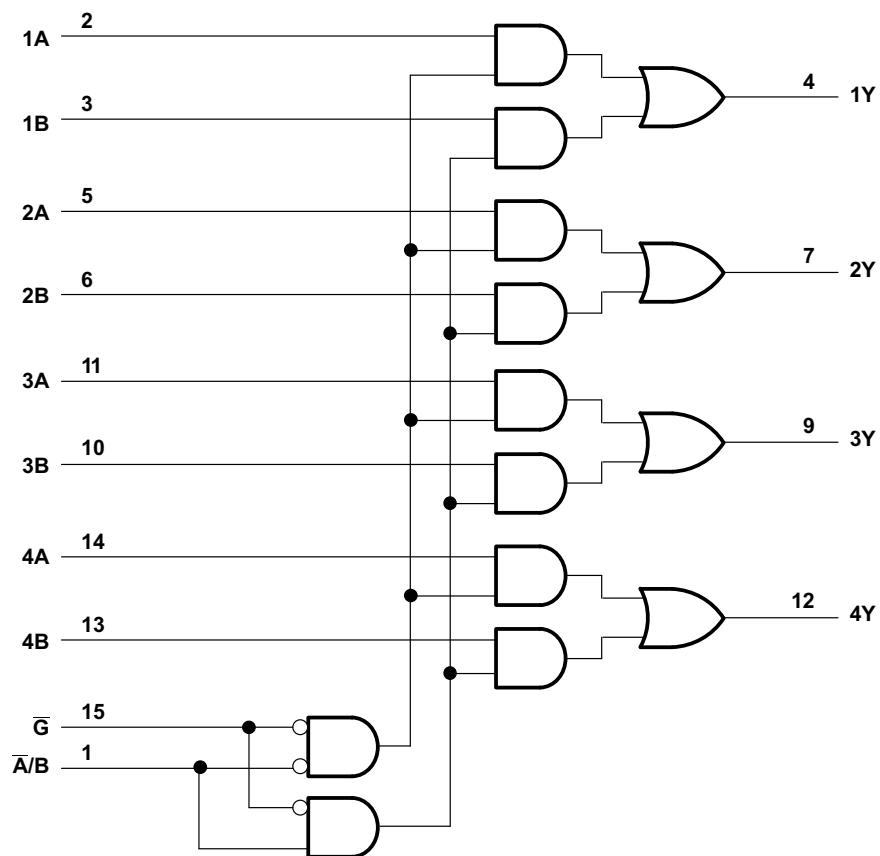
### FUNCTION TABLE

$\bar{G}$	INPUTS			OUTPUT
	$\bar{A}/B$	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, RGY, and W packages.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	VALUE	UNIT
Supply voltage range, $V_{CC}$	–0.5 to 7	V
Input voltage range, $V_I$ <sup>(2)</sup>	–0.5 to 7	V
Output voltage range, $V_O$ <sup>(2)</sup>	–0.5 to $V_{CC} + 0.5$	V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_O > V_{CC}$ )	–20	mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20	mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25	mA
Continuous current through $V_{CC}$ or GND	±50	mA
Package thermal impedance, $\theta_{JA}$	D package <sup>(3)</sup>	73
	DB package <sup>(3)</sup>	82
	DGV package <sup>(3)</sup>	120
	N package <sup>(3)</sup>	67
	NS package <sup>(3)</sup>	64
	PW package <sup>(3)</sup>	108
	RGY package <sup>(4)</sup>	39
Storage temperature range, $T_{stg}$	–65 to 150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.
- (4) The package thermal impedance is calculated in accordance with JESD 51-5.

## RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

		SN54AHC157		SN74AHC157		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2	5.5	2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5	1.5		V
		$V_{CC} = 3$ V	2.1	2.1		
		$V_{CC} = 5.5$ V	3.85	3.85		
$V_{IL}$	Low-level Input voltage	$V_{CC} = 2$ V	0.5	0.5		V
		$V_{CC} = 3$ V	0.9	0.9		
		$V_{CC} = 5.5$ V	1.65	1.65		
$V_I$	Input voltage	0	5.5	0	5.5	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2$ V	–50	–50		mA
		$V_{CC} = 3.3$ V ± 0.3 V	–4	–4		
		$V_{CC} = 5$ V ± 0.5 V	–8	–8		
$I_{OL}$	Low-level output current	$V_{CC} = 2$ V	50	50		mA
		$V_{CC} = 3.3$ V ± 0.3 V	4	4		
		$V_{CC} = 5$ V ± 0.5 V	8	8		
$\Delta t/\Delta v$	Input Transition rise or fall rate	$V_{CC} = 3.3$ V ± 0.3 V	100	100		ns/V
		$V_{CC} = 5$ V ± 0.5 V	20	20		
$T_A$	Operating free-air temperature	–55	125	–40	125	°C

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

## ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C	T <sub>A</sub> = -55°C TO 125°C		T <sub>A</sub> = -40°C TO 85°C		T <sub>A</sub> = -40°C TO 125°C		UNIT	
				SN54AHC157		SN74AHC157		SN74AHC157			
				MIN	TYP	MAX	MIN	MAX	MIN		
V <sub>OH</sub>	I <sub>OH</sub> = -50 µA	2 V	1.9	2		1.9		1.9		V	
		3 V	2.9	3		2.9		2.9			
		4.5 V	4.4	4.5		4.4		4.4			
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		2.48			
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	2 V		0.1		0.1		0.1		V	
		3 V		0.1		0.1		0.1			
		4.5 V		0.1		0.1		0.1			
	I <sub>OH</sub> = 4 mA	3 V		0.36		0.5		0.44			
	I <sub>OH</sub> = 8 mA	4.5 V		0.36		0.5		0.44			
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V		±0.1		±1 <sup>(1)</sup>		±1		±1 µA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		4		40		40		40 µA	
C <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2	10			10		pF	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C	T <sub>A</sub> = -55°C TO 125°C		T <sub>A</sub> = -40°C TO 85°C		T <sub>A</sub> = -40°C TO 125°C		UNIT	
					SN54AHC157		SN74AHC157		SN74AHC157			
					TYP	MAX	MIN	MAX	MIN	MAX		
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 15 pF	6.2 <sup>(1)</sup>	9.7 <sup>(1)</sup>	1 <sup>(1)</sup>	11.5 <sup>(1)</sup>	1	11.5	1	11.5	ns
				6.2 <sup>(1)</sup>	9.7 <sup>(1)</sup>	1 <sup>(1)</sup>	11.5 <sup>(1)</sup>	1	11.5	1	11.5	
t <sub>PLH</sub>	Ā/B̄	Y	C <sub>L</sub> = 15 pF	8.4 <sup>(1)</sup>	13.2 <sup>(1)</sup>	1 <sup>(1)</sup>	15.5 <sup>(1)</sup>	1	15.5	1	15.5	ns
				8.4 <sup>(1)</sup>	13.2 <sup>(1)</sup>	1 <sup>(1)</sup>	15.5 <sup>(1)</sup>	1	15.5	1	15.5	
t <sub>PLH</sub>	Ḡ	Y	C <sub>L</sub> = 15 pF	8.7 <sup>(1)</sup>	13.6 <sup>(1)</sup>	1 <sup>(1)</sup>	16 <sup>(1)</sup>	1	16	1	16	ns
				8.7 <sup>(1)</sup>	13.6 <sup>(1)</sup>	1 <sup>(1)</sup>	16 <sup>(1)</sup>	1	16	1	16	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 50 pF	8.7	13.2	1	15	1	15	1	15	ns
				8.7	13.2	1	15	1	15	1	15	
t <sub>PLH</sub>	Ā/B̄	Y	C <sub>L</sub> = 50 pF	10.9	16.7	1	19	1	19	1	19	ns
				10.9	16.7	1	19	1	19	1	19	
t <sub>PLH</sub>	Ḡ	Y	C <sub>L</sub> = 50 pF	11.2	17.1	1	19.5	1	19.5	1	19.5	ns
				11.2	17.1	1	19.5	1	19.5	1	19.5	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$	$T_A = -55^\circ\text{C} \text{ TO } 125^\circ\text{C}$	$T_A = -40^\circ\text{C} \text{ TO } 85^\circ\text{C}$	$T_A = -40^\circ\text{C} \text{ TO } 125^\circ\text{C}$	UNIT	
					Recommended				
					TYP	MAX	MIN		
$t_{PLH}$	A or B	Y	$C_L = 15 \text{ pF}$	4.1 <sup>(1)</sup>	6.4 <sup>(1)</sup>	1 <sup>(1)</sup>	7.5 <sup>(1)</sup>	1	7.5
$t_{PHL}$				4.1 <sup>(1)</sup>	6.4 <sup>(1)</sup>	1 <sup>(1)</sup>	7.5 <sup>(1)</sup>	1	7.5
$t_{PLH}$	$\overline{A}/\overline{B}$	Y	$C_L = 15 \text{ pF}$	5.3 <sup>(1)</sup>	8.1 <sup>(1)</sup>	1 <sup>(1)</sup>	9.5 <sup>(1)</sup>	1	9.5
$t_{PHL}$				5.3 <sup>(1)</sup>	8.1 <sup>(1)</sup>	1 <sup>(1)</sup>	9.5 <sup>(1)</sup>	1	9.5
$t_{PLH}$	$\overline{G}$	Y	$C_L = 15 \text{ pF}$	5.6 <sup>(1)</sup>	8.6 <sup>(1)</sup>	1 <sup>(1)</sup>	10 <sup>(1)</sup>	1	10
$t_{PHL}$				5.6 <sup>(1)</sup>	8.6 <sup>(1)</sup>	1 <sup>(1)</sup>	10 <sup>(1)</sup>	1	10
$t_{PLH}$	A or B	Y	$C_L = 50 \text{ pF}$	5.6 <sup>(1)</sup>	8.4 <sup>(1)</sup>	1 <sup>(1)</sup>	9.5 <sup>(1)</sup>	1	9.5
$t_{PHL}$				5.6 <sup>(1)</sup>	8.4 <sup>(1)</sup>	1 <sup>(1)</sup>	9.5 <sup>(1)</sup>	1	9.5
$t_{PLH}$	$\overline{A}/\overline{B}$	Y	$C_L = 50 \text{ pF}$	6.8 <sup>(1)</sup>	10.1 <sup>(1)</sup>	1 <sup>(1)</sup>	11.5 <sup>(1)</sup>	1	11.5
$t_{PHL}$				6.8 <sup>(1)</sup>	10.1 <sup>(1)</sup>	1 <sup>(1)</sup>	11.5 <sup>(1)</sup>	1	11.5
$t_{PLH}$	$\overline{G}$	Y	$C_L = 50 \text{ pF}$	7.1 <sup>(1)</sup>	10.6 <sup>(1)</sup>	1 <sup>(1)</sup>	12 <sup>(1)</sup>	1	12
$t_{PHL}$				7.1 <sup>(1)</sup>	10.6 <sup>(1)</sup>	1 <sup>(1)</sup>	12 <sup>(1)</sup>	1	12

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## NOISE CHARACTERISTICS

$V_{CC} = 5 \text{ V}$ ,  $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}^{(1)}$

PARAMETER	SN74AHC157			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$			0.8
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$			-0.8
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$			4.8
$V_{IH(D)}$	High-level dynamic input voltage			3.5
$V_{IL(D)}$	Low-level dynamic input voltage			1.5

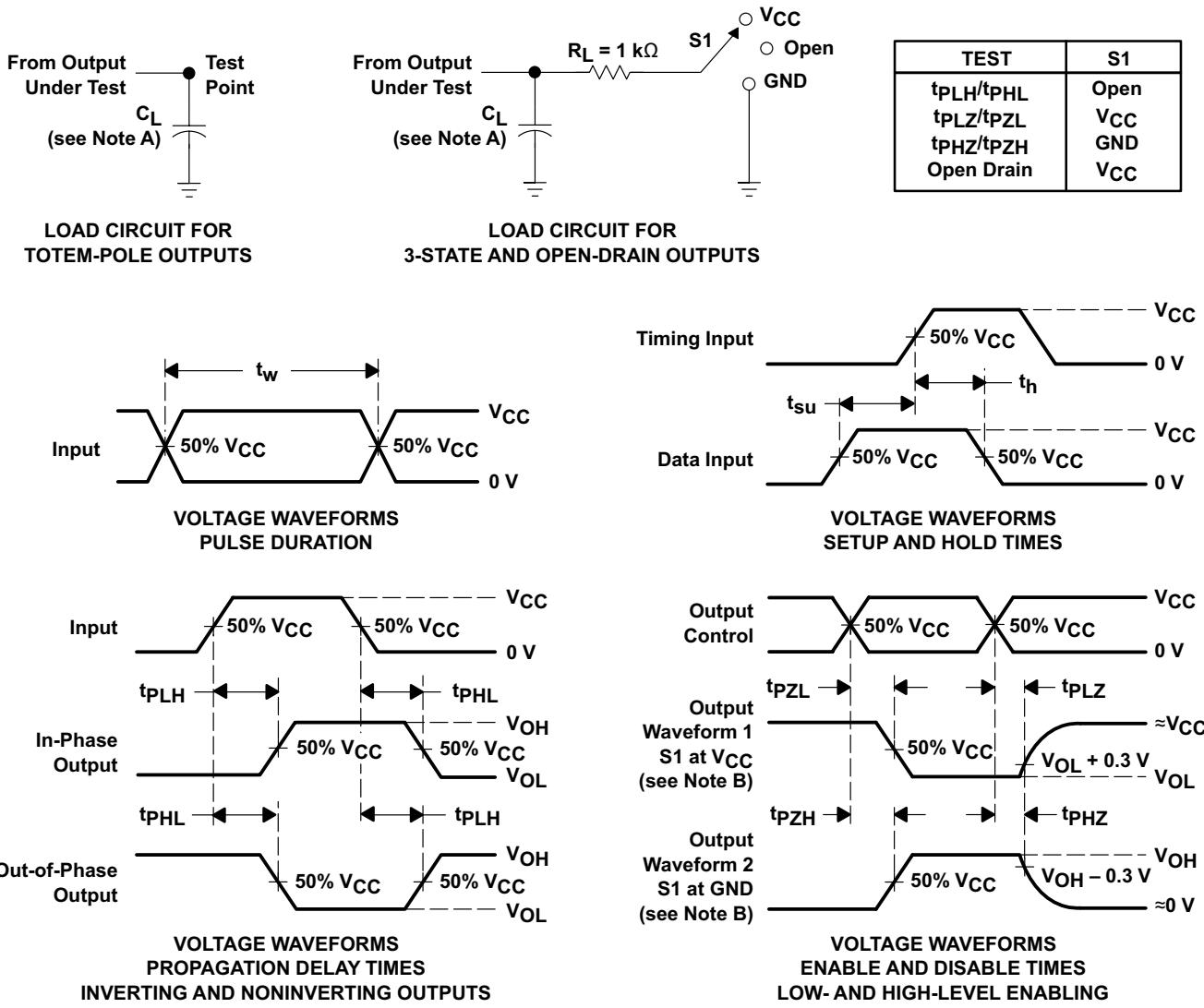
(1) Characteristics are for surface-mount packages only.

## OPERATING CHARACTERISTICS

$V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance No load, $f = 1 \text{ MHz}$	11	pF

## PARAMETER MEASUREMENT INFORMATION



A.  $C_L$  includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 3 \text{ ns}$ ,  $t_f \leq 3 \text{ ns}$ .

D. The outputs are measured one at a time with one input transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## REVISION HISTORY

<b>Changes from Revision I (May 1996) to Revision J</b>	<b>Page</b>
• Changed document format from Quicksilver to DocZone. ....	1
• Extended operating temperature range to 125°C ....	3

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9764201Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9764201Q2A SNJ54AHC 157FK	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
5962-9764201QEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9764201QE A SNJ54AHC157J	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
5962-9764201QFA	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9764201QF A SNJ54AHC157W	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC157D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC157	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC157DBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA157	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC157DGVR	ACTIVE	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA157	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC157DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC157	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC157DRG4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC157	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC157N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHC157N	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC157NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC157	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC157PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA157	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC157PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA157	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC157PWRG3	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	HA157	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC157RGYR	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HA157	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54AHC157FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9764201Q2A SNJ54AHC 157FK	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54AHC157J	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9764201QE A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										SNJ54AHC157J	
SNJ54AHC157W	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9764201QF A SNJ54AHC157W	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

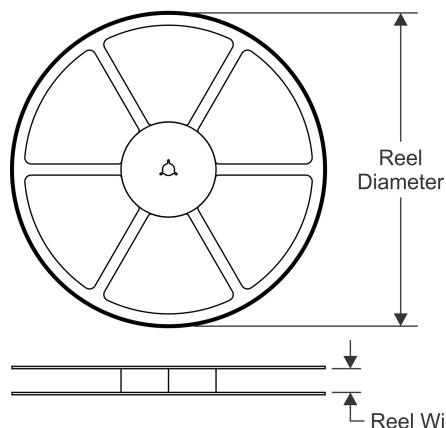
**OTHER QUALIFIED VERSIONS OF SN54AHC157, SN74AHC157 :**

- Catalog : [SN74AHC157](#)

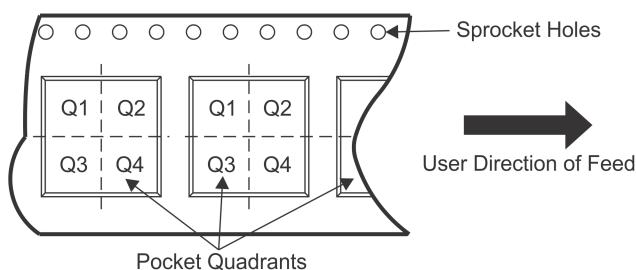
- Military : [SN54AHC157](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


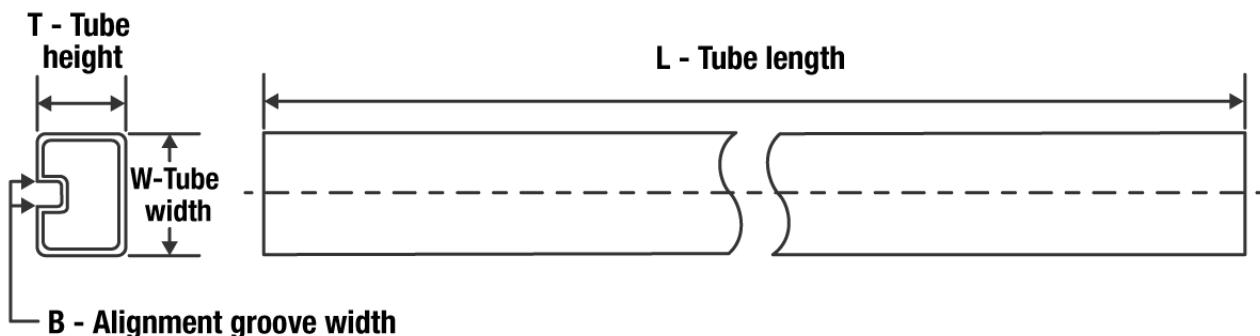
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC157DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC157DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC157DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHC157NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHC157PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC157PWRG3	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC157RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC157DBR	SSOP	DB	16	2000	853.0	449.0	35.0
SN74AHC157DGVR	TVSOP	DGV	16	2000	853.0	449.0	35.0
SN74AHC157DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74AHC157NSR	SO	NS	16	2000	853.0	449.0	35.0
SN74AHC157PWR	TSSOP	PW	16	2000	853.0	449.0	35.0
SN74AHC157PWRG3	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74AHC157RGYR	VQFN	RGY	16	3000	853.0	449.0	35.0

**TUBE**


\*All dimensions are nominal

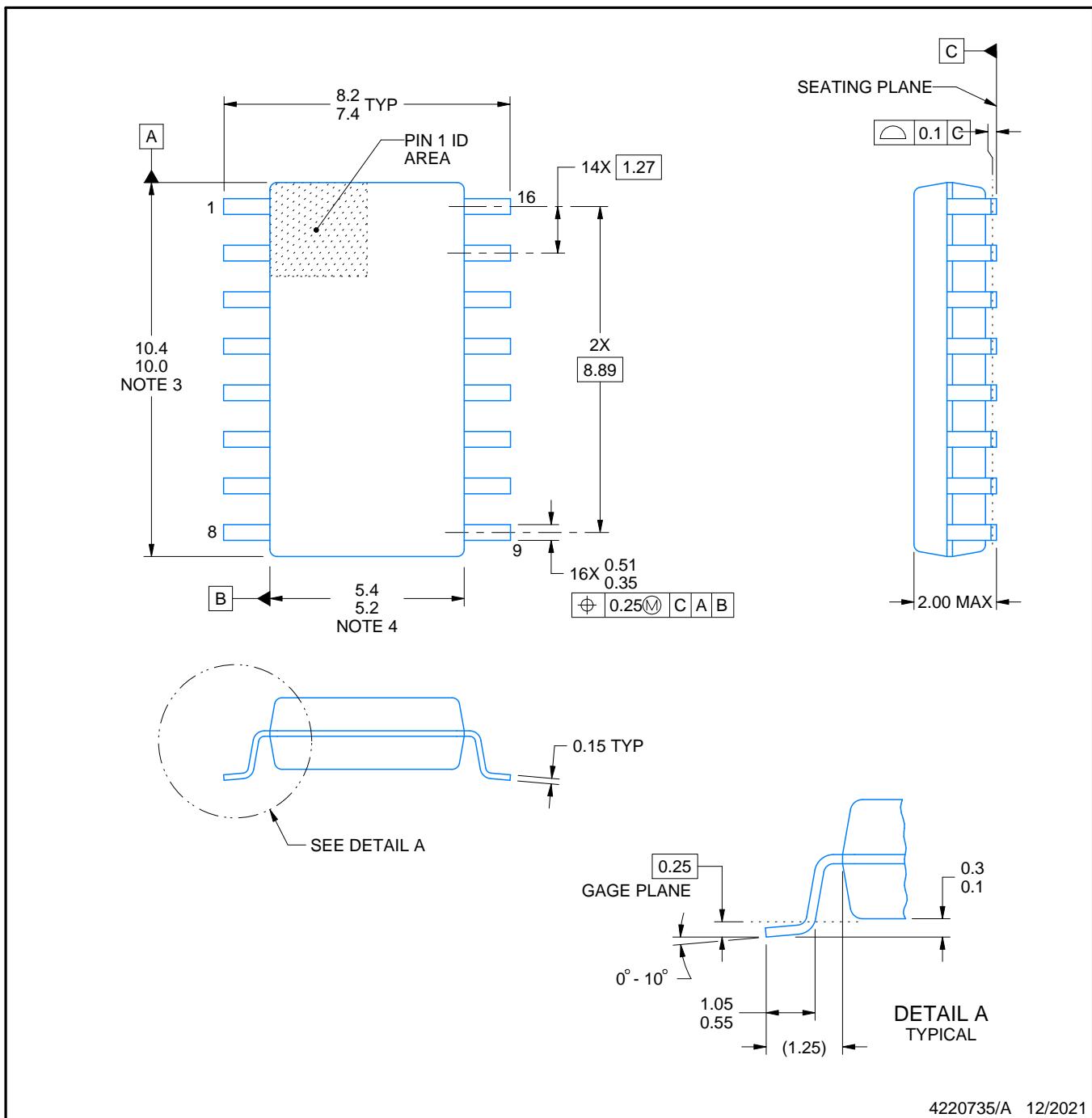
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9764201Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
SN74AHC157D	D	SOIC	16	40	507	8	3940	4.32
SN74AHC157N	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHC157N	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHC157PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SNJ54AHC157FK	FK	LCCC	20	1	506.98	12.06	2030	NA



## PACKAGE OUTLINE

**SOP - 2.00 mm max height**

SOP



## NOTES:

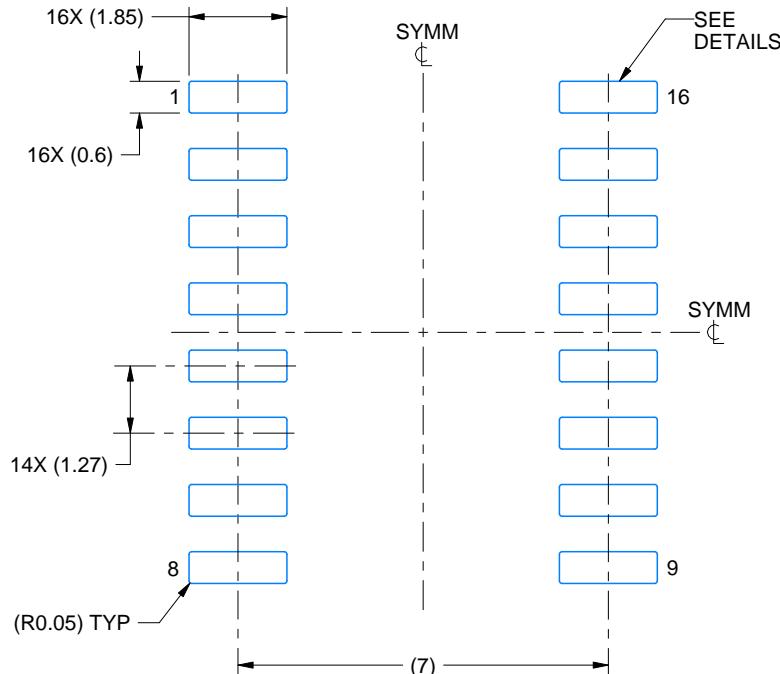
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

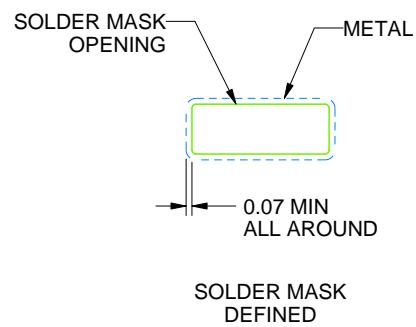
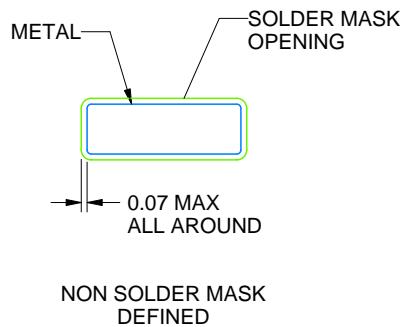
NS0016A

SOP - 2.00 mm max height

SOP



LAND PATTERN EXAMPLE  
SCALE:7X



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

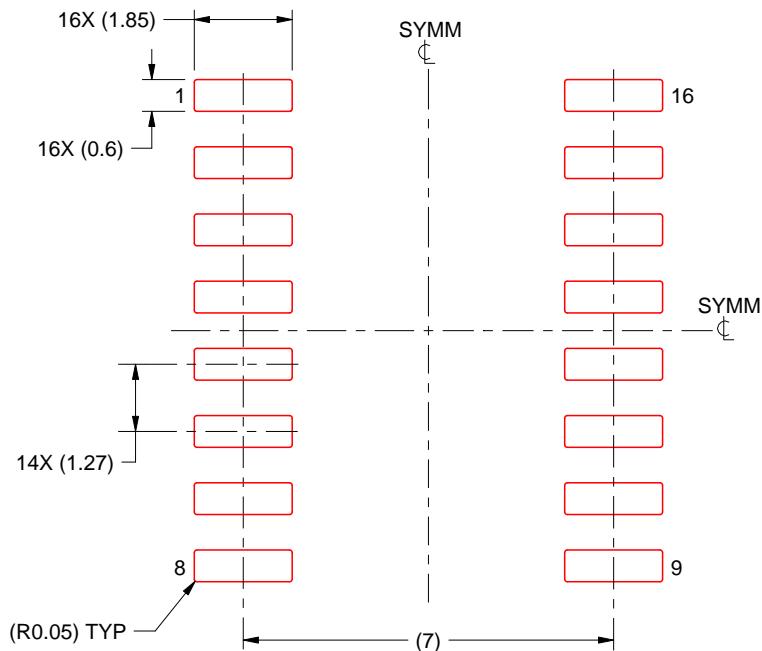
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220735/A 12/2021

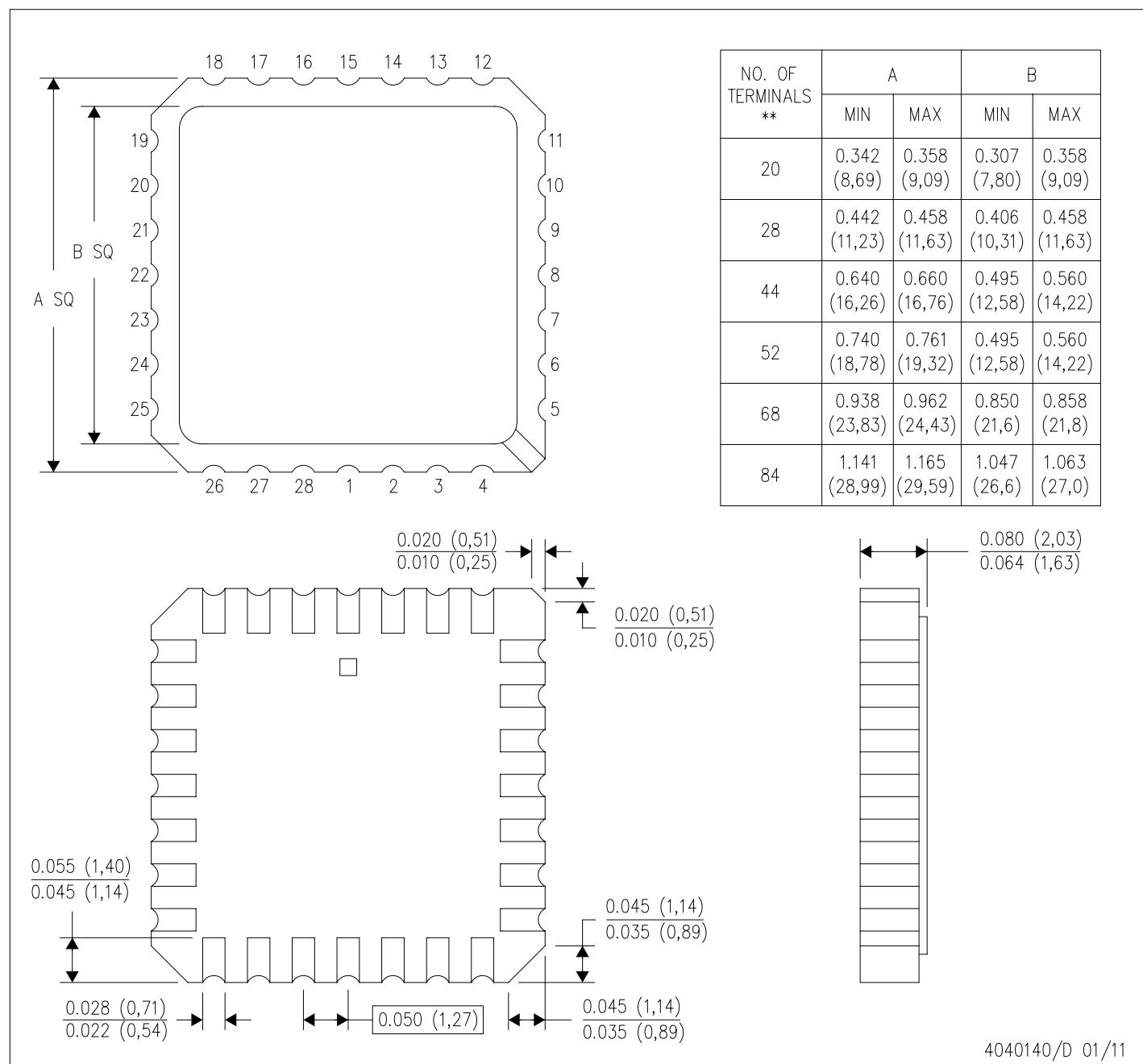
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

FK (S-CQCC-N\*\*)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



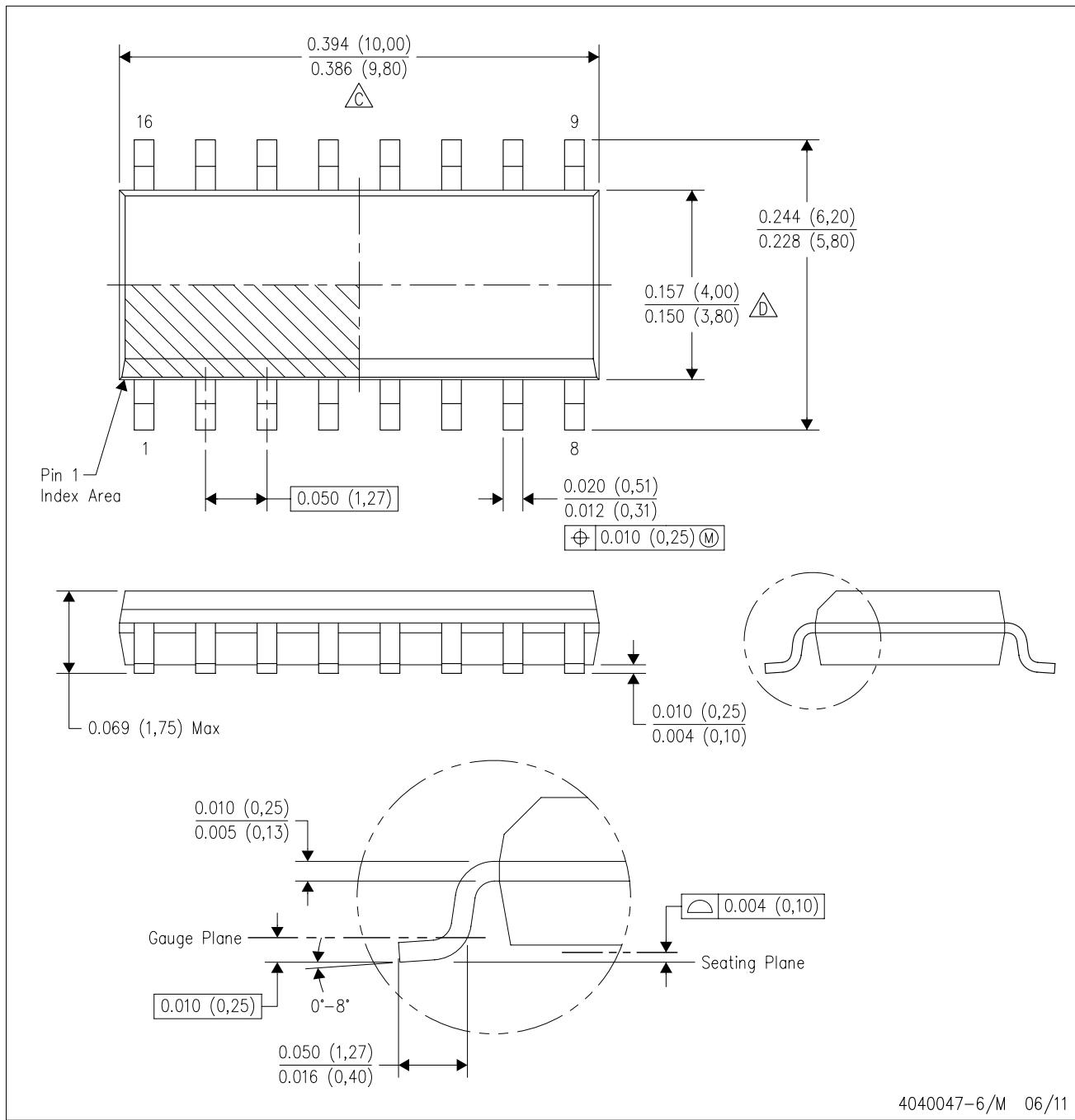
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

4040140/D 01/11

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

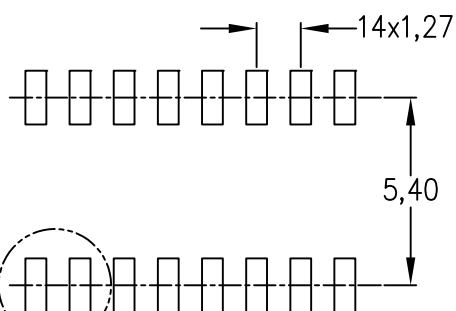
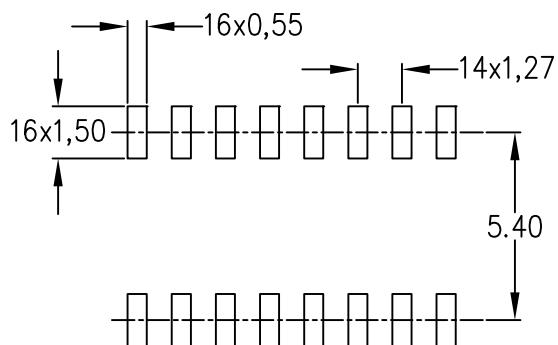
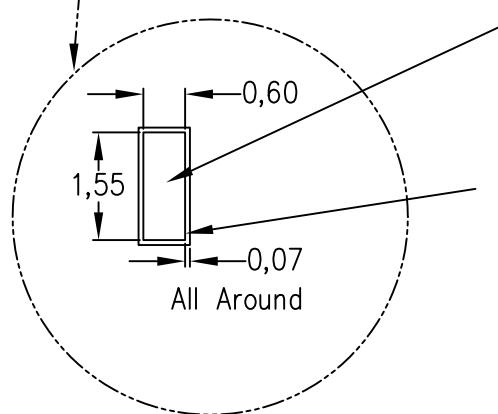
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)Example  
Non Soldermask Defined PadExample  
Pad Geometry  
(See Note C)Example  
Solder Mask Opening  
(See Note E)

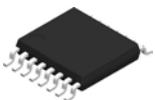
4211283-4/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

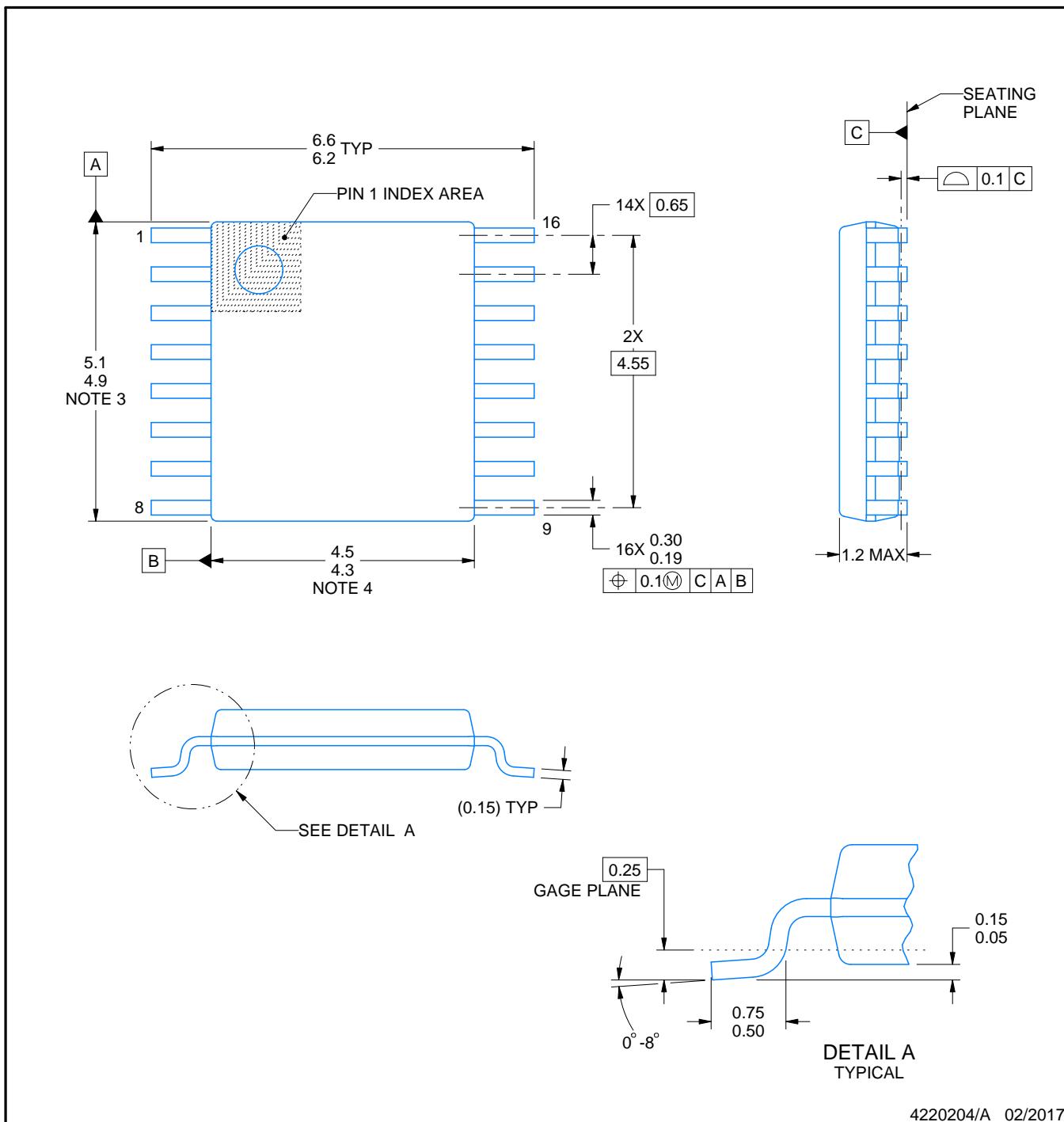
# PACKAGE OUTLINE

PW0016A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



## NOTES:

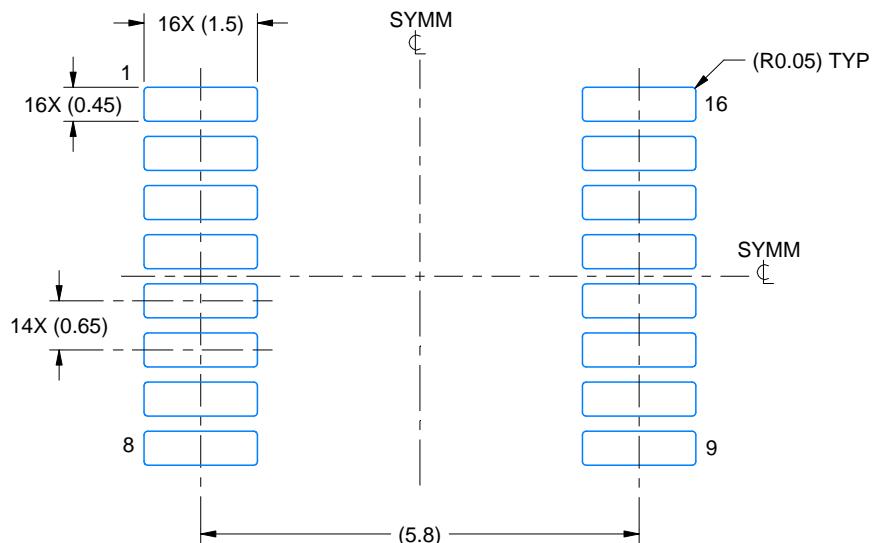
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

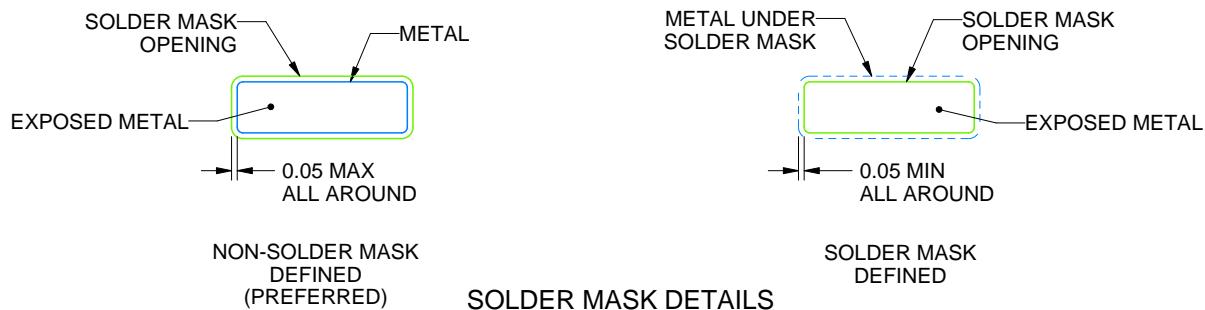
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

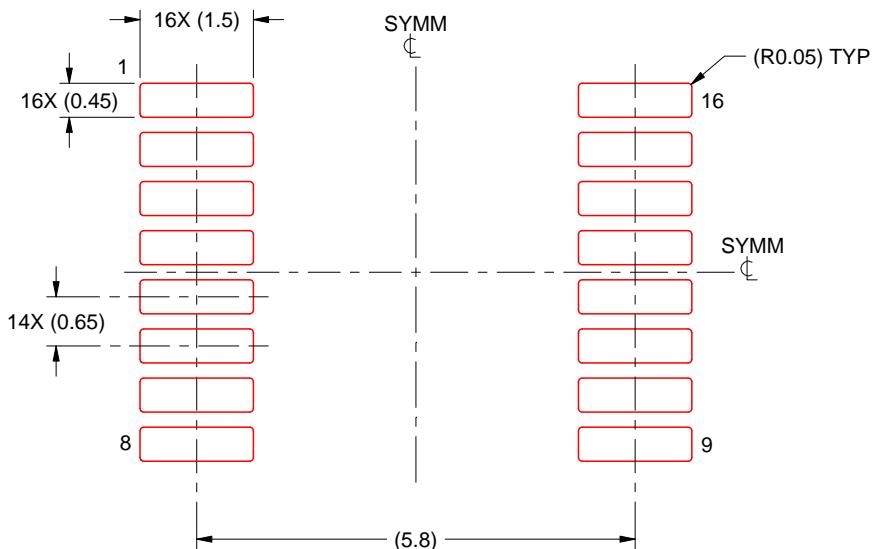
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

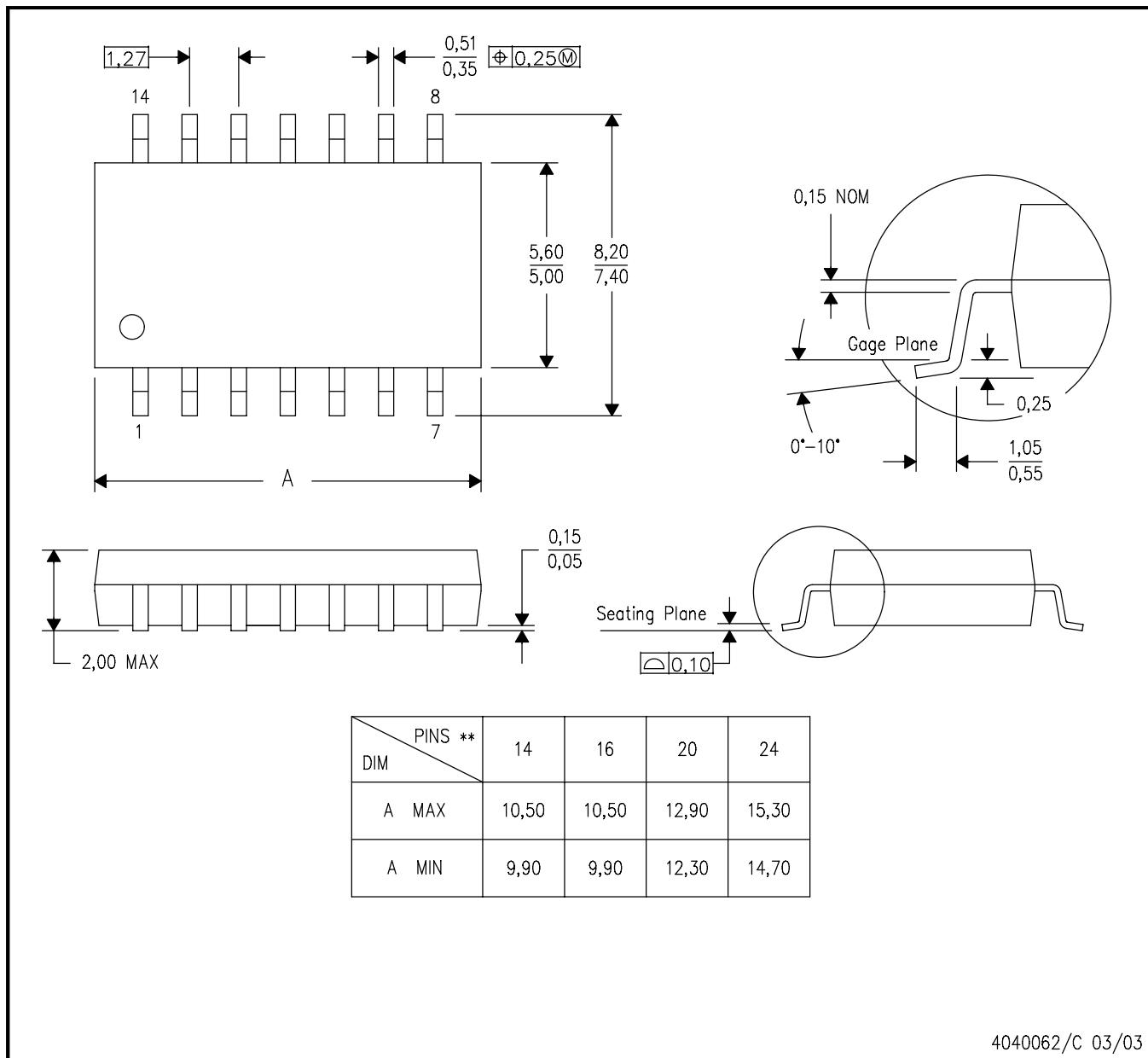
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

## PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**



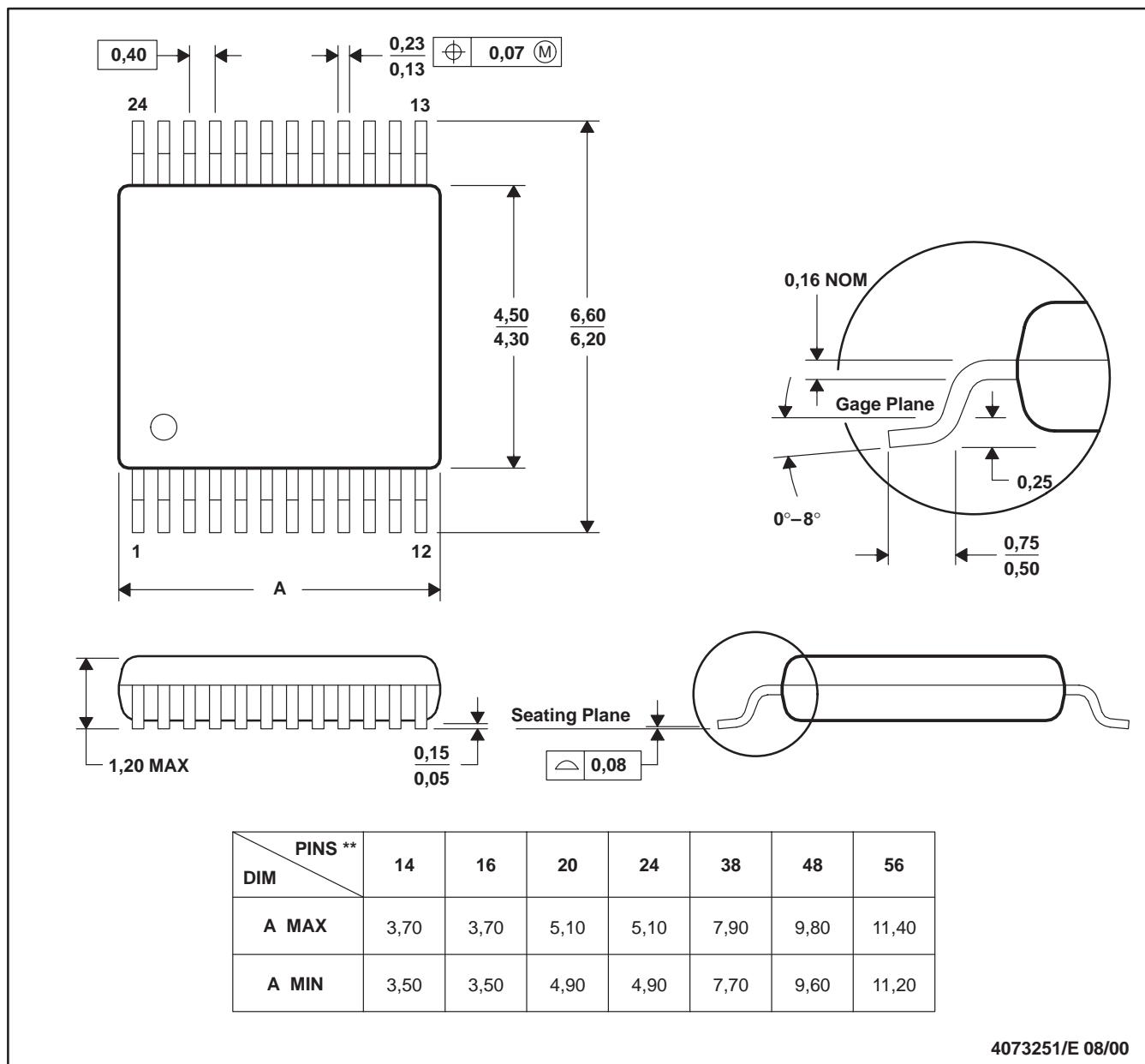
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

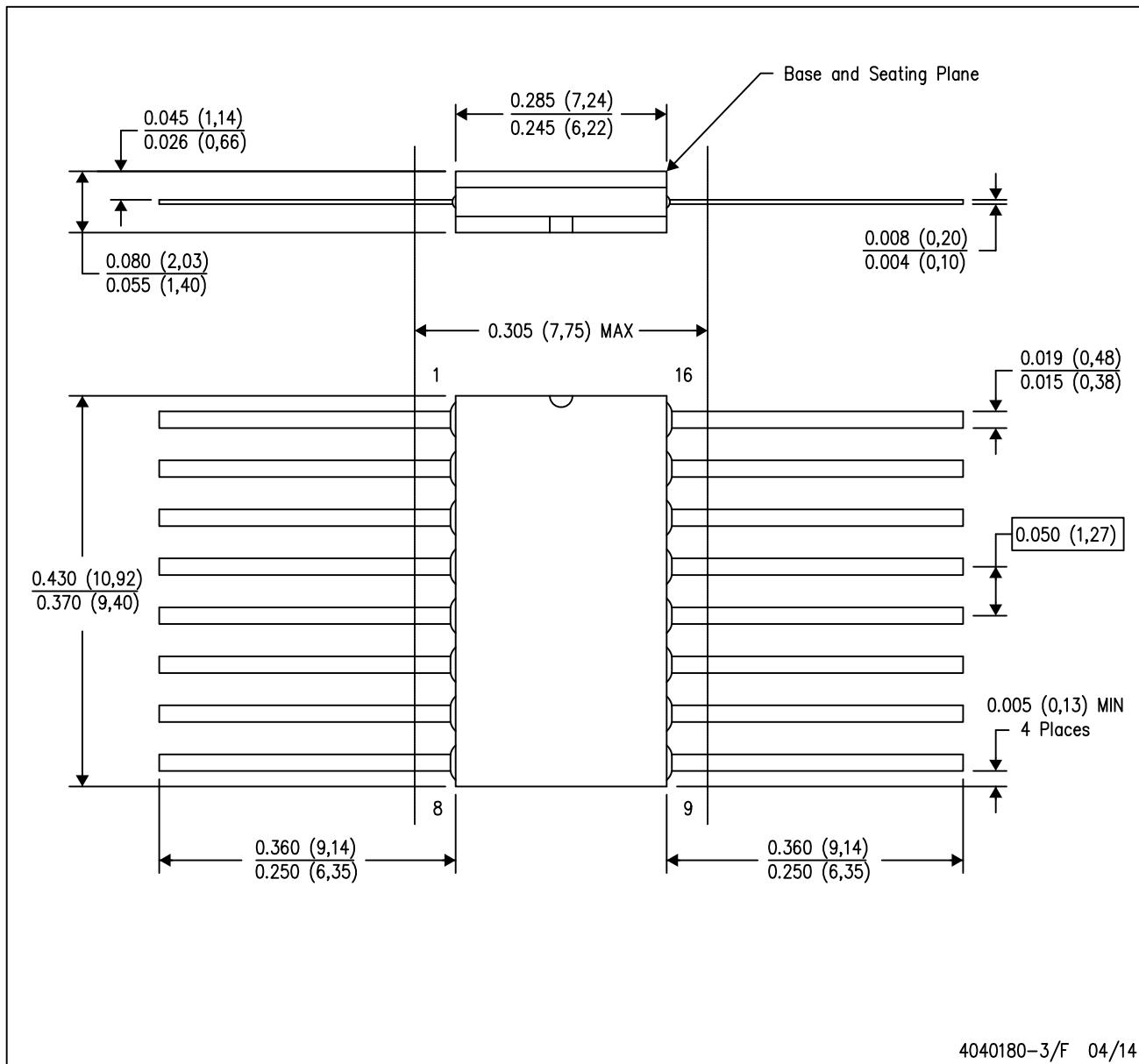
24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



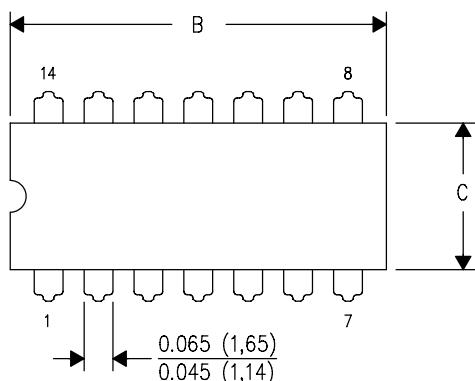
NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- This package can be hermetically sealed with a ceramic lid using glass frit.
- Index point is provided on cap for terminal identification only.
- Falls within MIL-STD 1835 GDFP2-F16

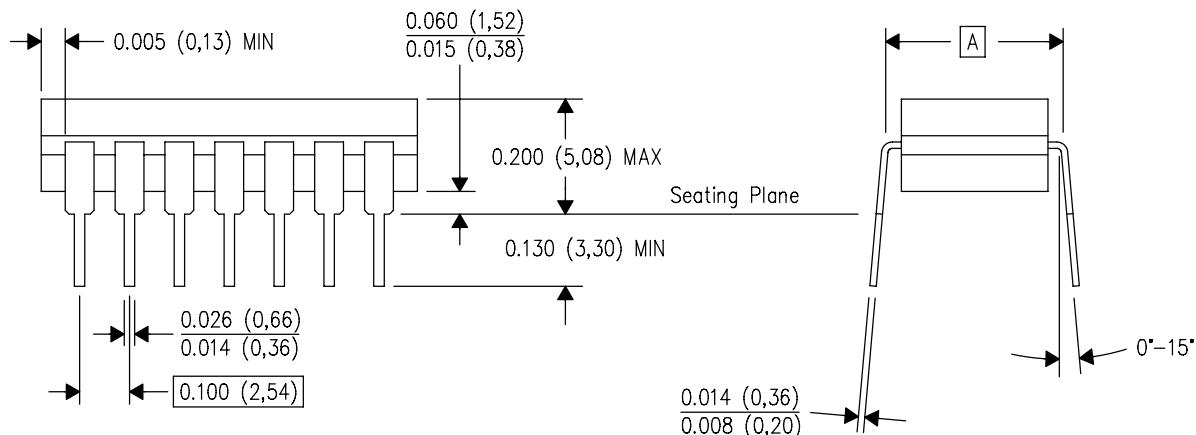
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



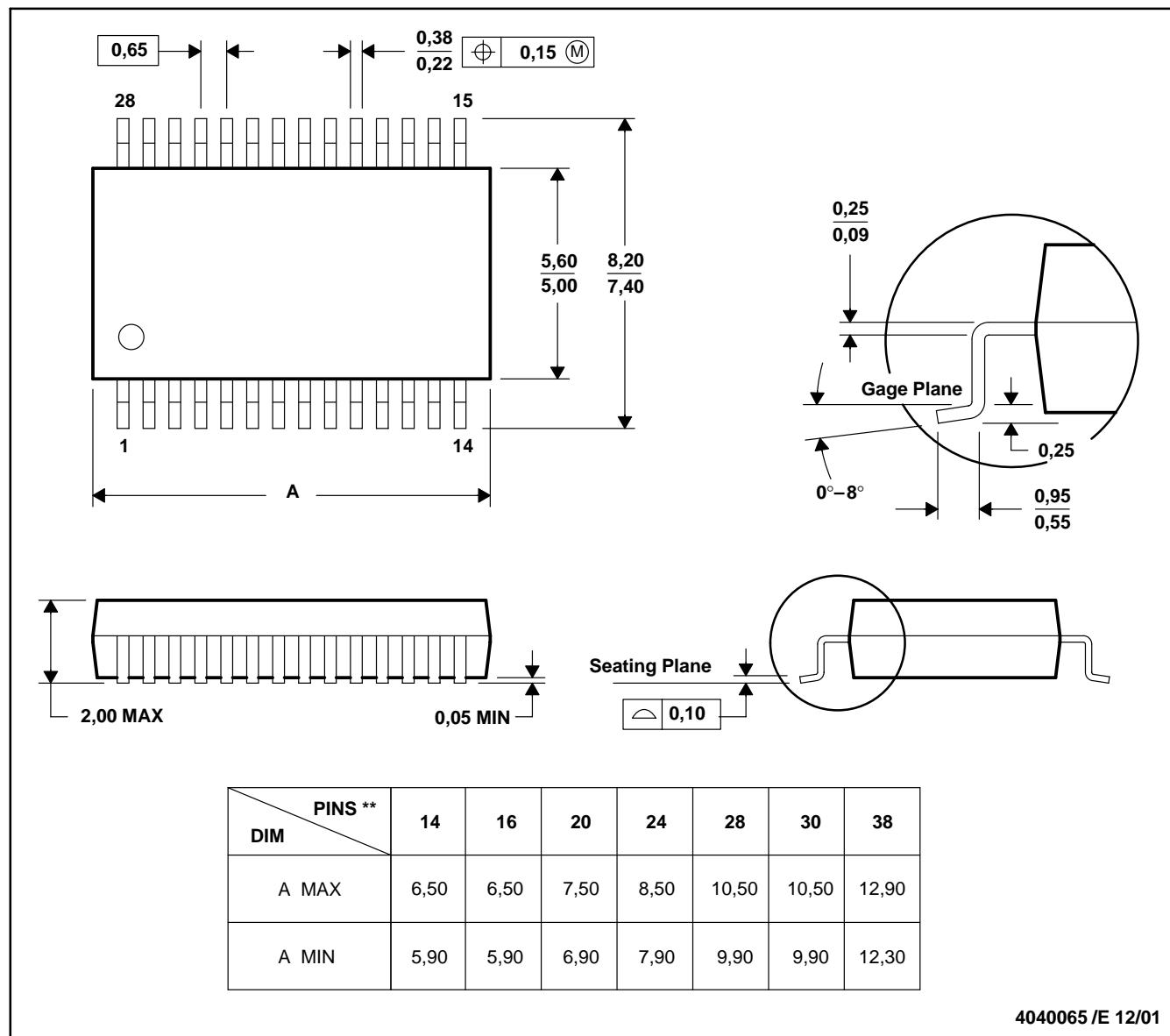
4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN

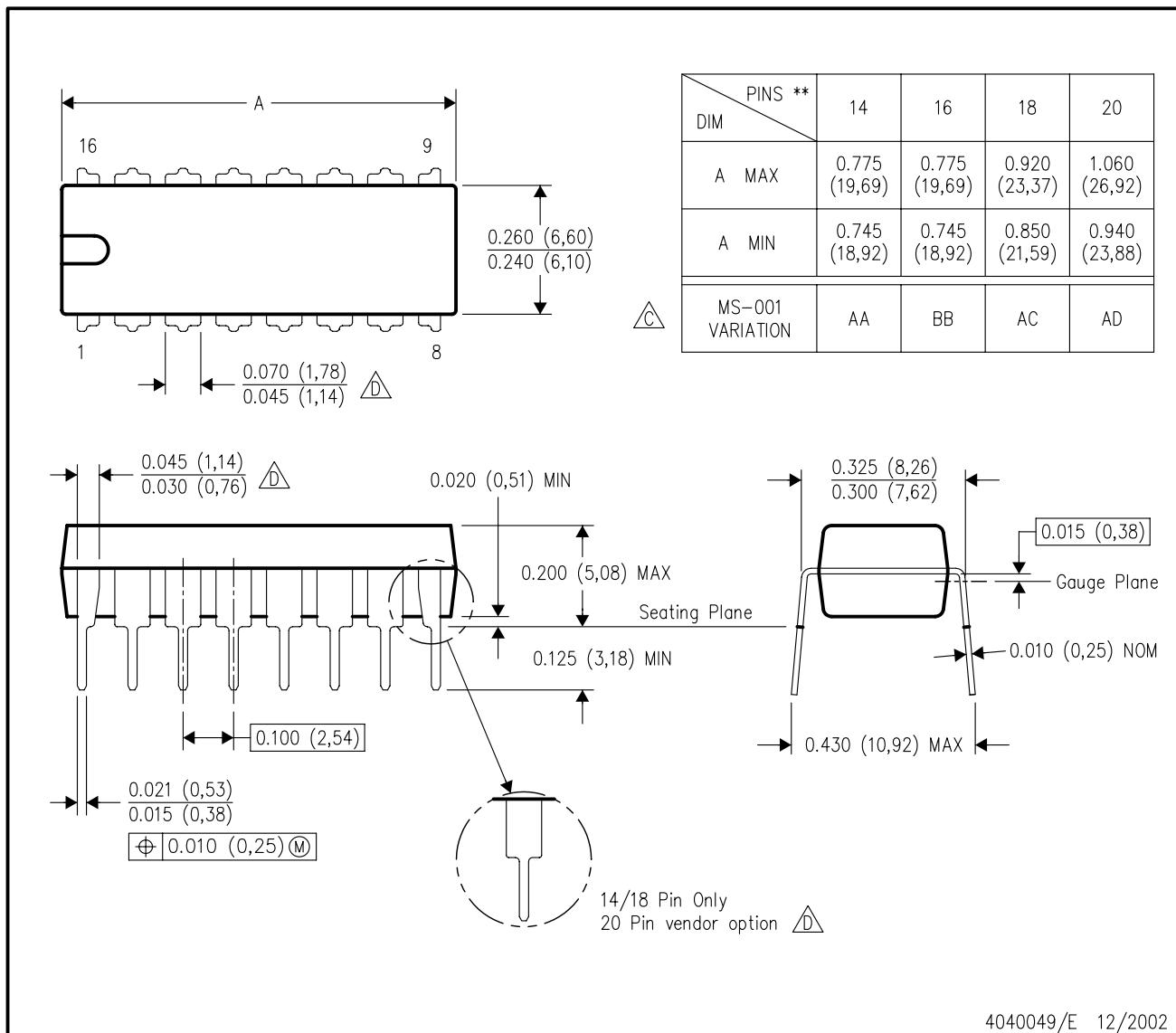


NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

## N (R-PDIP-T\*\*)

16 PINS SHOWN

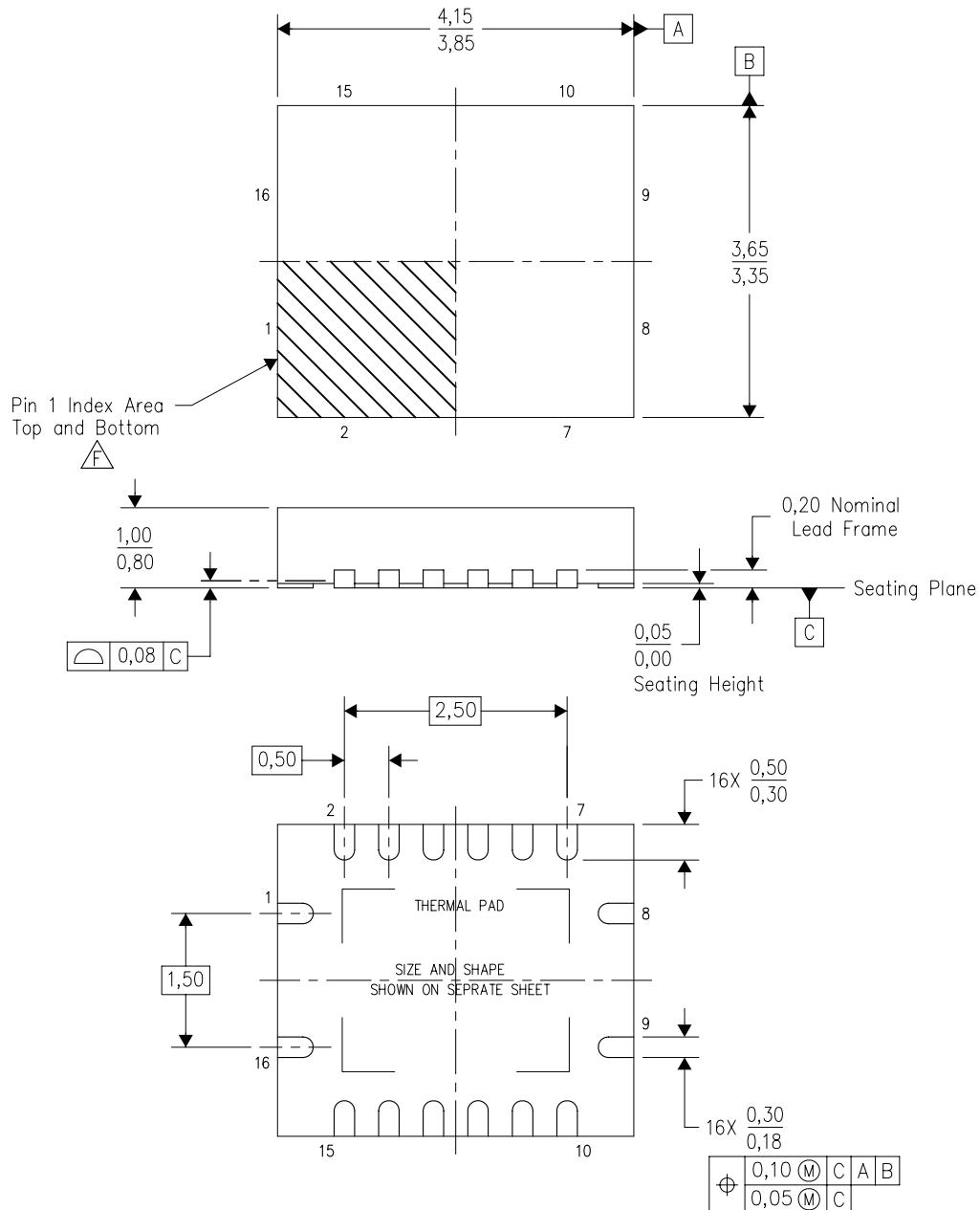
## PLASTIC DUAL-IN-LINE PACKAGE



## MECHANICAL DATA

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



Bottom View

4203539-3/l 06/2011

NOTES:

- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- QFN (Quad Flatpack No-Lead) package configuration.
- The package thermal pad must be soldered to the board for thermal and mechanical performance.
- See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- Package complies to JEDEC MO-241 variation BA.

## **THERMAL PAD MECHANICAL DATA**

RGY (R-PVQFN-N16)

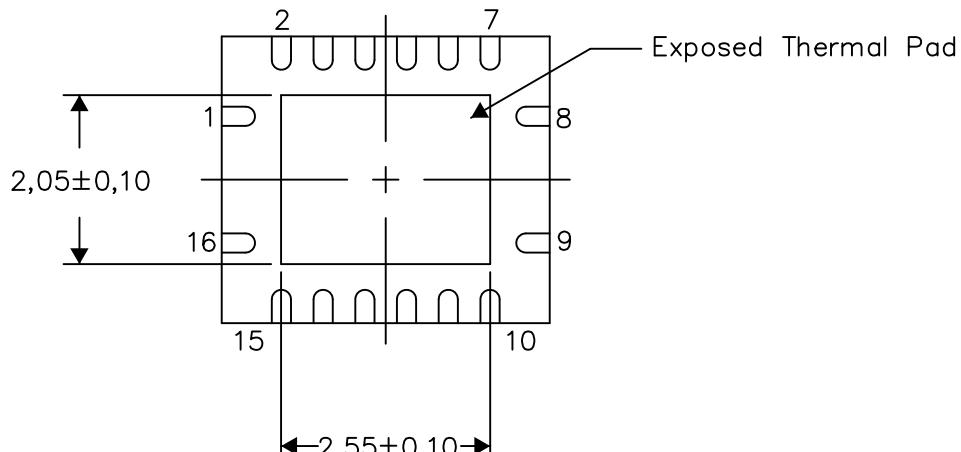
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



### Exposed Thermal Pad Dimensions

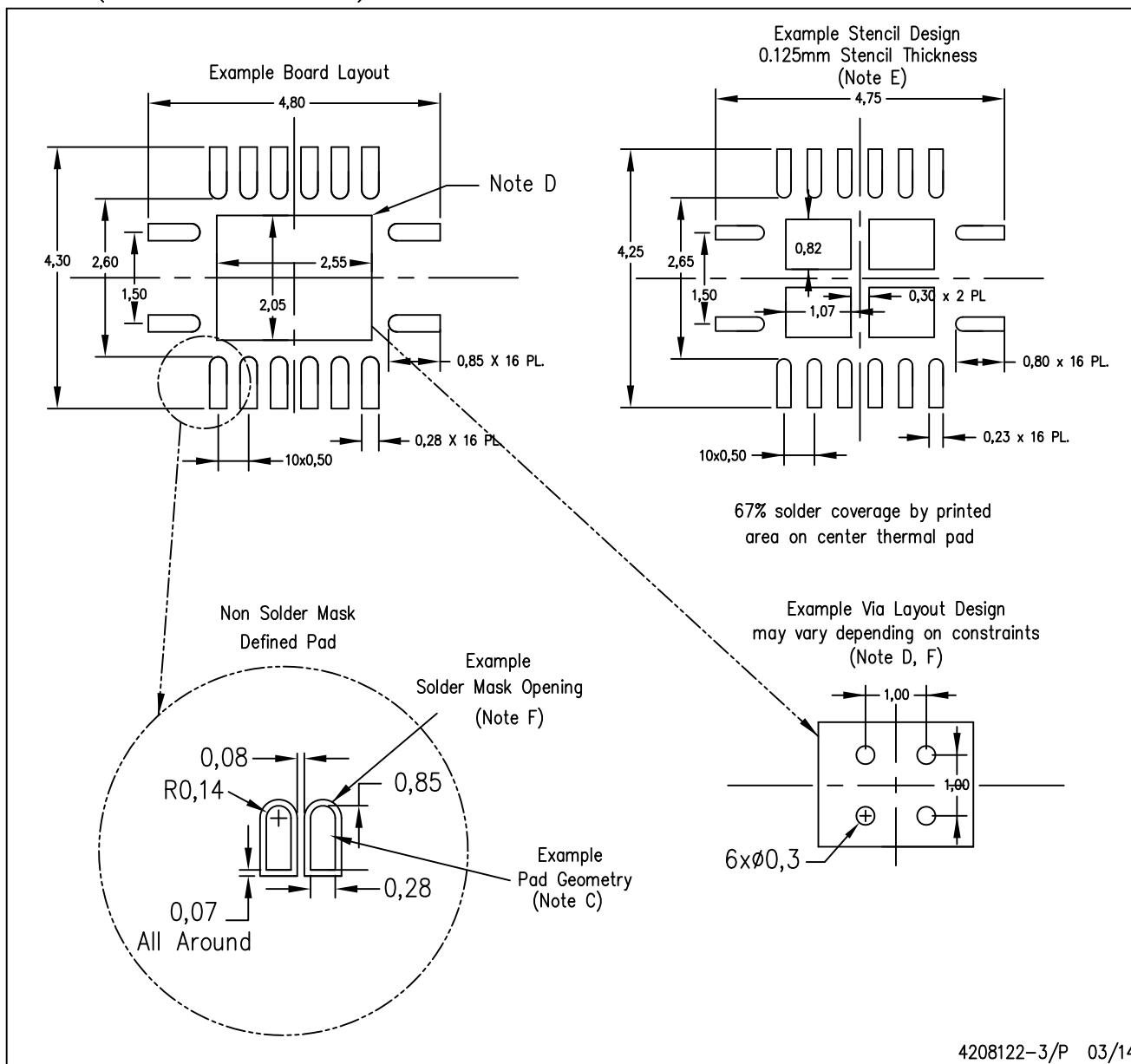
4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters

## LAND PATTERN DATA

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-3/P 03/14

**NOTES:**

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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