



PSMN012-60MS

N-channel 60 V 12 mΩ standard level MOSFET in LPAK33

19 December 2019

Product data sheet

1. General description

Standard level enhancement mode N-channel MOSFET in LPAK33 package. This product is designed and qualified for use in a wide range of motor, industrial, communications and domestic equipment.

2. Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources
- LPAK33 package is footprint compatible with other 3.3 mm footprint types
- Qualified to 175 °C

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	60	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	-	53	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	75	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 15\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11	-	10	12	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 15\text{ A}$; $V_{DS} = 48\text{ V}$; $V_{GS} = 10\text{ V}$; $T_j = 25\text{ °C}$; Fig. 13 ; Fig. 14	-	8.5	-	nC
$Q_{G(tot)}$	total gate charge		-	24.8	-	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	Source	LPAK33 (SOT1210)	mbb076
2	S	Source		
3	S	Source		
4	G	Gate		
mb	D	Mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN012-60MS	LFPAK33	Plastic, single ended surface mounted package (LFPAK33); 8 leads; 0.65 mm pitch	SOT1210

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN012-60MS	M12S60

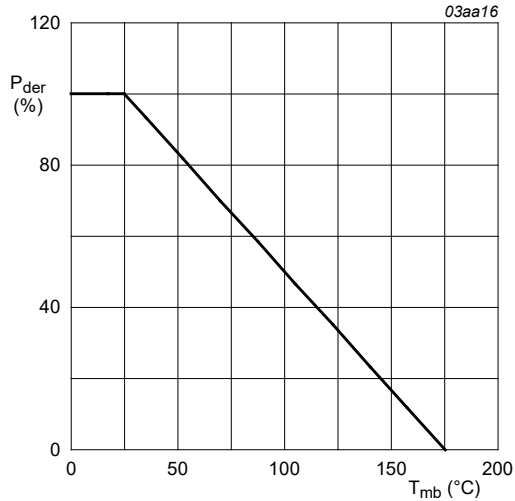
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

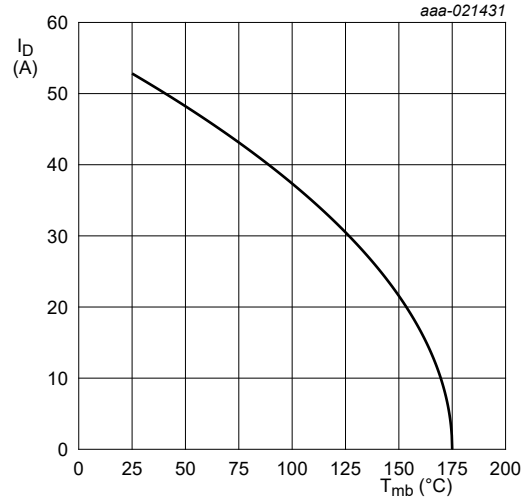
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	60	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$		-	60	V
V_{GS}	gate-source voltage	DC; $T_j \leq 175\text{ °C}$		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	75	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2		-	53	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2		-	37	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3		-	211	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$		-	53	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$		-	211	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 53\text{ A}$; $V_{sup} \leq 60\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; Fig. 4	[1]	-	34.3	mJ

[1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

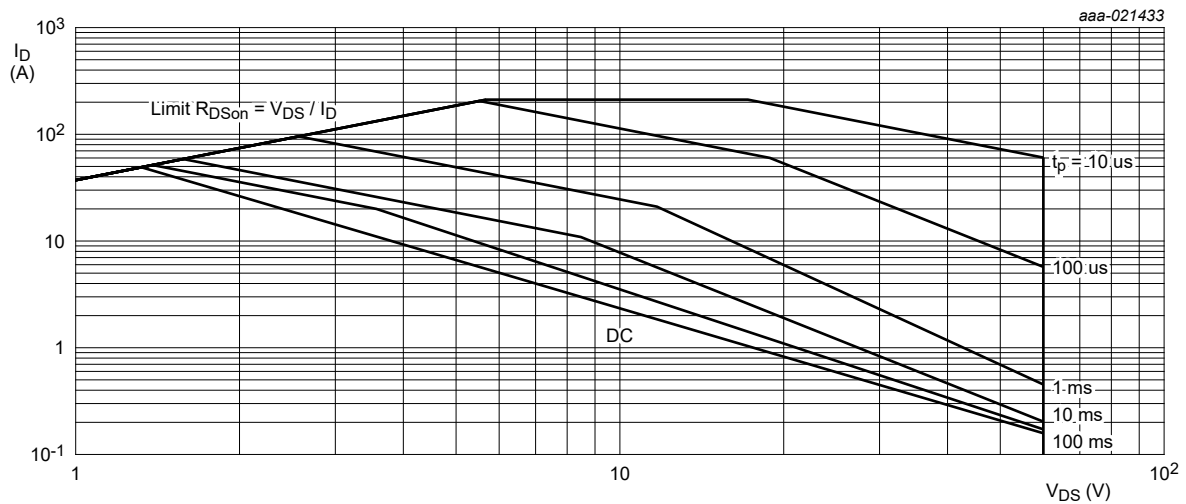
Fig. 1. Normalized total power dissipation as a function of mounting base temperature



$$V_{GS} \geq 10 \text{ V}$$

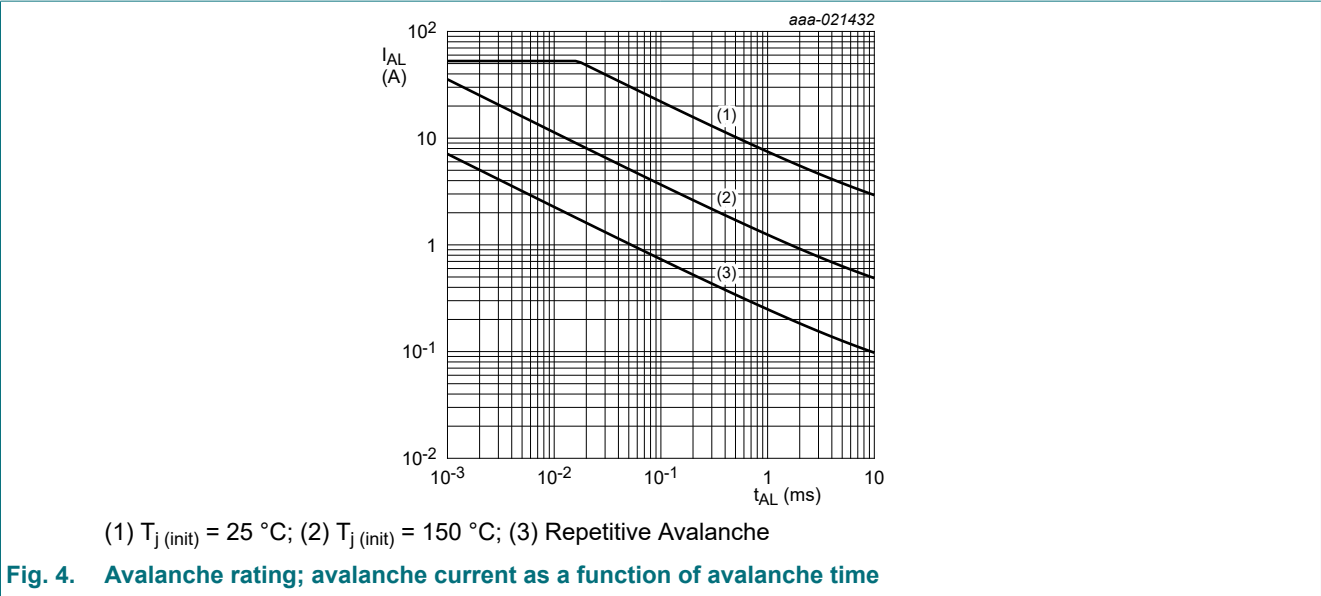
$$I_D = 53 \text{ A} \times \sqrt{\frac{175^{\circ}\text{C} - T_{mb}}{150^{\circ}\text{C}}} \quad \text{for } T_{mb} \geq 25^{\circ}\text{C}$$

Fig. 2. Continuous drain current as a function of mounting base temperature



$T_{mb} = 25^{\circ}\text{C}$; I_{DM} is a single pulse

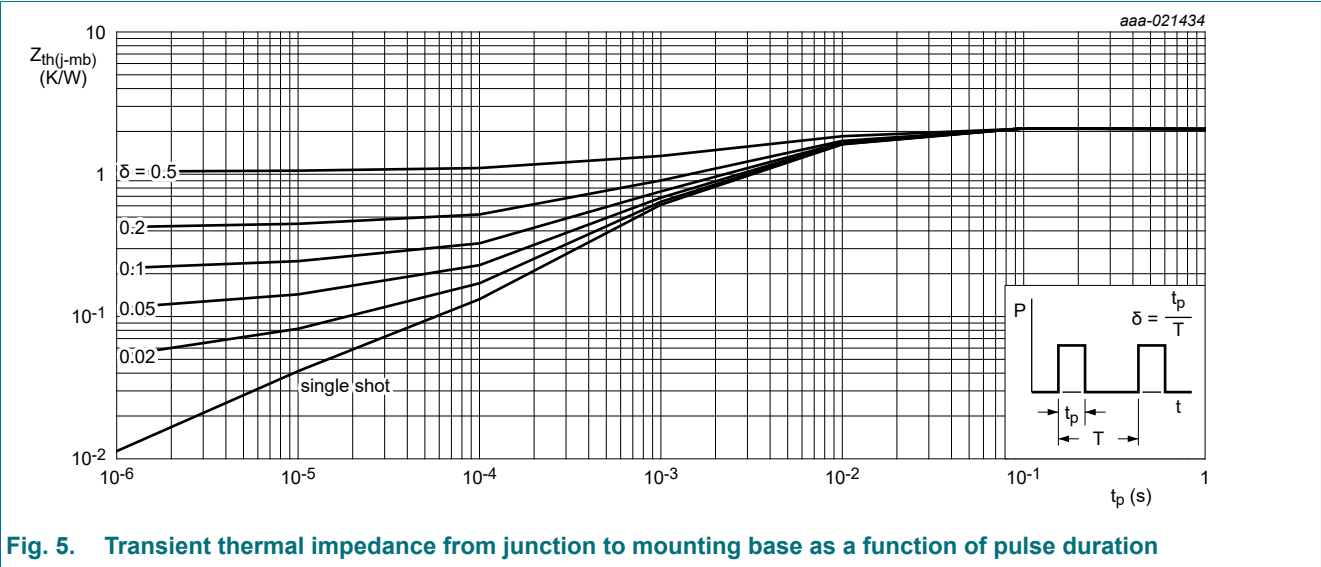
Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	1.82	2	K/W



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$	60	-	-	V
		$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_j = -55\text{ °C}$	54	-	-	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 9; Fig. 10	2.4	3	4	V
		$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = -55 \text{ }^\circ\text{C}$; Fig. 9	-	-	4.5	V
		$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 175 \text{ }^\circ\text{C}$; Fig. 9	1	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 60 \text{ V}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	0.02	1	μA
		$V_{DS} = 60 \text{ V}$; $V_{GS} = 0 \text{ V}$; $T_j = 175 \text{ }^\circ\text{C}$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{GS} = -20 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}$; $I_D = 15 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 11	-	10	12	mΩ
		$V_{GS} = 10 \text{ V}$; $I_D = 15 \text{ A}$; $T_j = 175 \text{ }^\circ\text{C}$; Fig. 12	-	-	27	mΩ

Dynamic characteristics

$Q_{G(tot)}$	total gate charge	$I_D = 15 \text{ A}$; $V_{DS} = 48 \text{ V}$; $V_{GS} = 10 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 13; Fig. 14	-	24.8	-	nC
Q_{GS}	gate-source charge		-	5.6	-	nC
Q_{GD}	gate-drain charge		-	8.5	-	nC
C_{iss}	input capacitance	$V_{DS} = 25 \text{ V}$; $V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 15	-	1222	1625	pF
C_{oss}	output capacitance		-	167	200	pF
C_{rss}	reverse transfer capacitance		-	104	143	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 45 \text{ V}$; $R_L = 3 \text{ } \Omega$; $V_{GS} = 10 \text{ V}$; $R_{G(ext)} = 5 \text{ } \Omega$; $T_j = 25 \text{ }^\circ\text{C}$	-	6.6	-	ns
t_r	rise time		-	9.7	-	ns
$t_{d(off)}$	turn-off delay time		-	17.4	-	ns
t_f	fall time		-	10.5	-	ns

Source-drain diode

V_{SD}	source-drain voltage	$I_S = 15 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 16	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 15 \text{ A}$; $dI_S/dt = -100 \text{ A}/\mu\text{s}$; $V_{GS} = 0 \text{ V}$; $V_{DS} = 25 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	19.5	-	ns
Q_r	recovered charge		-	16.6	-	nC

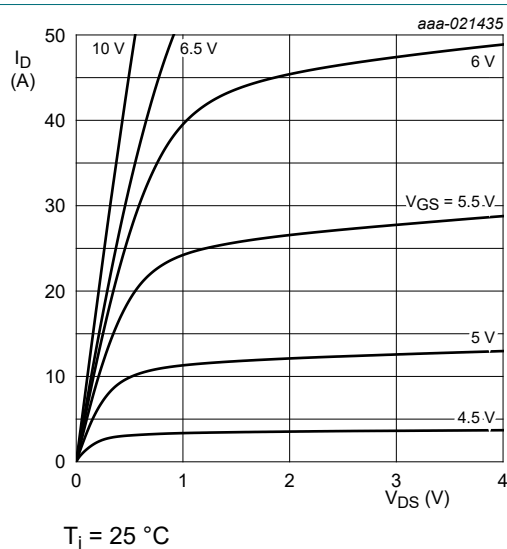


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

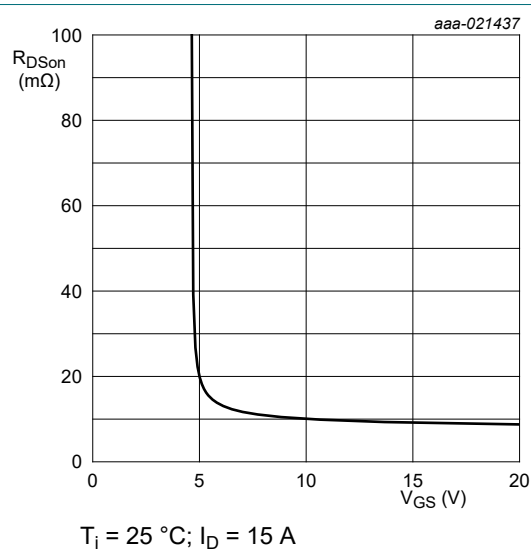


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

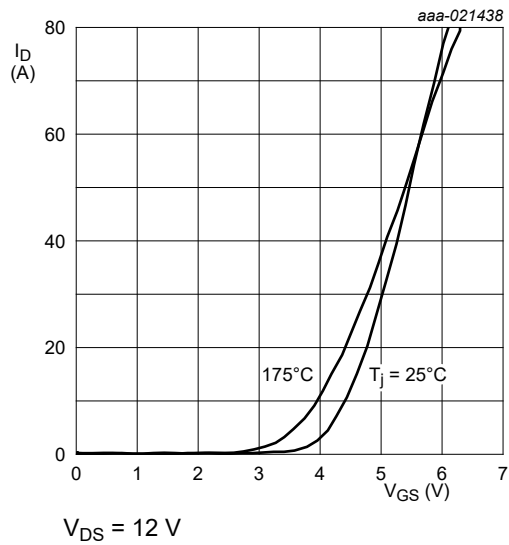


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

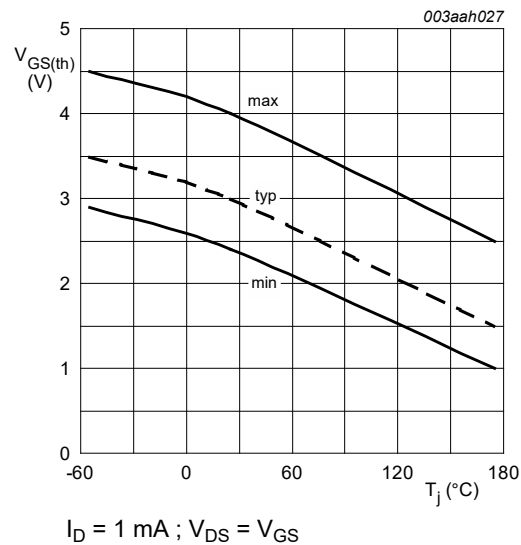


Fig. 9. Gate-source threshold voltage as a function of junction temperature

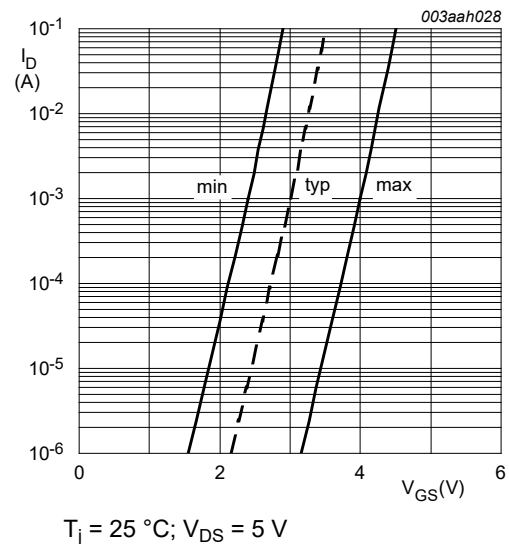


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

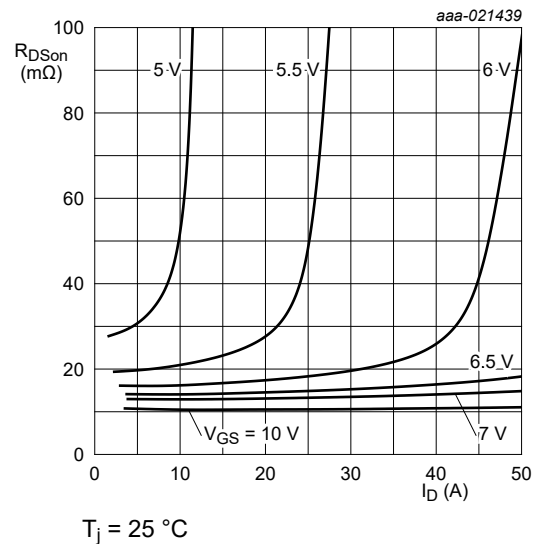


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

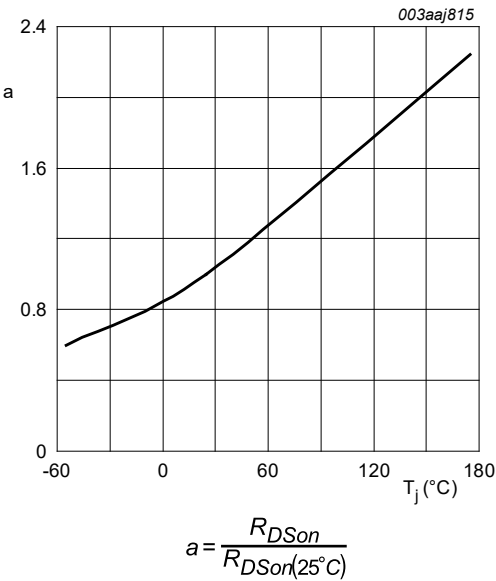


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

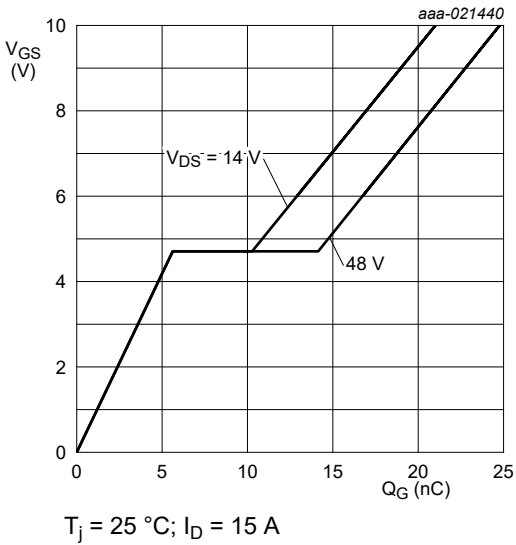


Fig. 13. Gate-source voltage as a function of gate charge; typical values

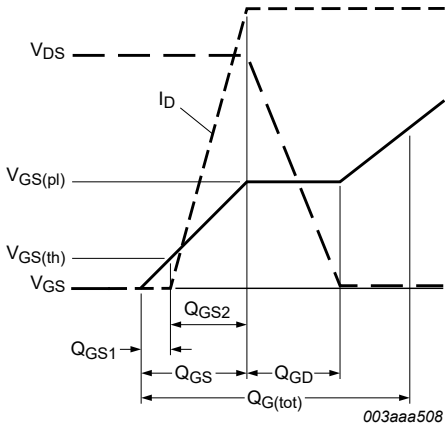


Fig. 14. Gate charge waveform definitions

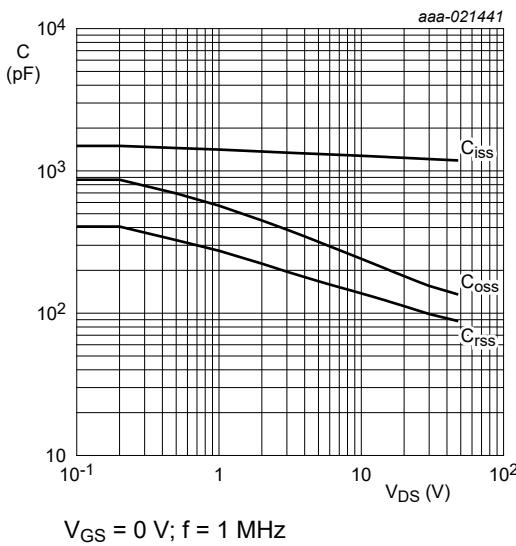
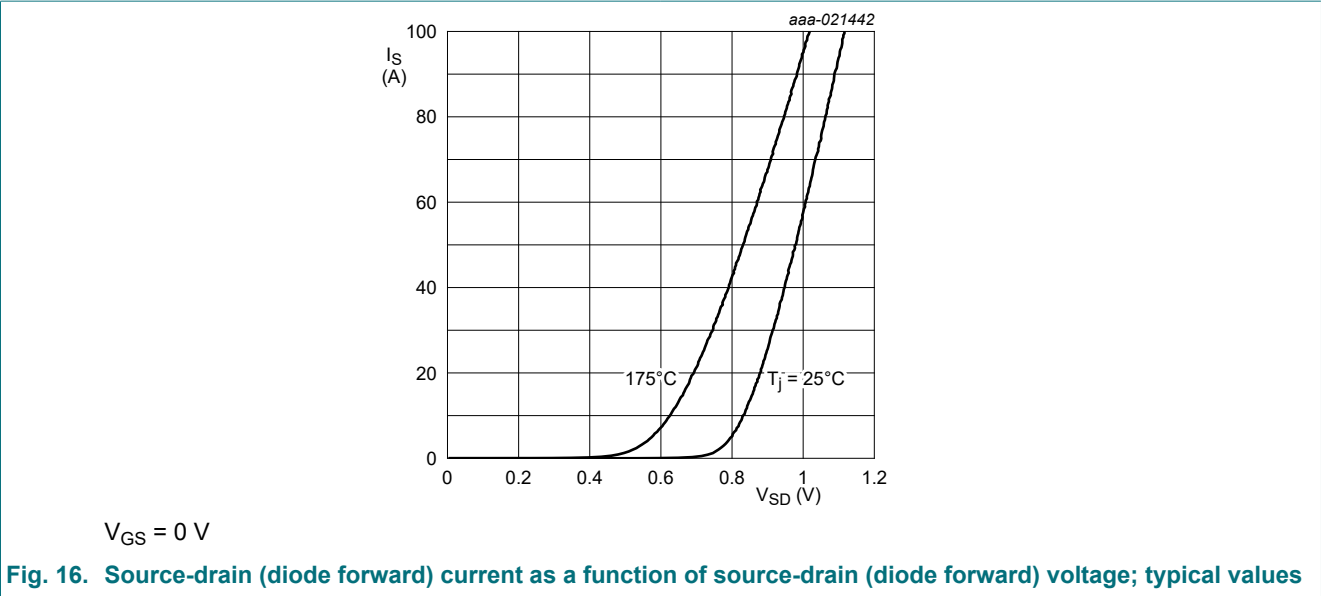


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



11. Package outline

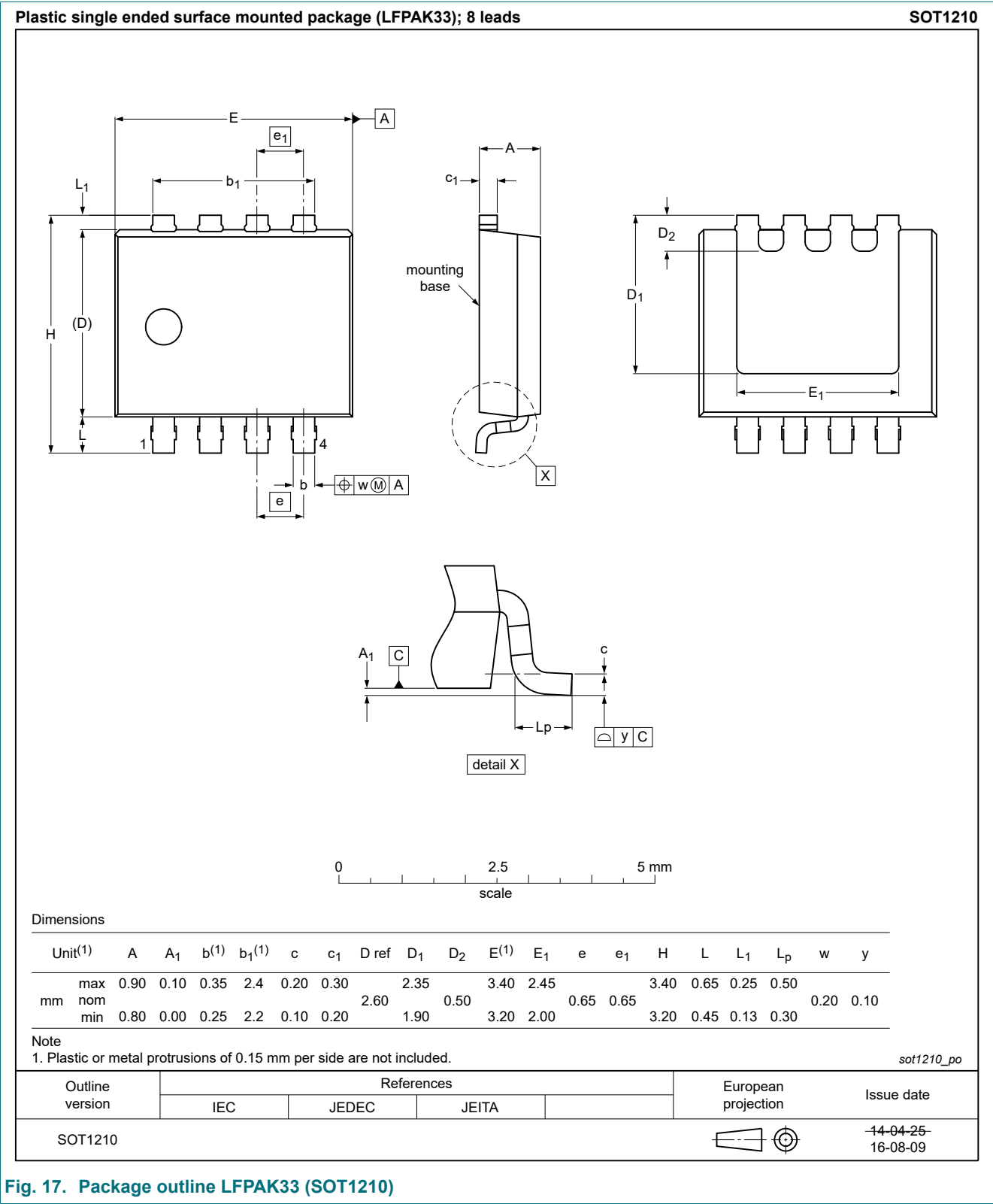


Fig. 17. Package outline LPAK33 (SOT1210)

12. Soldering

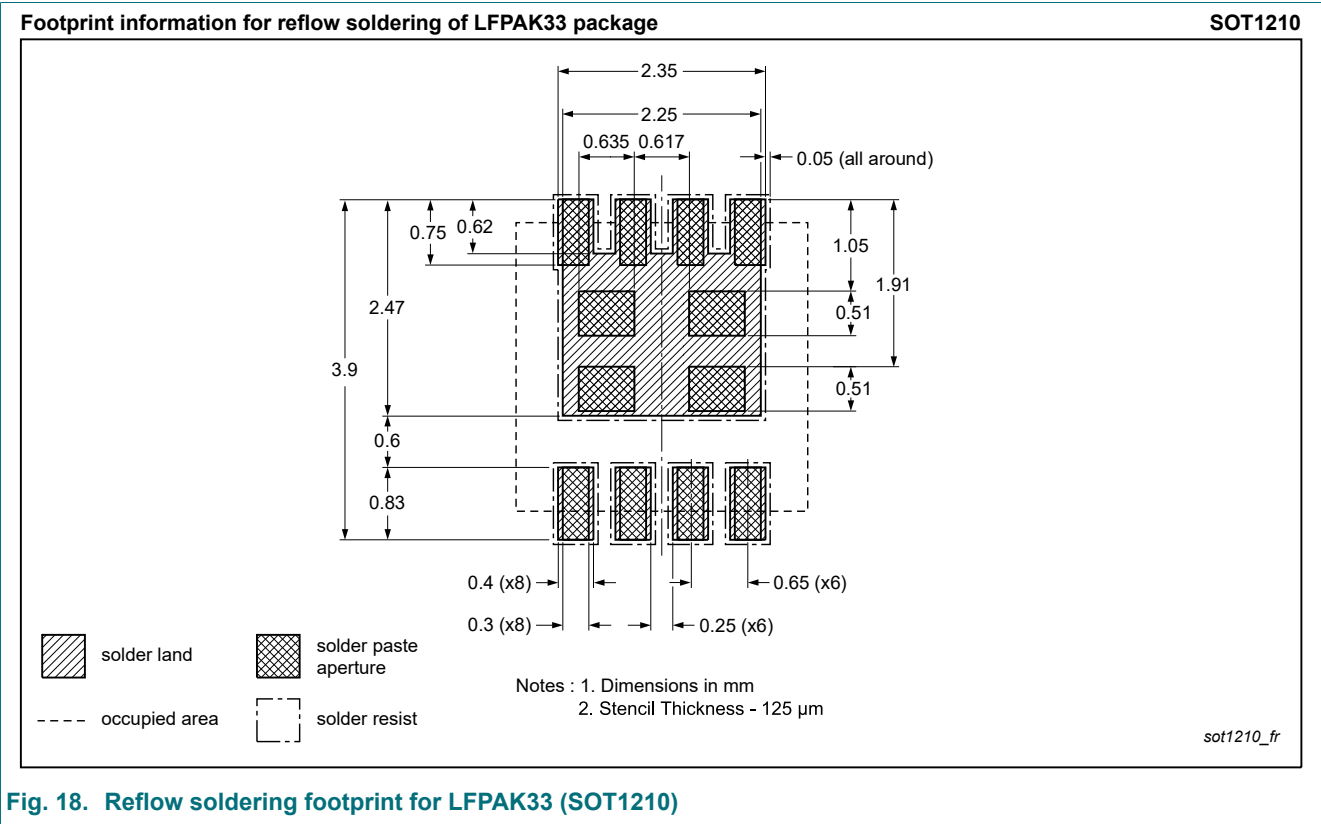


Fig. 18. Reflow soldering footprint for LPAK33 (SOT1210)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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Contents

1. General description..... 1

2. Features and benefits..... 1

4. Quick reference data..... 1

5. Pinning information..... 1

6. Ordering information..... 2

7. Marking..... 2

8. Limiting values..... 2

9. Thermal characteristics..... 4

10. Characteristics..... 4

11. Package outline..... 9

12. Soldering..... 10

13. Legal information..... 11

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