

# SN54ALS645A, SN54AS645, SN74ALS645A, SN74AS645 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SDAS278 – JANUARY 1995

- Bidirectional Bus Transceivers in High-Density 20-Pin Packages
- True Logic
- 3-State Outputs
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

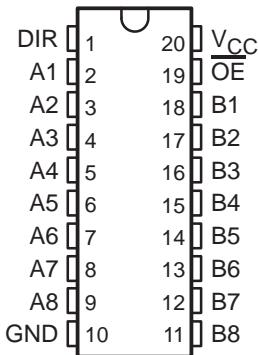
## description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated.

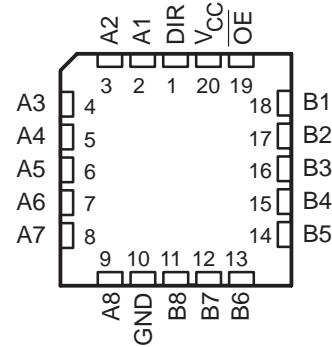
The -1 version of the SN74ALS645A is identical to the standard version, except that the recommended maximum  $I_{OL}$  is increased to 48 mA. There is no -1 version of the SN54ALS645A.

The SN54ALS645A and SN54AS645 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS645A and SN74AS645 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54ALS645A, SN54AS645 . . . J PACKAGE  
SN74ALS645A, SN74AS645 . . . DW OR N PACKAGE  
(TOP VIEW)



SN54ALS645A, SN54AS645 . . . FK PACKAGE  
(TOP VIEW)



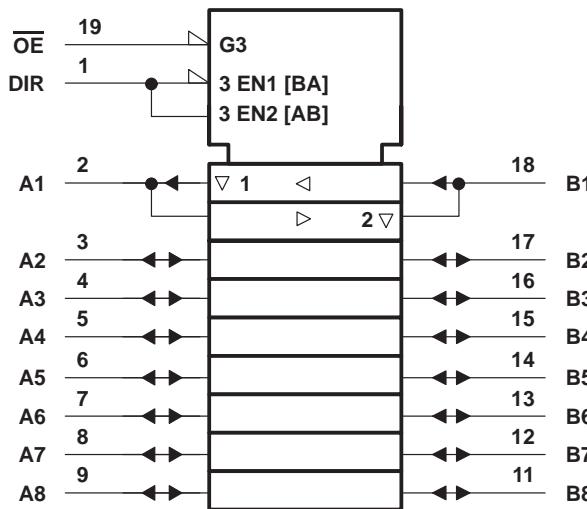
FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

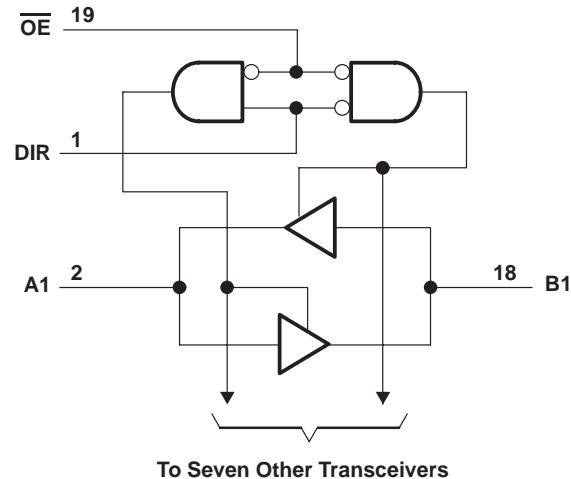
**SN54ALS645A, SN54AS645, SN74ALS645A, SN74AS645  
OCTAL BUS TRANSCEIVERS  
WITH 3-STATE OUTPUTS**

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**logic symbol†**



**logic diagram (positive logic)**



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡**

Supply voltage, $V_{CC}$ .....	7 V
Input voltage, $V_I$ : All inputs .....	7 V
I/O ports .....	5.5 V
Operating free-air temperature range, $T_A$ : SN54ALS645A .....	–55°C to 125°C
SN74ALS645A .....	0°C to 70°C
Storage temperature range .....	–65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**recommended operating conditions**

		SN54ALS645A			SN74ALS645A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$I_{OH}$	High-level output current			–12			–15	mA
$I_{OL}$	Low-level output current			12			24	mA
							48§	
$T_A$	Operating free-air temperature	–55		125	0		70	°C

§ Applies only to the -1 version and only if  $V_{CC}$  is between 4.75 V and 5.25 V

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN54ALS645A			SN74ALS645A			UNIT
		MIN	TYPT <sup>†</sup>	MAX	MIN	TYPT <sup>†</sup>	MAX	
$V_{IK}$	$V_{CC} = 4.5 \text{ V}$ , $I_I = -18 \text{ mA}$			-1.5			-1.5	V
$V_{OH}$	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ , $I_{OH} = -0.4 \text{ mA}$	$V_{CC} - 2$		$V_{CC} - 2$				V
	$V_{CC} = 4.5 \text{ V}$	$I_{OH} = -3 \text{ mA}$	2.4	3.2	2.4	3.2		
		$I_{OH} = -12 \text{ mA}$	2					
		$I_{OH} = -15 \text{ mA}$				2		
$V_{OL}$	$V_{CC} = 4.5 \text{ V}$	$I_{OL} = 12 \text{ mA}$	0.25	0.4	0.25	0.4		V
		$I_{OL} = 24 \text{ mA}$			0.35	0.5		
		$I_{OL} = 48 \text{ mA}^{\ddagger}$			0.35	0.5		
$I_I$	Control inputs	$V_I = 7 \text{ V}$		0.1		0.1		mA
	A or B ports	$V_I = 5.5 \text{ V}$		0.1		0.1		
$I_{IH}$	Control inputs	$V_{CC} = 5.5 \text{ V}$ , $V_I = 2.7 \text{ V}$		20		20		$\mu\text{A}$
	A or B ports $\S$			20		20		
$I_{IL}$	Control inputs	$V_{CC} = 5.5 \text{ V}$ , $V_I = 0.4 \text{ V}$		-0.1		-0.1		mA
	A or B ports $\S$			-0.1		-0.1		
$I_{O\ddagger}$	$V_{CC} = 5.5 \text{ V}$ , $V_O = 2.25 \text{ V}$	-20	-112	-30	-112			mA
$I_{CC}$	$V_{CC} = 5.5 \text{ V}$	Outputs high	30	48	30	45		mA
		Outputs low	36	60	36	55		
		Outputs disabled	38	63	38	58		

<sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

<sup>‡</sup> Applies only to the -1 version and only if  $V_{CC}$  is between 4.75 V and 5.25 V

$\S$  For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

$\ddagger$  The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

### switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ , $C_L = 50 \text{ pF}$ , $R1 = 500 \Omega$ , $R2 = 500 \Omega$ , $T_A = \text{MIN to MAX}^{\#}$				UNIT	
			SN54ALS645A		SN74ALS645A			
			MIN	MAX	MIN	MAX		
$t_{PLH}$	A or B	B or A	1	19	3	10	ns	
$t_{PHL}$			1	14	3	10		
$t_{PZH}$	$\overline{OE}$	A or B	2	30	5	20	ns	
$t_{PZL}$			2	29	5	20		
$t_{PHZ}$	$\overline{OE}$	A or B	2	14	2	10	ns	
$t_{PLZ}$			2	30	4	15		

# For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

# SN54ALS645A, SN54AS645, SN74ALS645A, SN74AS645 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

		SN54AS645			SN74AS645			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
I <sub>OH</sub>	High-level output current			-12			-15	mA
I <sub>OL</sub>	Low-level output current			48			64	mA
T <sub>A</sub>	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS645			SN74AS645			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IK}$	$V_{CC} = 4.5 \text{ V}$ , $I_L = -18 \text{ mA}$			-1.2			-1.2	V
$V_{OH}$	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ , $I_{OH} = -2 \text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5 \text{ V}$	$I_{OH} = -3 \text{ mA}$	2.4	3.2	2.4	3.2		
		$I_{OH} = -12 \text{ mA}$	2.4					
		$I_{OH} = -15 \text{ mA}$			2.4			
$V_{OL}$	$V_{CC} = 4.5 \text{ V}$	$I_{OL} = 48 \text{ mA}$	0.3	0.55				V
		$I_{OL} = 64 \text{ mA}$				0.35	0.55	
$I_I$	Control inputs	$V_{CC} = 5.5 \text{ V}$	$V_I = 7 \text{ V}$		0.1		0.1	mA
	A or B ports		$V_I = 5.5 \text{ V}$		0.1		0.1	
$I_{IH}$	Control inputs	$V_{CC} = 5.5 \text{ V}$	$V_I = 2.7 \text{ V}$		20		20	$\mu\text{A}$
	A or B ports§				70		70	
$I_{IL}$	Control inputs	$V_{CC} = 5.5 \text{ V}$	$V_I = 0.4 \text{ V}$		-0.5		-0.5	mA
	A or B ports§				-0.75		-0.75	
$I_O$ ¶	$V_{CC} = 5.5 \text{ V}$ , $V_O = 2.25 \text{ V}$		-50	-150	-50	-150	mA	
$I_{CC}$	$V_{CC} = 5.5 \text{ V}$	Outputs high	62	97	62	97		mA
		Outputs low	95	149	95	149		
		Outputs disabled	79	123	79	123		

<sup>†</sup> All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{SC}$ .

switching characteristics (see Figure 1)

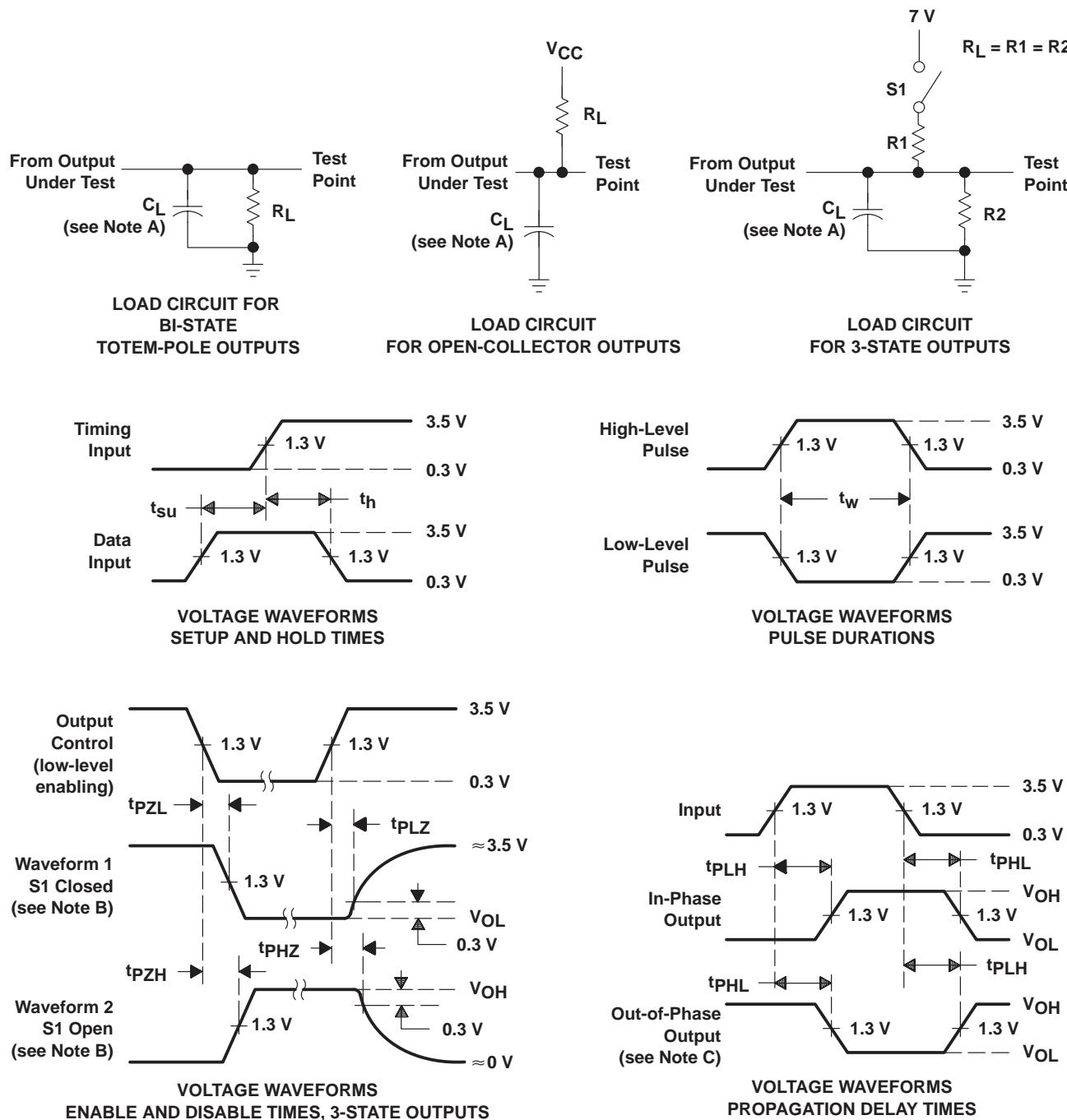
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $C_L = 50\text{ pF}$ , $R1 = 500\text{ }\Omega$ , $R2 = 500\text{ }\Omega$ , $T_A = \text{MIN to MAX}^{\dagger}$				UNIT	
			SN54AS645		SN74AS645			
			MIN	MAX	MIN	MAX		
$t_{PLH}$	A or B	B or A	2	11	2	9.5	ns	
$t_{PHL}$			2	10.5	2	9		
$t_{PZH}$	$\overline{OE}$	A or B	2	12	2	11	ns	
$t_{PZL}$			2	12	2	10		
$t_{PHZ}$	$\overline{OE}$	A or B	2	8	2	7	ns	
$t_{PLZ}$			2	13	2	12		

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**SN54ALS645A, SN54AS645, SN74ALS645A, SN74AS645  
OCTAL BUS TRANSCEIVERS  
WITH 3-STATE OUTPUTS**

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**PARAMETER MEASUREMENT INFORMATION  
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES**



NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $t_r = t_f = 2 \text{ ns}$ , duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
8403301RA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8403301RA SNJ54ALS645AJ	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
8403301SA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8403301SA SNJ54ALS645AW	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN54ALS645AJ	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54ALS645AJ	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN54AS645J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54AS645J	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74ALS645A-1DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS645A-1	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74ALS645A-1DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS645A-1	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74ALS645A-1N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS645A-1N	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74ALS645A-1NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS645A-1	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74ALS645ADW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS645A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74ALS645ADWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS645A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74ALS645AN	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS645AN	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74ALS645ANSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS645A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AS645N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74AS645N	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54ALS645AJ	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8403301RA SNJ54ALS645AJ	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54ALS645AW	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8403301SA SNJ54ALS645AW	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54AS645J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54AS645J	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

**(2) RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3) MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54ALS645A, SN54AS645, SN74ALS645A, SN74AS645 :**

- Catalog: [SN74ALS645A](#), [SN74AS645](#)
- Military: [SN54ALS645A](#), [SN54AS645](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product



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## PACKAGE OPTION ADDENDUM

4-Feb-2021

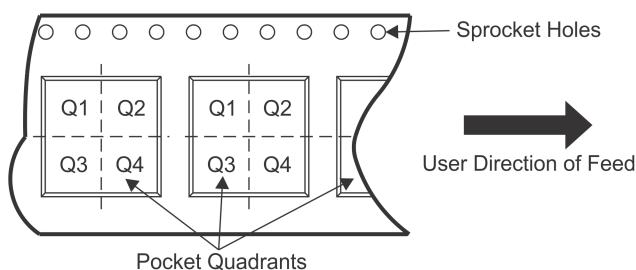
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- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


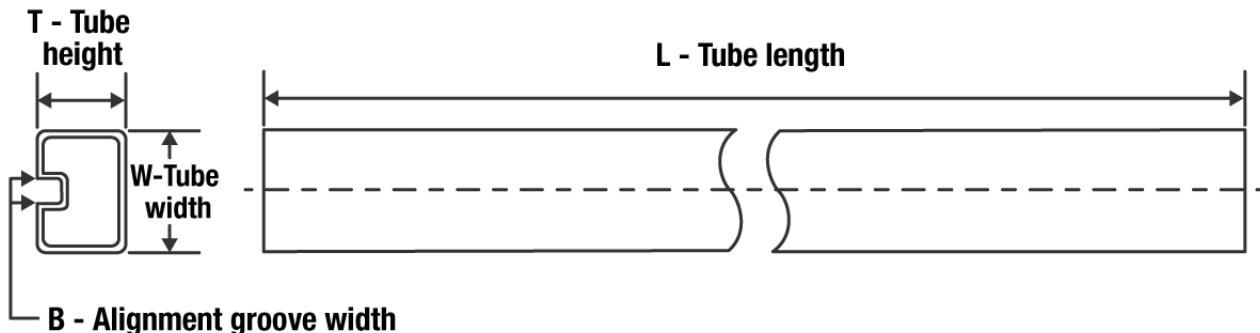
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS645A-1DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ALS645A-1NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74ALS645ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ALS645ANSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS645A-1DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74ALS645A-1NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74ALS645ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74ALS645ANSR	SO	NS	20	2000	367.0	367.0	45.0

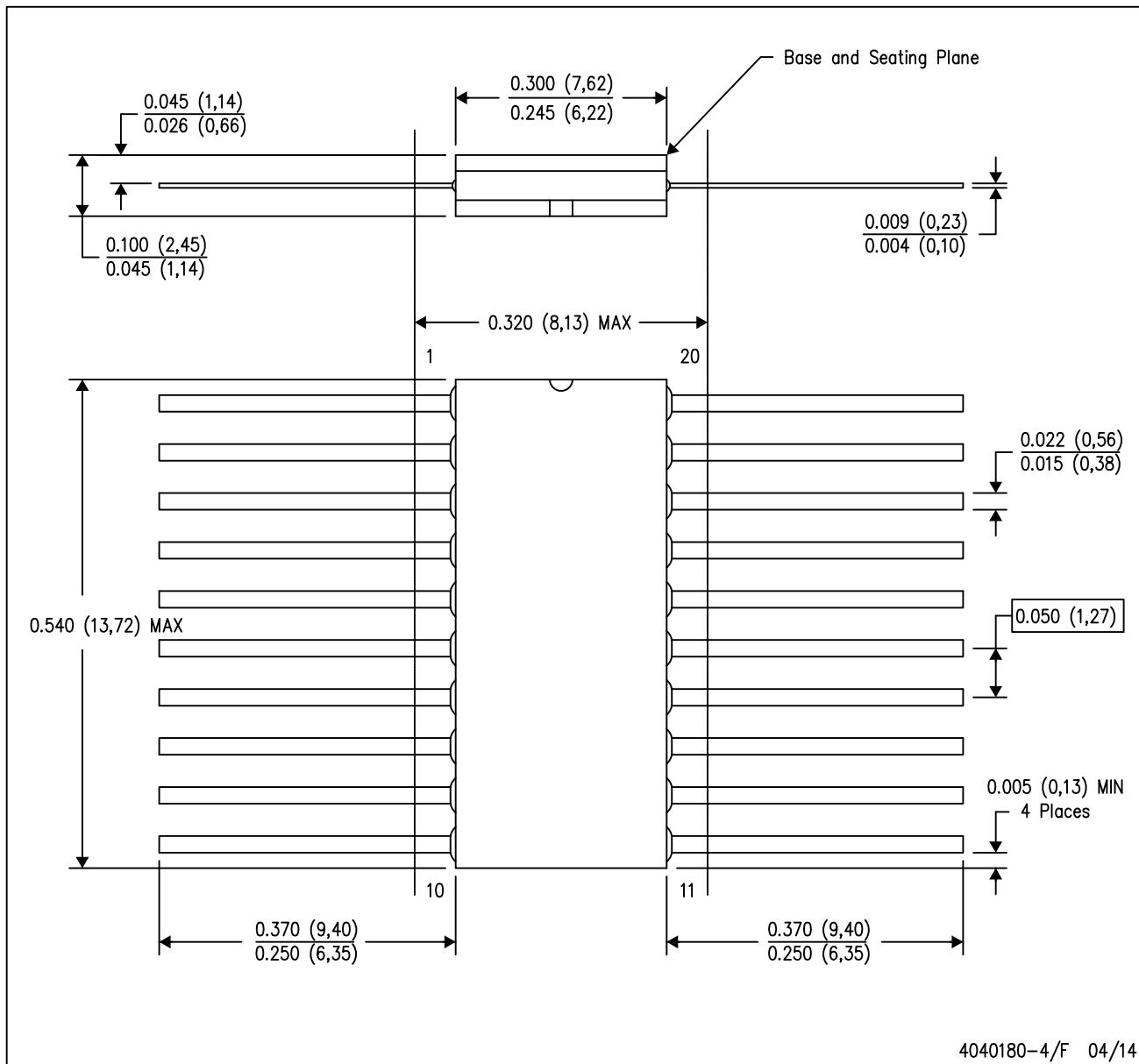
**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ALS645A-1DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS645A-1N	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS645ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS645AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74AS645N	N	PDIP	20	20	506	13.97	11230	4.32

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



NOTES:

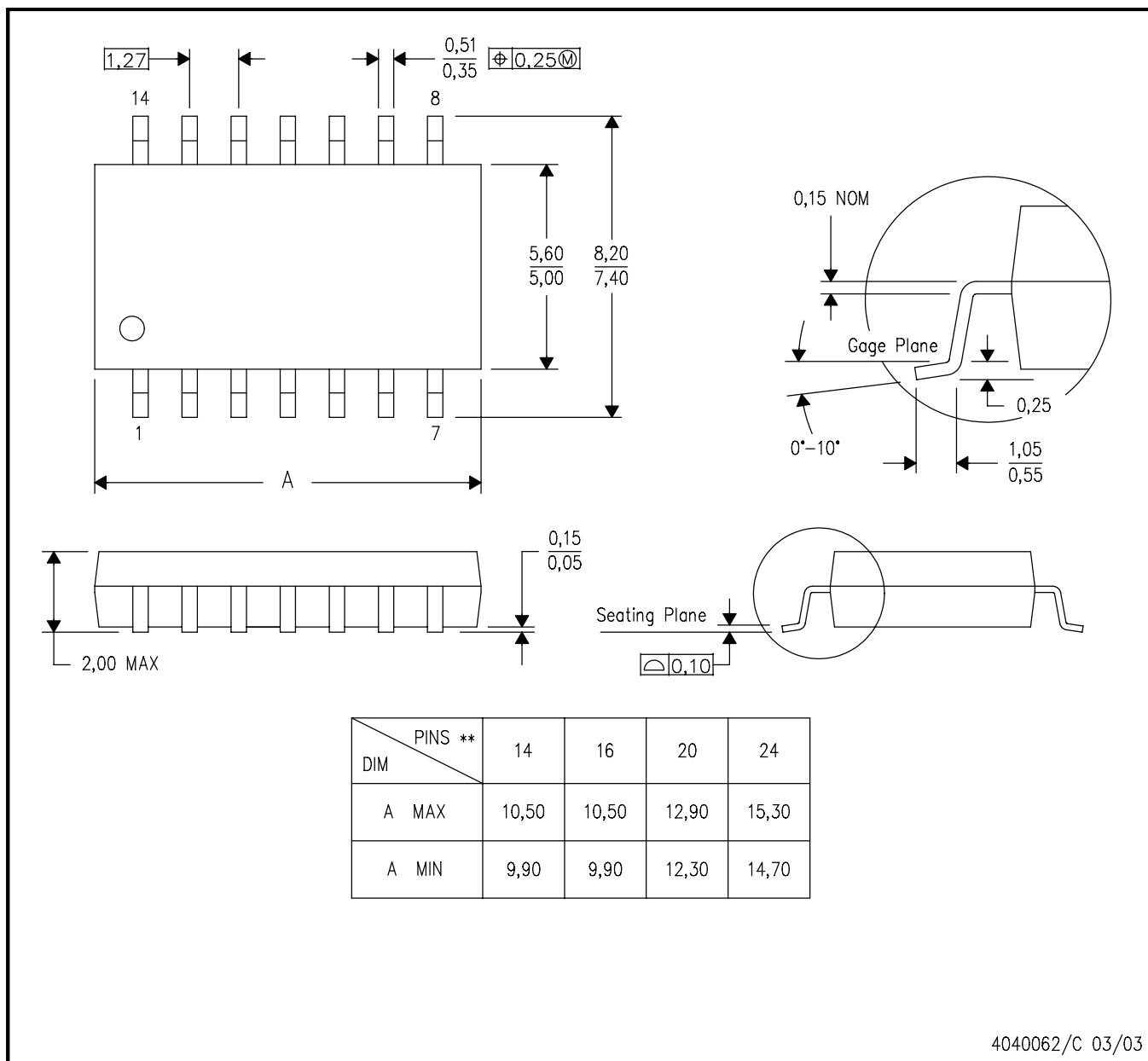
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



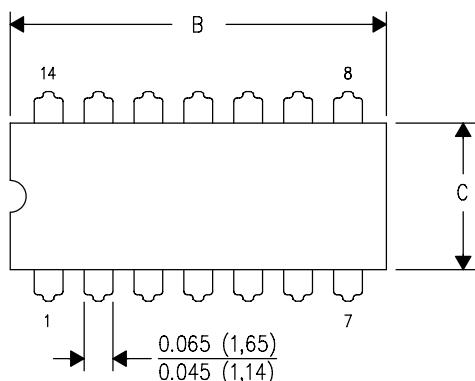
4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

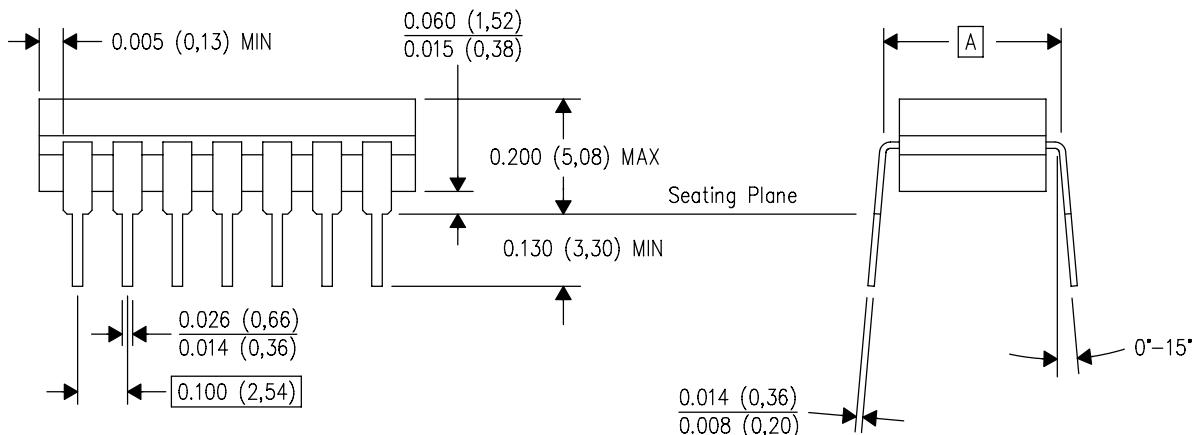
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

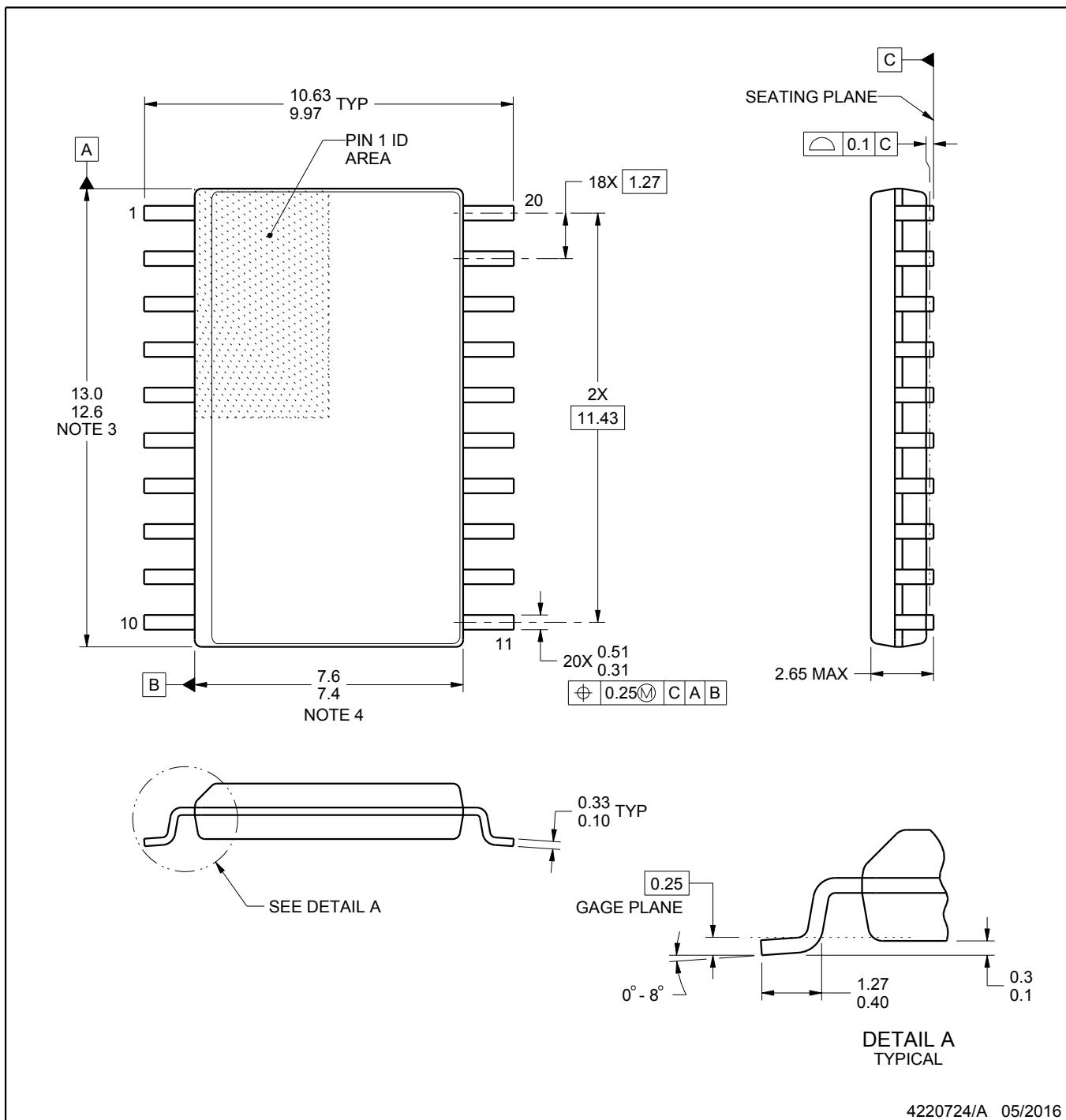
# PACKAGE OUTLINE

DW0020A



SOIC - 2.65 mm max height

SOIC



## NOTES:

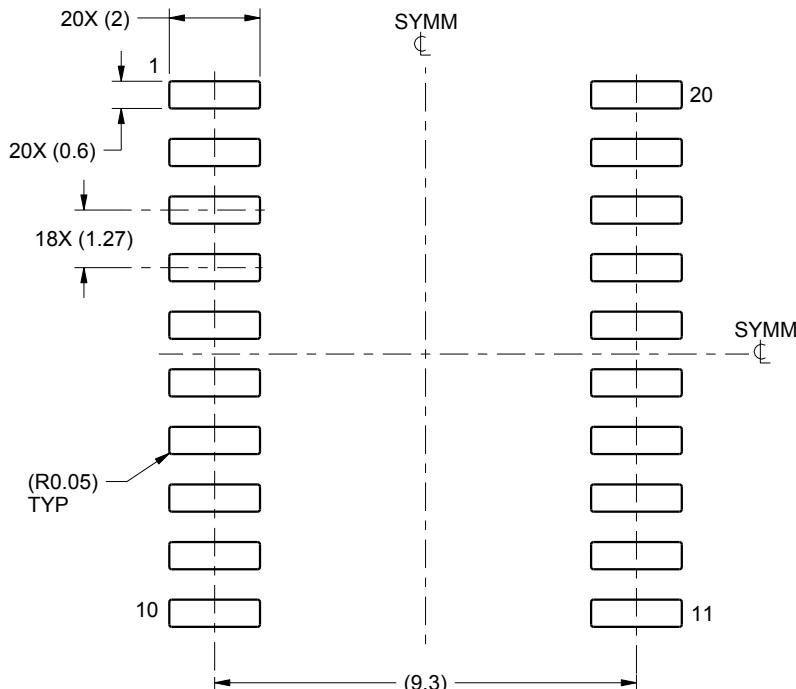
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

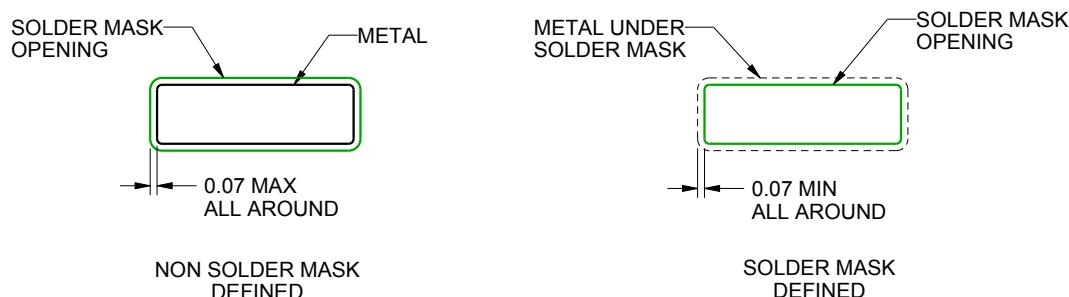
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

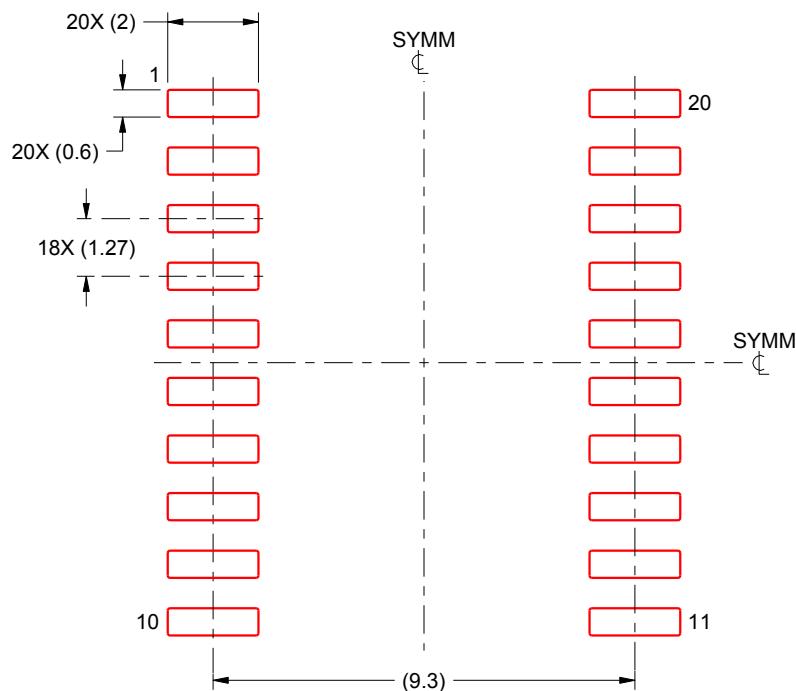
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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