

MOSFET - Power, Single N-Channel, PQFN8

120 V, 4.0 mΩ, 114 A

FDMS4D0N12C

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These are Pb-free, Halogen Free / BFR Free and are RoHS Compliant

Typical Applications

- Synchronous Rectification
- AC-DC and DC-DC Power Supplies
- AC-DC Adapters (USB PD) SR
- Load Switch

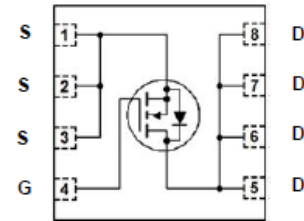
MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	120	V
Gate-to-Source Voltage			V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Note 7)	Steady State	$T_C = 25^{\circ}\text{C}$	I_D	114	A
Power Dissipation $R_{\theta JC}$ (Note 2)			P_D	106	W
Continuous Drain Current $R_{\theta JA}$ (Note 6, 7)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	18.5	A
Power Dissipation $R_{\theta JA}$ (Note 6, 7)			P_D	2.7	W
Pulsed Drain Current	$T_A = 25^{\circ}\text{C}$, $t_p = 10\text{ }\mu\text{s}$		I_{DM}	628	A
Operating Junction and Storage Temperature			T_J , T_{stg}	-55 to +150	$^{\circ}\text{C}$
Source Current (Body Diode)			I_S	114	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{AV} = 66.7\text{ A}$, $L = 0.1\text{ mH}$)			E_{AS}	222	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)			T_L	300	$^{\circ}\text{C}$

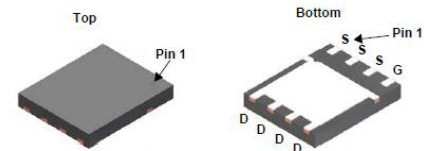
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

$V_{(BR)DDS}$	$I_D \text{ MAX}$	$R_{DS(on)} \text{ MAX}$
120 V	67 A	4.0 mΩ @ 10 V
	33 A	8.0 mΩ @ 6 V

ELECTRICAL CONNECTION

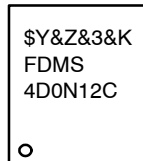


N-Channel MOSFET



PQFN8 5x6
(Power 56)
CASE 483AF

MARKING DIAGRAM



\$Y = onsemi Logo
 &Z = Assembly Plant Code
 &3 = Numeric Date Code
 &K = Lot Code
 FDMS4D0N12C = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDMS4D0N12C

ORDERING INFORMATION

Device	Package	Shipping†
FDMS4D0N12C	PQFN8 (Pb-Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction – to – Case – Steady State (Note 7)	$R_{\theta JC}$	1.18	°C/W
Junction – to – Ambient – Steady State (Note 7)	$R_{\theta JA}$	45	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
--------	-----------	-----------------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain – to – Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	120			V
Drain – to – Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\text{ }\mu\text{A}$, ref to 25°C		49		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 96\text{ V}$	$T_J = 25^\circ\text{C}$		1	μA
			$T_J = 125^\circ\text{C}$		100	μA
Gate – to – Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 8)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 370\text{ }\mu\text{A}$	2.0		4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 370\text{ }\mu\text{A}$, ref to 25°C		-8.5		mV/°C
Drain – to – Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 67\text{ A}$		3.3	4.0	m Ω
		$V_{GS} = 6\text{ V}, I_D = 33\text{ A}$		4.7	8.0	
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 67\text{ A}$		144		S
Gate-Resistance	R_G	$T_A = 25^\circ\text{C}$		0.9	1.8	Ω

CHARGES & CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 60\text{ V}$		4565	6460	pF
Output Capacitance	C_{OSS}			2045	3060	
Reverse Transfer Capacitance	C_{RSS}			17	24	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 6\text{ V}, V_{DS} = 60\text{ V}, I_D = 67\text{ A}$		36	51	nC
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 60\text{ V}, I_D = 67\text{ A}$		58	82	
Gate-to-Source Charge	Q_{GS}			21		
Gate-to-Drain Charge	Q_{GD}			9		
Plateau Voltage	V_{GP}			5		
Output Charge	Q_{OSS}	$V_{DD} = 60\text{ V}, V_{GS} = 0\text{ V}$		207		nC

FDMS4D0N12C

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
--------	-----------	-----------------	-----	-----	-----	------

SWITCHING CHARACTERISTICS (Note 8)

Turn – On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 60\text{ V},$ $I_D = 67\text{ A}, R_G = 6\ \Omega$		25	41	ns
Rise Time	t_r			8	16	
Turn – Off Delay Time	$t_{d(OFF)}$			45	72	
Fall Time	t_f			12	22	

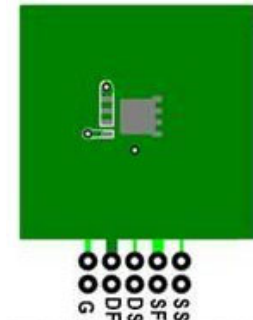
DRAIN–SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V},$ $I_S = 67\text{ A}$	$T_J = 25^\circ\text{C}$		0.86	1.3	V
			$T_J = 125^\circ\text{C}$		0.7	1.2	
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V},$ $dI_S/dt = 300\text{ A}/\mu\text{s},$ $I_S = 33\text{ A}$			53	84	ns
Reverse Recovery Charge	Q_{RR}				175	280	nC
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V},$ $dI_S/dt = 1000\text{ A}/\mu\text{s},$ $I_S = 33\text{ A}$			36	57	ns
Reverse Recovery Charge	Q_{RR}				360	575	nC

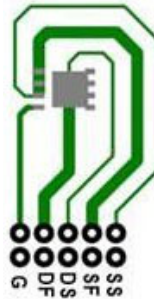
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR–4 material. $R_{\theta CA}$ is determined by the user's board design.



a) 45°C/W when mounted on a 1 in² pad of 2 oz copper.



b) 115°C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.
- E_{AS} of 222 mJ is based on starting $T_J = 25^\circ\text{C}$; $L = 0.1\text{ mH}$, $I_{AS} = 66.7\text{ A}$, $V_{DD} = 100\text{ V}$, $V_{GS} = 12\text{ V}$, 100% tested at $L = 0.1\text{ mH}$, $I_{AS} = 66.7\text{ A}$.
- Pulsed I_D please refer to Fig. 11 SOA graph for more details.
- Computed continuous current limited to max Junction Temperature only, actual continuous current will be limited by thermal & electro–mechanical application board design.
- Surface–mounted on FR4 board using 1 in² pad size, 2 oz Cu pad.
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

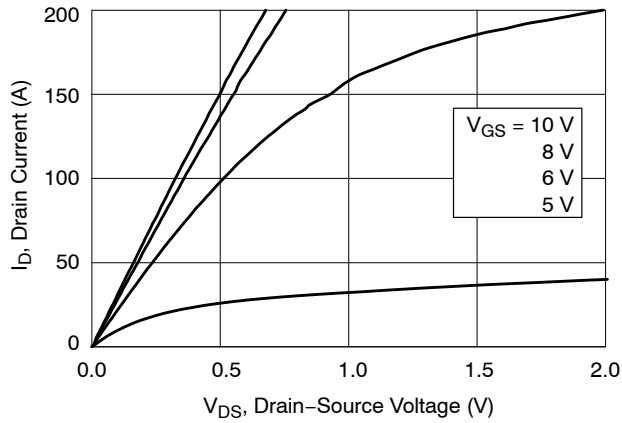


Figure 1. On-Region Characteristics

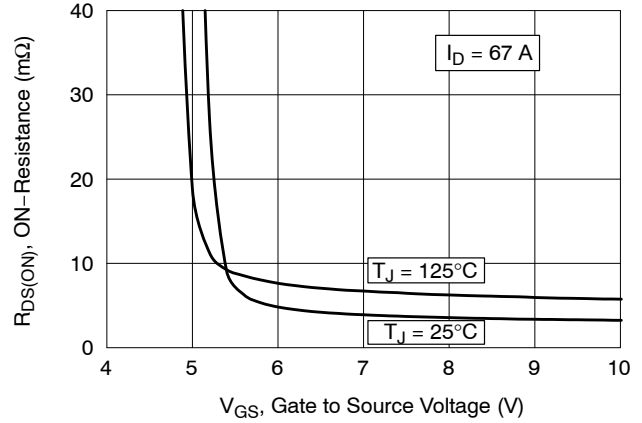


Figure 2. Transfer Characteristics

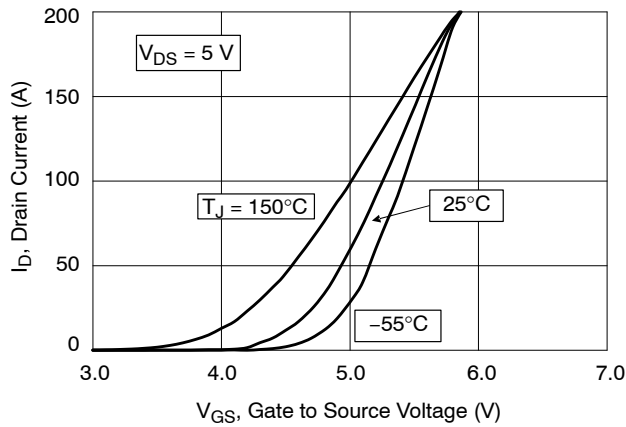


Figure 3. On-Resistance vs. Gate-to-Source Voltage

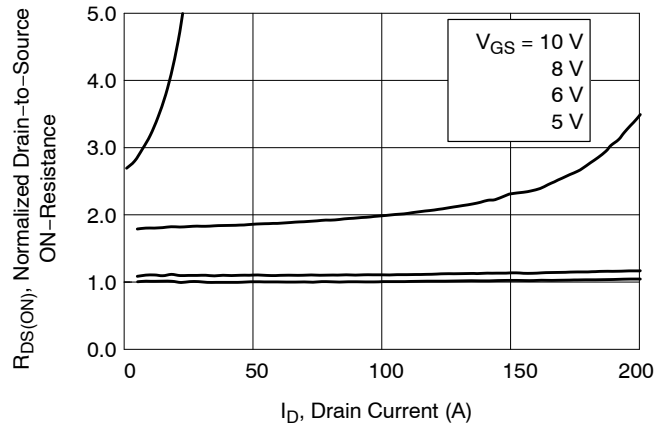


Figure 4. Normalized On-Resistance vs. Drain Current and Gate Voltage

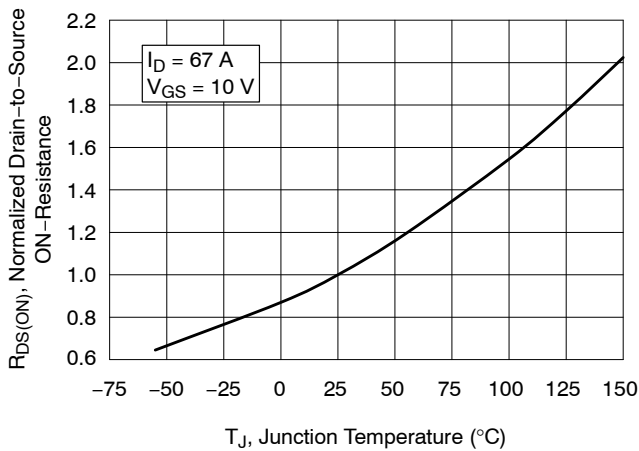


Figure 5. Normalized On-Resistance Variation with Temperature

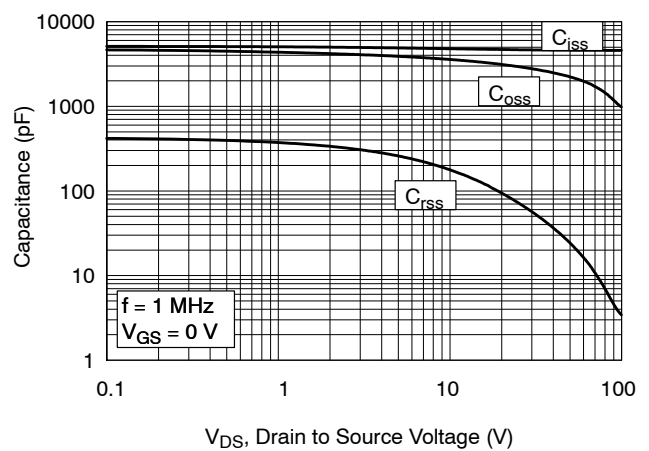


Figure 6. Capacitance Variation

TYPICAL CHARACTERISTICS (continued)

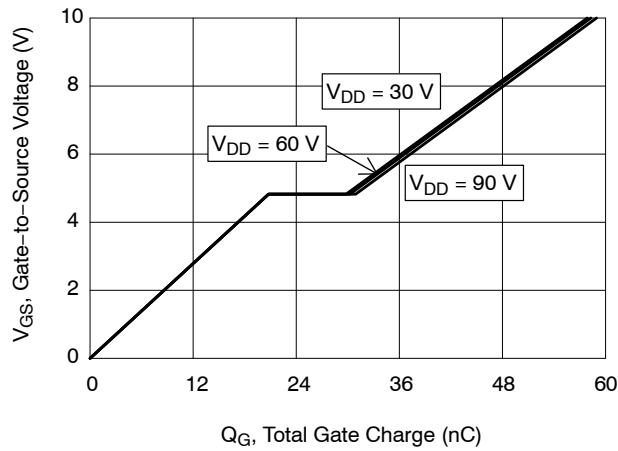


Figure 7. Gate-to-Source Voltage vs. Total Charge

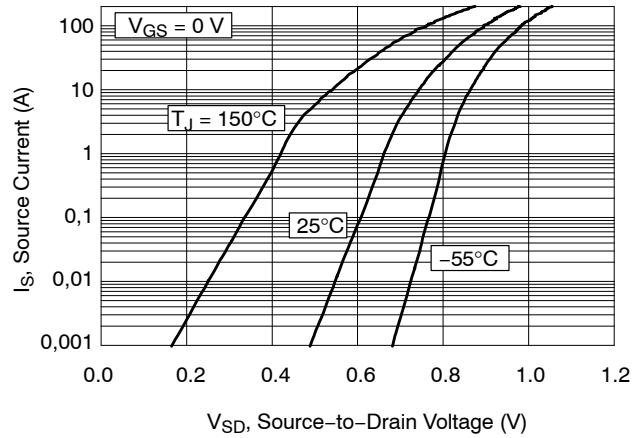


Figure 8. Diode Forward Voltage vs. Current

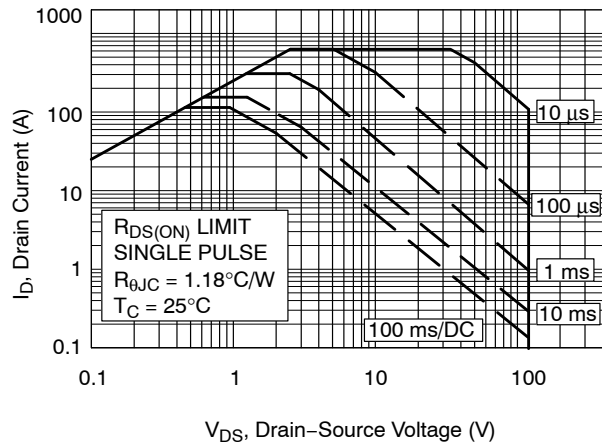


Figure 9. Safe Operating Area

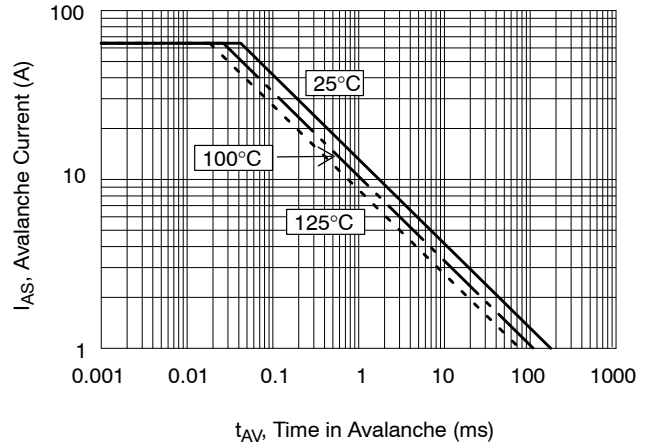


Figure 10. I_{PEAK} vs. Time in Avalanche

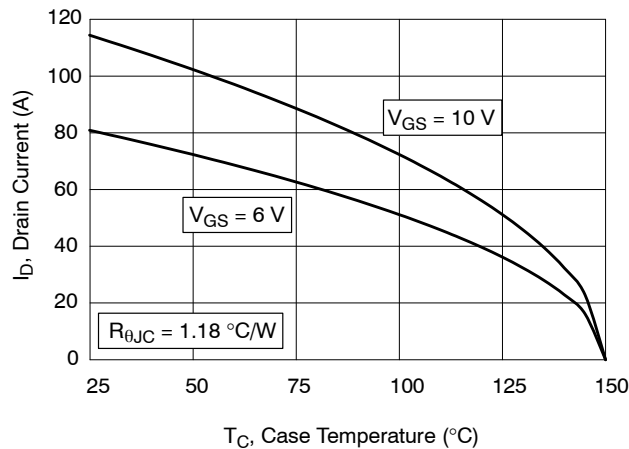


Figure 11. Maximum Drain Current vs. Case Temperature

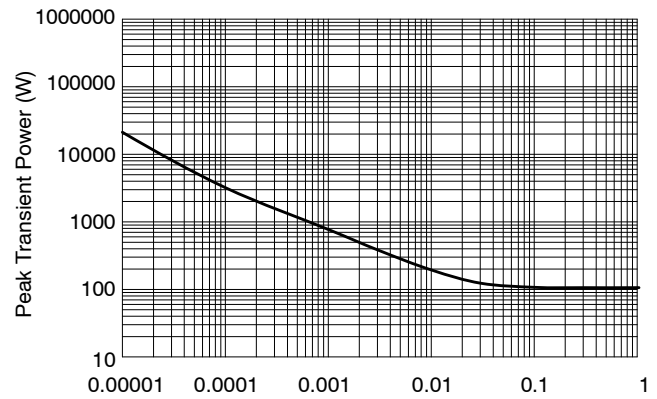


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

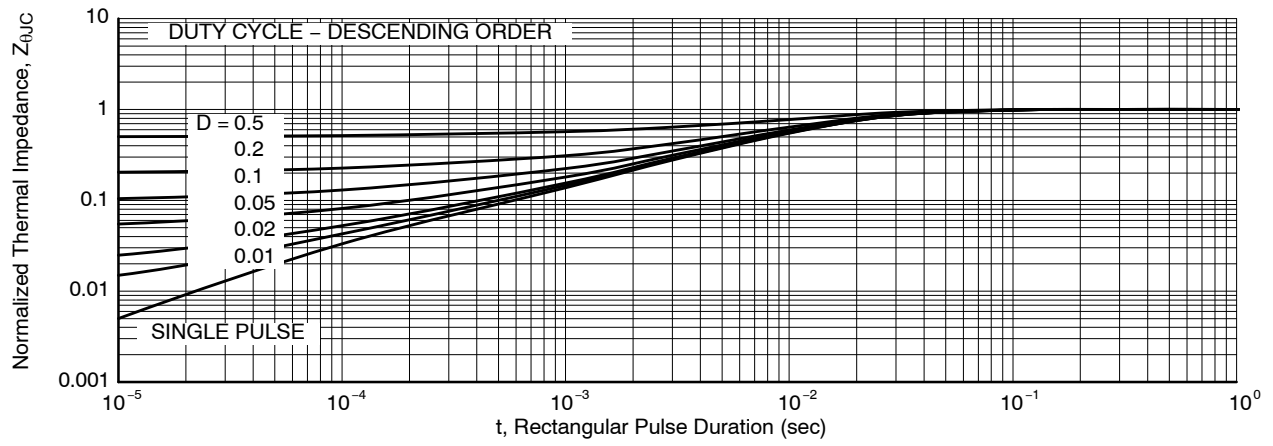
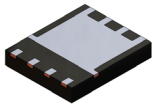


Figure 13. Transient Thermal Response Curve

MECHANICAL CASE OUTLINE

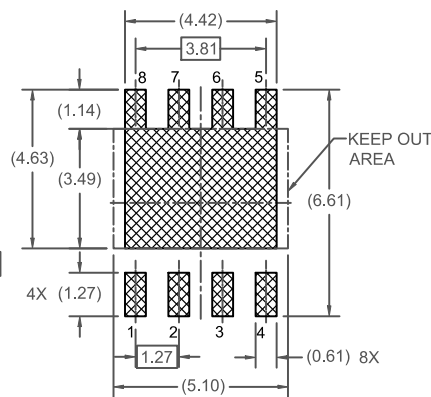
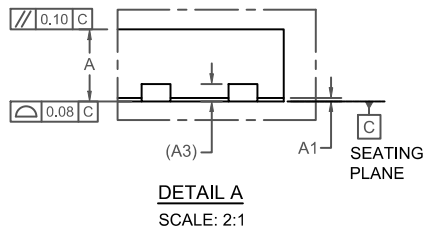
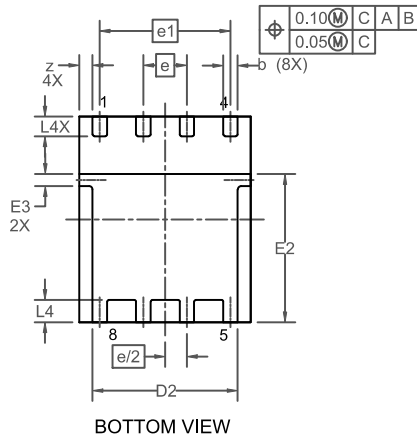
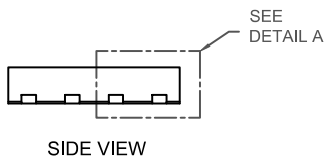
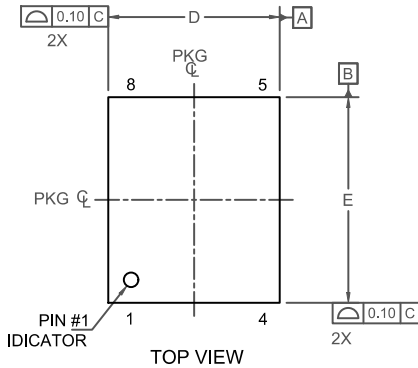
PACKAGE DIMENSIONS

ON Semiconductor®



PQFN8 5X6, 1.27P
CASE 483AF
ISSUE A

DATE 06 JUL 2021



LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

NOTES: UNLESS OTHERWISE SPECIFIED

- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
A3	0.20 REF.		
b	0.37	0.42	0.47
D	4.90	5.00	5.10
D2	4.13	4.23	4.33
E	5.90	6.00	6.10
E2	4.23	4.33	4.43
E3	0.35 REF.		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
L	0.52	0.57	0.62
L4	0.55	0.65	0.75
z	0.38 REF		

DOCUMENT NUMBER: 98AON13656G

Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.

DESCRIPTION: PQFN8 5X6, 1.27P

PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative