

MC74LVX4053

Analog Multiplexer/ Demultiplexer High-Performance Silicon-Gate CMOS

The MC74LVX4053 utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. This analog multiplexer/demultiplexer controls analog voltages that may vary across the complete power supply range (from V_{CC} to V_{EE}).

The LVX4053 is similar in pinout to the LVX8053, the HC4053A, and the metal-gate MC14053B. The Channel-Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

The Channel-Select and Enable inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device has been designed so the ON resistance (R_{ON}) is more linear over input voltage than the R_{ON} of metal-gate CMOS analog switches and High-Speed CMOS analog switches.

Features

- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Analog Power Supply Range ($V_{CC} - V_{EE}$) = -3.0 V to $+3.0\text{ V}$
- Digital (Control) Power Supply Range ($V_{CC} - GND$) = 2.5 to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal-Gate, HSL, or VHC Counterparts
- Low Noise
- Designed to Operate on a Single Supply with $V_{EE} = GND$, or Using Split Supplies up to $\pm 3.0\text{ V}$
- Break-Before-Make Circuitry
- These Devices are Pb-Free and are RoHS Compliant



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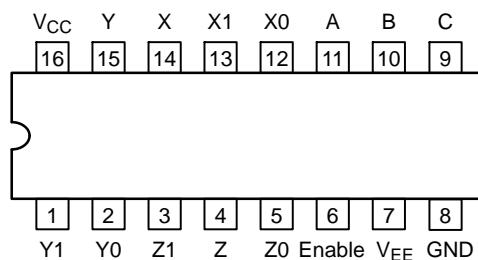


SOIC-16
D SUFFIX
CASE 751B

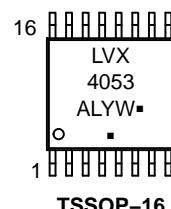
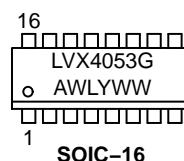


TSSOP-16
DT SUFFIX
CASE 948F

PIN ASSIGNMENT



MARKING DIAGRAMS



LVX4053 = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

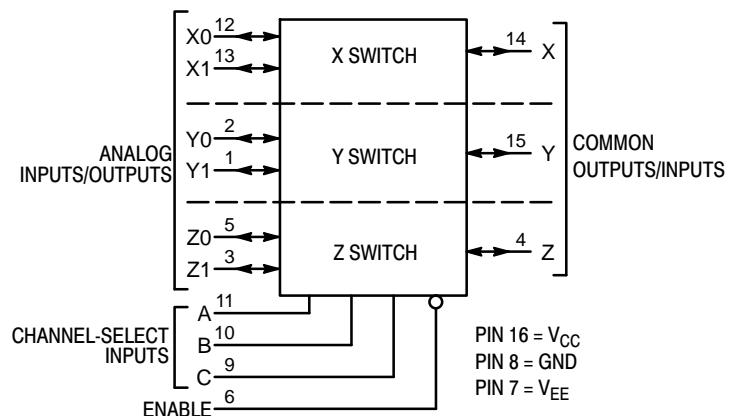
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

MC74LVX4053

FUNCTION TABLE				
Control Inputs			ON Channels	
Enable	C	B	A	
L	L	L	L	Z0 Y0 X0
L	L	L	H	Z0 Y0 X1
L	L	H	L	Z0 Y1 X0
L	L	H	H	Z0 Y1 X1
L	H	L	L	Z1 Y0 X0
L	H	L	H	Z1 Y0 X1
L	H	H	L	Z1 Y1 X0
L	H	H	H	Z1 Y1 X1
H	X	X	X	NONE

X = Don't Care



NOTE: This device allows independent control of each switch.
Channel-Select Input A controls the X-Switch, Input B controls the Y-Switch and Input C controls the Z-Switch

Figure 1. Logic Diagram Triple Single-Pole, Double-Position Plus Common Off

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{EE}	Negative DC Supply Voltage (Referenced to GND)	-7.0 to +0.5	V
V _{CC}	Positive DC Supply Voltage (Referenced to GND) (Referenced to V _{EE})	-0.5 to +7.0 -0.5 to +7.0	V
V _{IS}	Analog Input Voltage	V _{EE} - 0.5 to V _{CC} + 0.5	V
V _{IN}	Digital Input Voltage (Referenced to GND)	-0.5 to 7.0	V
I	DC Current, Into or Out of Any Pin	±20	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction Temperature under Bias	+150	°C
θ _{JA}	Thermal Resistance SOIC TSSOP	143 164	°C/W
P _D	Power Dissipation in Still Air, SOIC TSSOP	500 450	mW
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Index: 30% – 35%	UL-94-VO (0.125 in)	
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	> 2000 > 200 > 1000	V
I _{LATCHUP}	Latchup Performance Above V _{CC} and Below GND at 125°C (Note 4)	±300	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22-A114-A.
2. Tested to EIA/JESD22-A115-A.
3. Tested to JESD22-C101-A.
4. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V_{EE}	Negative DC Supply Voltage (Referenced to GND)	-6.0	GND	V	
V_{CC}	Positive DC Supply Voltage (Referenced to GND) (Referenced to V_{EE})	2.5 2.5	6.0 6.0	V	
V_{IS}	Analog Input Voltage	V_{EE}	V_{CC}	V	
V_{IN}	Digital Input Voltage (Note 5) (Referenced to GND)	0	6.0	V	
T_A	Operating Temperature Range, All Package Types	-55	125	°C	
t_r, t_f	Input Rise/Fall Time (Channel Select or Enable Inputs)	$V_{CC} = 3.0 \text{ V} \pm 0.3 \text{ V}$ $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	0 0	100 20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Unused inputs may not be left open. All inputs must be tied to a high-logic voltage level or a low-logic input voltage level.

DEVICE JUNCTION TEMPERATURE VERSUS
TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

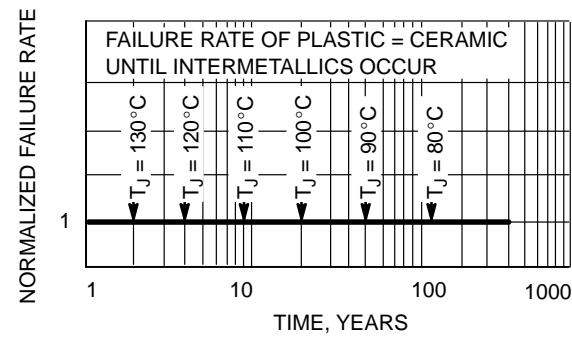


Figure 2. Failure Rate vs. Time Junction Temperature

DC CHARACTERISTICS – Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				-55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High-Level Input Voltage, Channel-Select or Enable Inputs		2.5 3.0 4.5 6.0	1.90 2.10 3.15 4.2	1.90 2.10 3.15 4.2	1.90 2.10 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage, Channel-Select or Enable Inputs		2.5 3.0 4.5 6.0	0.6 0.9 1.35 1.8	0.6 0.9 1.35 1.8	0.6 0.9 1.35 1.8	V
I_{IN}	Maximum Input Leakage Current, Channel-Select or Enable Inputs	$V_{IN} = 6.0 \text{ or GND}$	0 V to 6.0 V	±0.1	±1.0	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select, Enable and $V_{IS} = V_{CC}$ or GND	6.0	4.0	40	80	µA

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DC ELECTRICAL CHARACTERISTICS – Analog Section

Symbol	Parameter	Test Conditions	V _{CC} V	V _{EE} V	Guaranteed Limit			Unit
					–55 to 25°C	≤ 85°C	≤ 125°C	
R _{ON}	Maximum “ON” Resistance	V _{IN} = V _{IL} or V _{IH} V _{IS} = 1/2 (V _{CC} – V _{EE}) I _S = 2.0 mA (Figure 3)	3.0 4.5 3.0	0 0 –3.0	86 37 26	108 46 33	120 55 37	Ω
ΔR _{ON}	Maximum Difference in “ON” Resistance Between Any Two Channels in the Same Package	V _{IN} = V _{IL} or V _{IH} V _{IS} = 1/2 (V _{CC} – V _{EE}) I _S = 2.0 mA	3.0 4.5 3.0	0 0 –3.0	15 13 10	20 18 15	20 18 15	Ω
I _{off}	Maximum Off-Channel Leakage Current, Any One Channel	V _{in} = V _{IL} or V _{IH} ; V _{IO} = V _{CC} or GND; Switch Off (Figure 3)	5.5 +3.0	0 –3.0	0.1 0.1	0.5 0.5	1.0 1.0	μA
	Maximum Off-Channel Leakage Current, Common Channel	V _{in} = V _{IL} or V _{IH} ; V _{IO} = V _{CC} or GND; Switch Off (Figure 4)	5.5 +3.0	0 –3.0	0.2 0.2	2.0 2.0	4.0 4.0	
I _{on}	Maximum On-Channel Leakage Current, Channel-to-Channel	V _{in} = V _{IL} or V _{IH} ; Switch-to-Switch = V _{CC} or GND; (Figure 5)	5.5 +3.0	0 –3.0	0.2 0.2	2.0 2.0	4.0 4.0	μA

AC CHARACTERISTICS (Input t_r = t_f = 3 ns)

Symbol	Parameter	Test Conditions	V _{CC} V	V _{EE} V	Guaranteed Limit			Unit	
					–55 to 25°C		≤ 85°C	≤ 125°C	
					Min	Typ*			
t _{BBM}	Min. Break-Before-Make Time	V _{IN} = V _{IL} or V _{IH} V _{IS} = V _{CC} R _L = 300 Ω, C _L = 35 pF (Figures 11 and 12)	3.0 4.5 3.0	0.0 0.0 –3.0	1.0 1.0 1.0	6.5 5.0 3.5	– – –	– – –	ns

*Typical Characteristics are at 25°C.

AC CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 3 ns)

Symbol	Parameter	V _{CC} V	V _{EE} V	Guaranteed Limit						Unit	
				–55 to 25°C			≤ 85°C		≤ 125°C		
				Min	Typ	Max	Min	Max	Min		
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Channel-Select to Analog Output (Figures 15 and 16)	2.5 3.0 4.5 3.0	0 0 0 –3.0			40 28 23 23		45 30 25 25		50 35 30 28	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Enable to Analog Output (Figures 13 and 14)	2.5 3.0 4.5 3.0	0 0 0 –3.0			40 28 23 23		45 30 25 25		50 35 30 28	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Enable to Analog Output (Figures 13 and 14)	2.5 3.0 4.5 3.0	0 0 0 –3.0			40 28 23 23		45 30 25 25		50 35 30 28	ns
C _{PD}	Power Dissipation Capacitance (Figure 17) (Note 6)				Typical @ 25°C, V _{CC} = 5.0 V, V _{EE} = 0 V						pF
					45						
C _{IN}	Maximum Input Capacitance, Channel-Select or Enable Inputs				10						pF
C _{I/O}	Maximum Capacitance Analog I/O Common O/I Feedthrough				10 10 1.0						pF

6. Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}.

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Condition	V _{CC} V	V _{EE} V	Typ		Unit
					25°C		
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response	V _{IS} = 1/2 (V _{CC} – V _{EE}) Ref and Test Attn = 10 dB Source Amplitude = 0 dB (Figure 6)	3.0 4.5 6.0 3.0	0.0 0.0 0.0 –3.0	80 80 80 80		MHz
V _{ISO}	Off-Channel Feedthrough Isolation	f = 1 MHz; V _{IS} = 1/2 (V _{CC} – V _{EE}) Adjust Network Analyzer output to 10 dBm on each output from the power splitter (Figures 7 and 8)	3.0 4.5 6.0 3.0	0.0 0.0 0.0 –3.0	–70 –70 –70 –70		dB
V _{ONL}	Maximum Feedthrough On Loss	V _{IS} = 1/2 (V _{CC} – V _{EE}) Adjust Network Analyzer output to 10 dBm on each output from the power splitter (Figure 10)	3.0 4.5 6.0 3.0	0.0 0.0 0.0 –3.0	–2 –2 –2 –2		dB
Q	Charge Injection	V _{IN} = V _{CC} to V _{EE} , f _{IS} = 1 kHz, t _r = t _f = 3 ns R _{IS} = 0 Ω, C _L = 1000 pF, Q = C _L * ΔV _{OUT} (Figure 9)	5.0 3.0	0.0 –3.0	9.0 12		pC
THD	Total Harmonic Distortion THD + Noise	f _{IS} = 1 MHz, R _L = 10 KΩ, C _L = 50 pF, V _{IS} = 5.0 V _{PP} sine wave V _{IS} = 6.0 V _{PP} sine wave (Figure 18)	6.0 3.0	0.0 –3.0	0.10 0.05		%

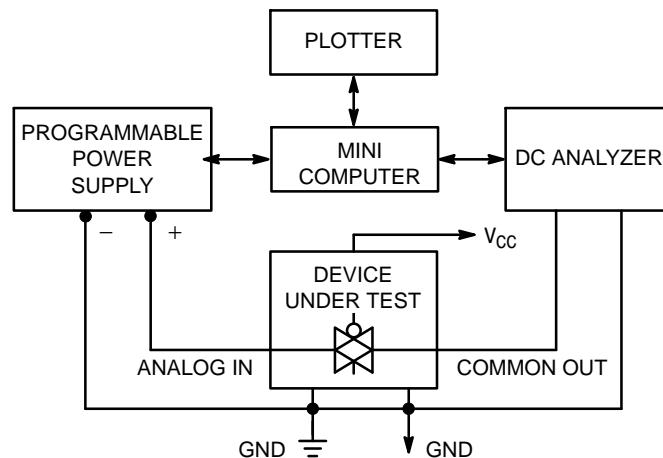


Figure 3. On Resistance, Test Set-Up

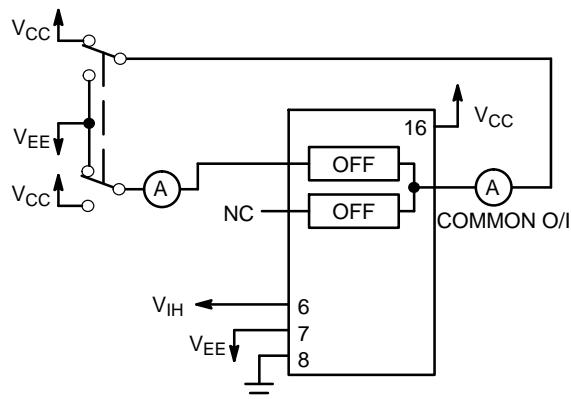


Figure 4. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

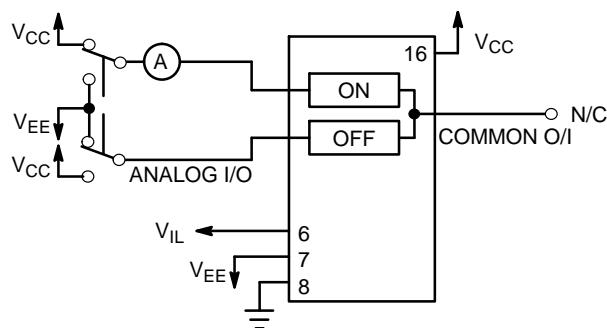


Figure 5. Maximum On Channel Leakage Current, Channel to Channel, Test Set-Up

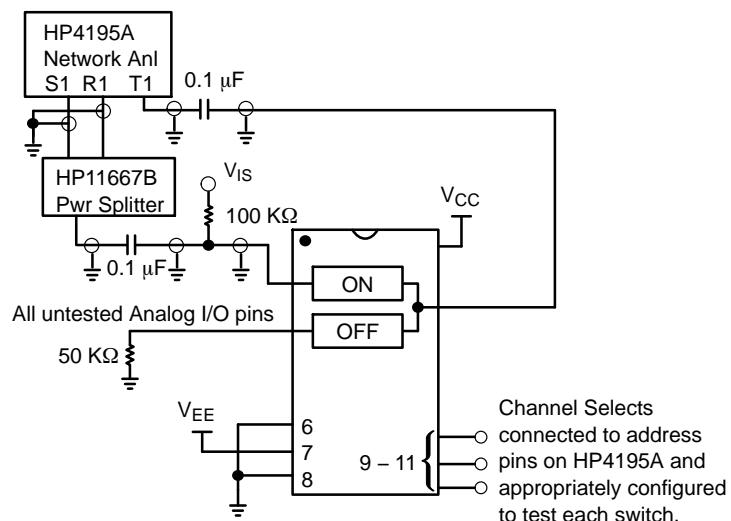
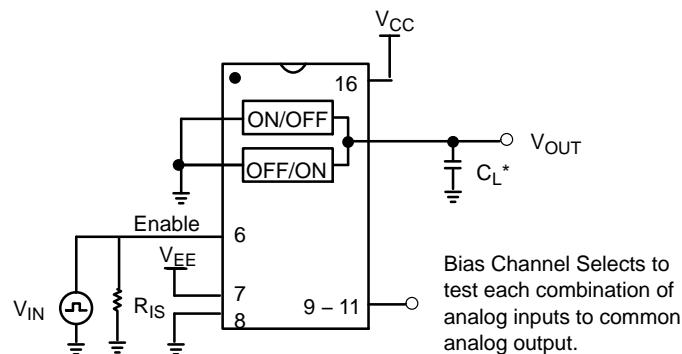


Figure 6. Maximum On Channel Bandwidth, Test Set-Up

MC74LVX4053



*Includes all probe and jig capacitance.

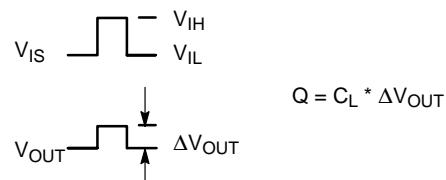


Figure 9. Charge Injection, Test Set-Up

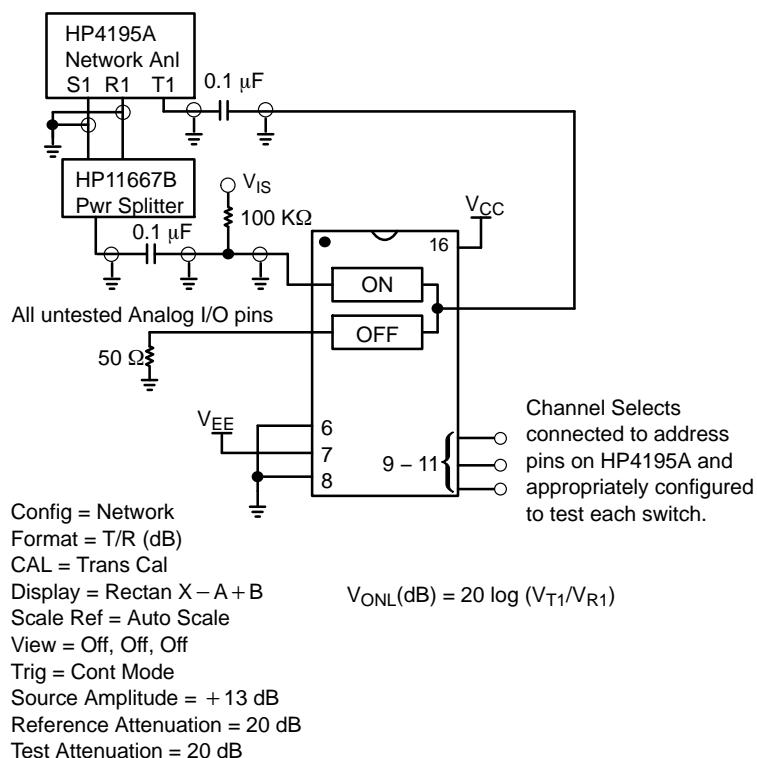


Figure 10. Maximum On Channel Feedthrough On Loss, Test Set-Up

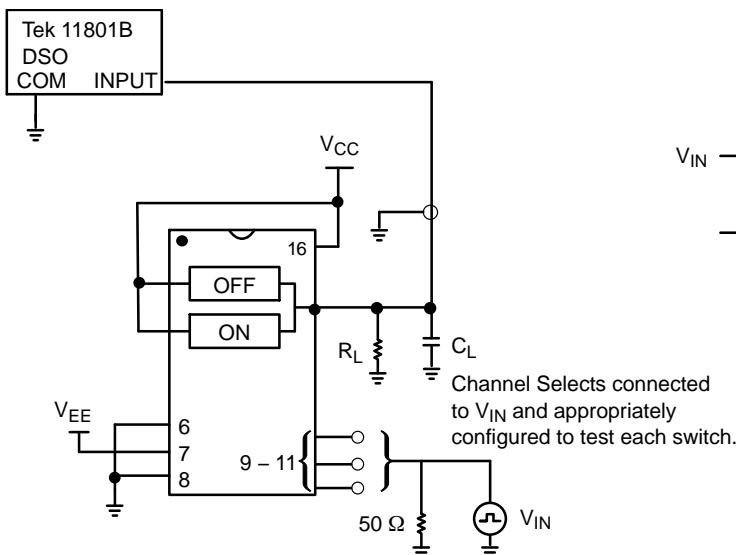


Figure 11. Break-Before-Make, Test Set-Up

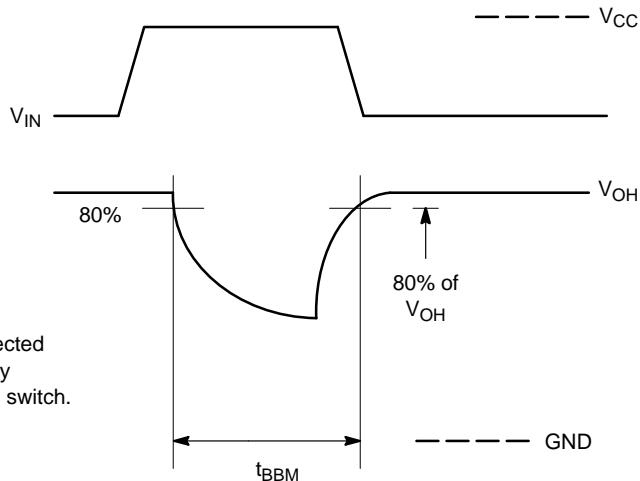


Figure 12. Break-Before-Make Time

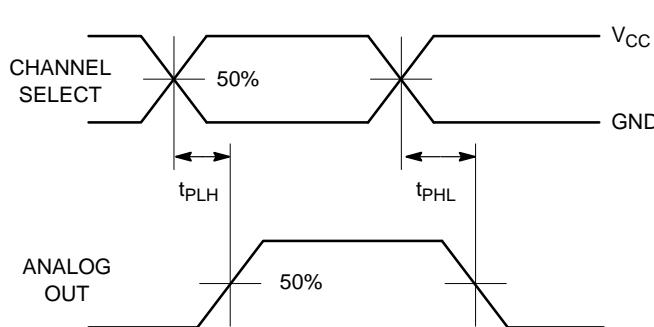
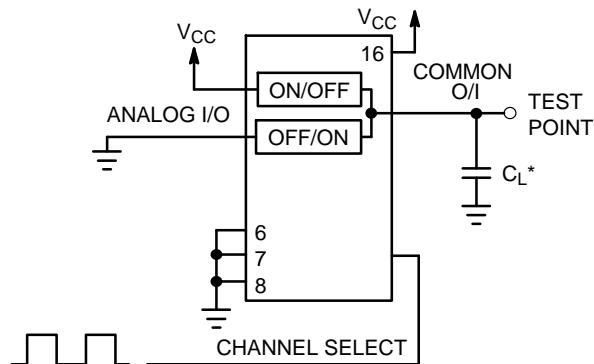


Figure 13. Propagation Delays, Channel Select to Analog Out



*Includes all probe and jig capacitance.

**Figure 14. Propagation Delay, Test Set-Up
Channel Select to Analog Out**

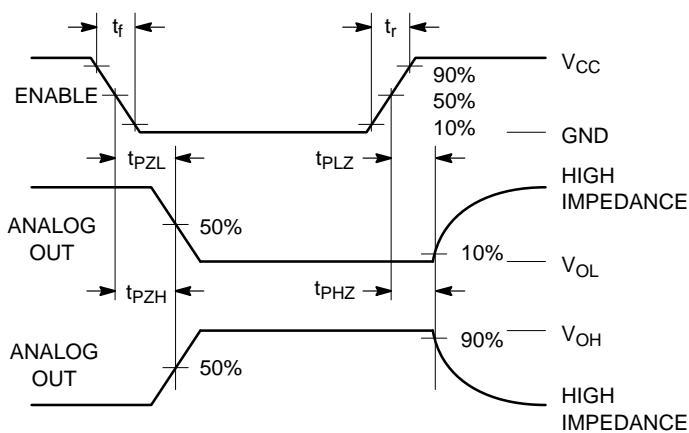
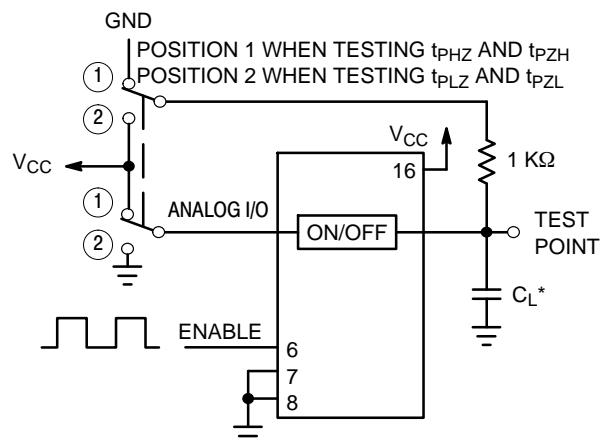


Figure 15. Propagation Delays, Enable to Analog Out



**Figure 16. Propagation Delay, Test Set-Up
Enable to Analog Out**

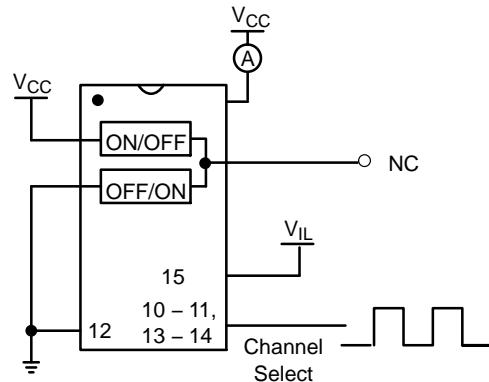


Figure 17. Power Dissipation Capacitance, Test Set-Up

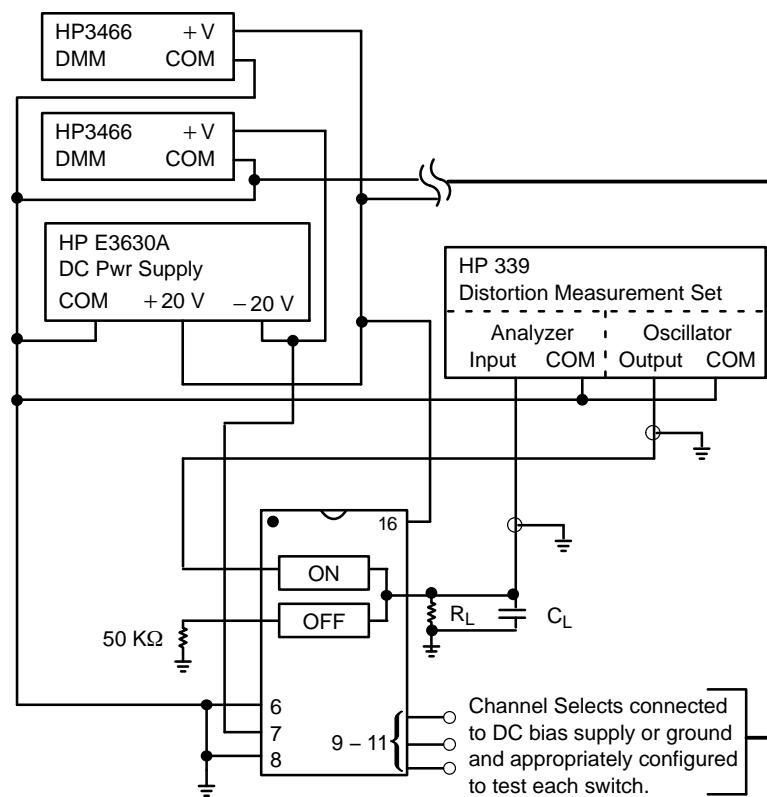


Figure 18. Total Harmonic Distortion, Test Set-Up

APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at V_{CC} or GND logic levels. V_{CC} being recognized as a logic high and GND being recognized as a logic low. In this example:

$$\begin{aligned} V_{CC} &= +5 \text{ V} = \text{logic high} \\ \text{GND} &= 0 \text{ V} = \text{logic low} \end{aligned}$$

The maximum analog voltage swing is determined by the supply voltages V_{CC} and V_{EE}. The positive peak analog voltage should not exceed V_{CC}. Similarly, the negative peak analog voltage should not go below V_{EE}. In this example, the difference between V_{CC} and V_{EE} is 5.0 volts. Therefore, using the configuration of Figure 20, a maximum analog signal of 5.0 volts peak-to-peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and

outputs to V_{CC} or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

$$\begin{aligned} V_{EE} - \text{GND} &= 0 \text{ to } -6 \text{ volts} \\ V_{CC} - \text{GND} &= 2.5 \text{ to } 6 \text{ volts} \\ V_{CC} - V_{EE} &= 2.5 \text{ to } 6 \text{ volts} \\ \text{and } V_{EE} &\leq \text{GND} \end{aligned}$$

When voltage transients above V_{CC} and/or below V_{EE} are anticipated on the analog channels, external Germanium or Schottky diodes (D_x) are recommended as shown in Figure 21. These diodes should be able to absorb the maximum anticipated current surges during clipping.

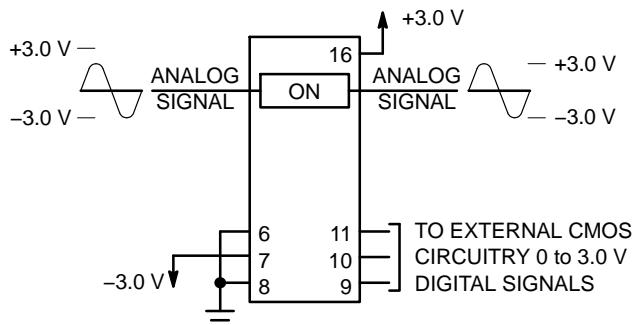


Figure 19. Application Example

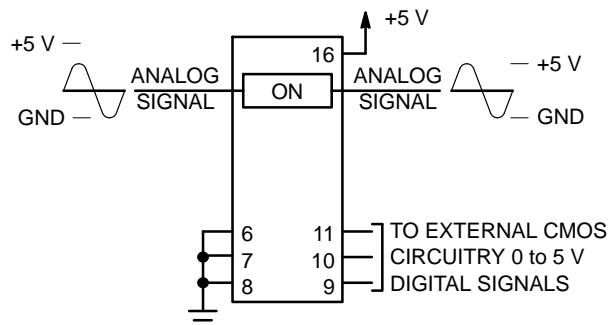


Figure 20. Application Example

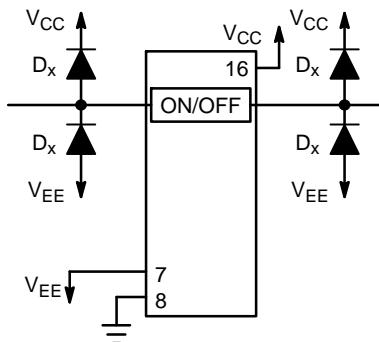


Figure 21. External Germanium or Schottky Clipping Diodes

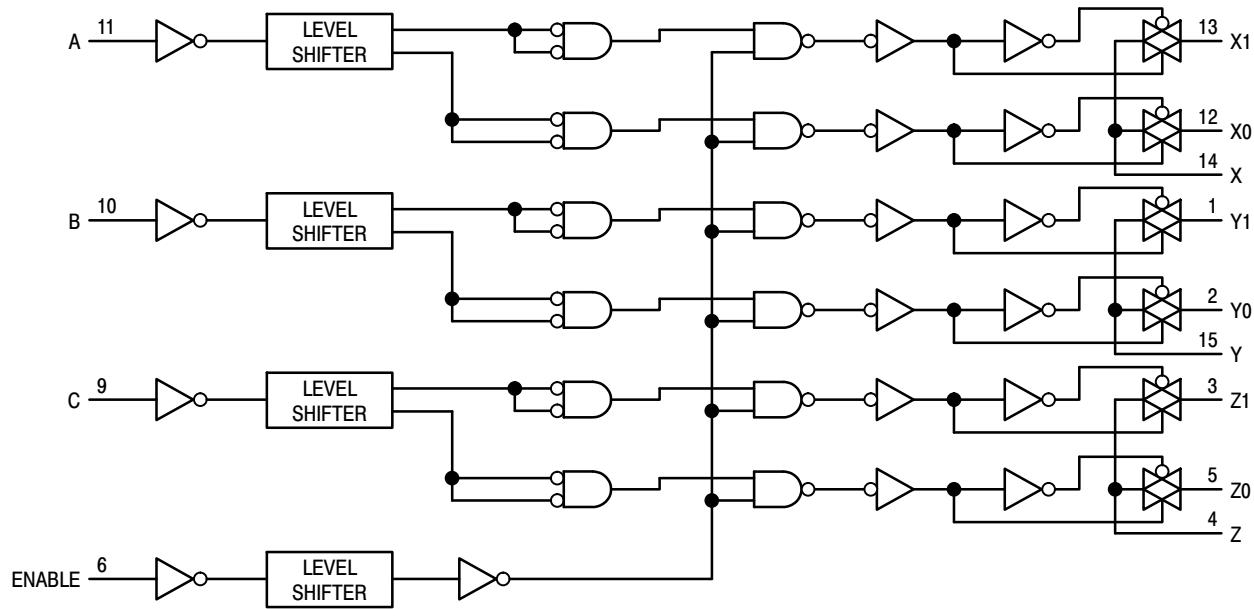


Figure 22. Function Diagram, LVX4053

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74LVX4053DG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74LVX4053DR2G	SOIC-16 (Pb-Free)	2500 Tape & Reel
MC74LVX4053DTG	TSSOP-16 (Pb-Free)	96 Units / Rail
MC74LVX4053DTR2G	TSSOP-16 (Pb-Free)	2500 Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

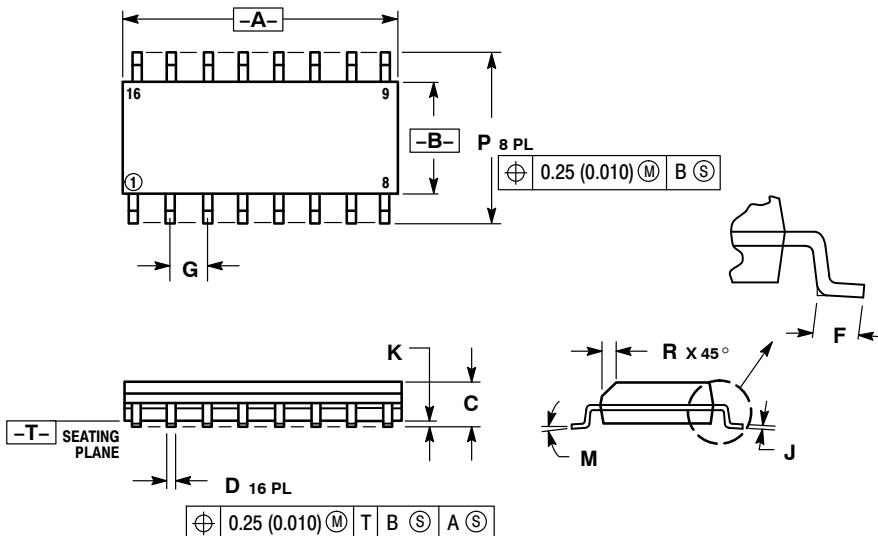
ON Semiconductor®



SCALE 1:1

SOIC-16
CASE 751B-05
ISSUE K

DATE 29 DEC 2006



NOTES:

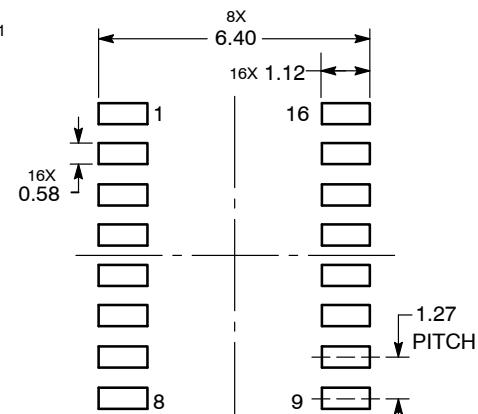
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27	BSC	0.050	BSC
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 1:	STYLE 2:	STYLE 3:	STYLE 4:
PIN 1. COLLECTOR	PIN 1. CATHODE	PIN 1. COLLECTOR, DYE #1	PIN 1. COLLECTOR, DYE #1
2. BASE	2. ANODE	2. BASE, #1	2. COLLECTOR, #1
3. Emitter	3. NO CONNECTION	3. Emitter, #1	3. COLLECTOR, #2
4. NO CONNECTION	4. CATHODE	4. COLLECTOR, #1	4. COLLECTOR, #2
5. Emitter	5. CATHODE	5. COLLECTOR, #2	5. COLLECTOR, #3
6. BASE	6. NO CONNECTION	6. BASE, #2	6. COLLECTOR, #3
7. COLLECTOR	7. ANODE	7. Emitter, #2	7. COLLECTOR, #4
8. COLLECTOR	8. CATHODE	8. COLLECTOR, #2	8. COLLECTOR, #4
9. BASE	9. CATHODE	9. COLLECTOR, #3	9. BASE, #4
10. Emitter	10. ANODE	10. BASE, #3	10. Emitter, #4
11. NO CONNECTION	11. NO CONNECTION	11. Emitter, #3	11. BASE, #3
12. Emitter	12. CATHODE	12. COLLECTOR, #3	12. Emitter, #3
13. BASE	13. CATHODE	13. COLLECTOR, #4	13. BASE, #2
14. COLLECTOR	14. NO CONNECTION	14. BASE, #4	14. Emitter, #2
15. Emitter	15. ANODE	15. Emitter, #4	15. BASE, #1
16. COLLECTOR	16. CATHODE	16. COLLECTOR, #4	16. Emitter, #1

STYLE 5:	STYLE 6:	STYLE 7:
PIN 1. DRAIN, DYE #1	PIN 1. CATHODE	PIN 1. SOURCE N-CH
2. DRAIN, #1	2. CATHODE	2. COMMON DRAIN (OUTPUT)
3. DRAIN, #2	3. CATHODE	3. COMMON DRAIN (OUTPUT)
4. DRAIN, #2	4. CATHODE	4. GATE P-CH
5. DRAIN, #3	5. CATHODE	5. COMMON DRAIN (OUTPUT)
6. DRAIN, #3	6. CATHODE	6. COMMON DRAIN (OUTPUT)
7. DRAIN, #4	7. CATHODE	7. COMMON DRAIN (OUTPUT)
8. DRAIN, #4	8. CATHODE	8. SOURCE P-CH
9. GATE, #4	9. ANODE	9. SOURCE P-CH
10. SOURCE, #4	10. ANODE	10. COMMON DRAIN (OUTPUT)
11. GATE, #3	11. ANODE	11. COMMON DRAIN (OUTPUT)
12. SOURCE, #3	12. ANODE	12. COMMON DRAIN (OUTPUT)
13. GATE, #2	13. ANODE	13. GATE N-CH
14. SOURCE, #2	14. ANODE	14. COMMON DRAIN (OUTPUT)
15. GATE, #1	15. ANODE	15. COMMON DRAIN (OUTPUT)
16. SOURCE, #1	16. ANODE	16. SOURCE N-CH

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

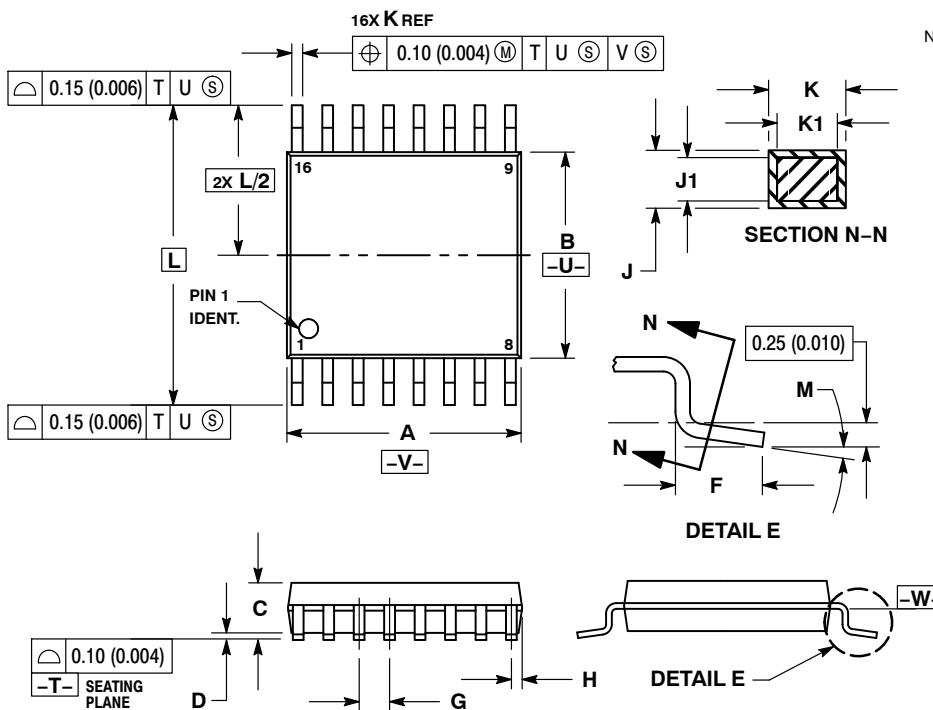
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1
SCALE 2:1

TSSOP-16
CASE 948F-01
ISSUE B

DATE 19 OCT 2006

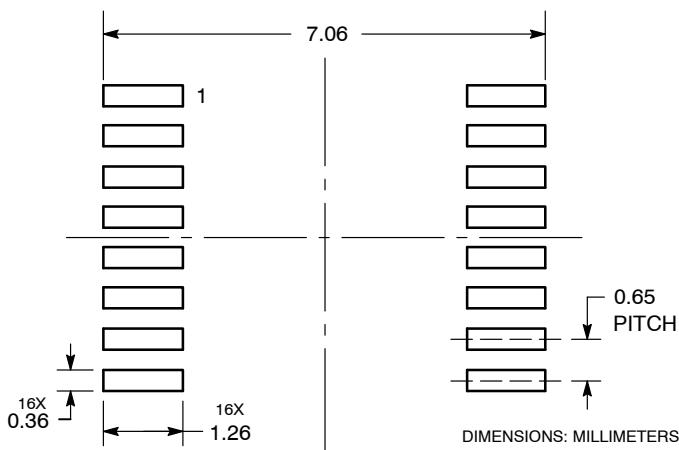


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT

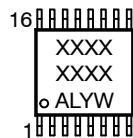


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DESCRIPTION: TSSOP-16

PAGE 1 OF 1

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

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