

# MOSFET – N-Channel, POWERTRENCH® 150 V, 169 A, 6.3 mΩ

## FDBL86210-F085

### Features

- Typical  $r_{DS(on)} = 5 \text{ mΩ}$  at  $V_{GS} = 10 \text{ V}$ ,  $I_D = 80 \text{ A}$
- Typical  $Q_{g(\text{tot})} = 70 \text{ nC}$  at  $V_{GS} = 10 \text{ V}$ ,  $I_D = 80 \text{ A}$
- UIS Capability
- AEC-Q101 Qualified and PPAP Capable
- This Device is Pb-Free and are RoHS Compliant

### Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Integrated Starter/Alternator
- Primary Switch for 12 V Systems

### MOSFET MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$V_{DSS}$	Drain to Source Voltage	150	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current – Continuous ( $V_{GS} = 10$ ), $T_C = 25^\circ\text{C}$ (Note 1)	169	A
	Pulsed Drain Current, $T_C = 25^\circ\text{C}$	See Figure 4	
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)	502	mJ
$P_D$	Power Dissipation	500	W
	Derate Above $25^\circ\text{C}$	3.3	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to +175	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance Junction to Case	0.3	$^\circ\text{C/W}$
$R_{\theta JA}$	Maximum Thermal Resistance Junction to Ambient (Note 3)	43	$^\circ\text{C/W}$

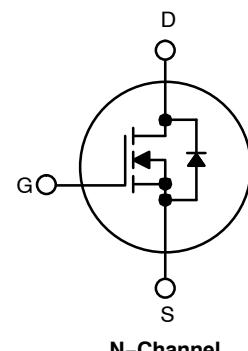
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by silicon.
2. Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.24 \text{ mH}$ ,  $I_{AS} = 64 \text{ A}$ ,  $V_{DD} = 100 \text{ V}$  during inductor charging and  $V_{DD} = 0 \text{ V}$  during time in avalanche.
3.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design, while  $R_{\theta JA}$  is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in<sup>2</sup> pad of 2oz copper.



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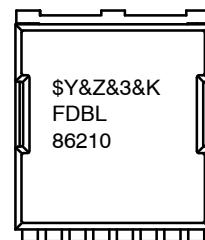


N-Channel



H-PSOF8L  
CASE 100CU

### MARKING DIAGRAM



$\$Y$  = ON Semiconductor Logo  
 $\&Z$  = Assembly Plant Code  
 $\&3$  = Numeric Date Code  
 $\&K$  = Lot Code  
 FDBL86210 = Specific Device Code

### ORDERING INFORMATION

Device	Top Mark	Package	Shipping <sup>†</sup>
FDBL86210-F085	FDBL86210	H-PSOF8L	2000 Units/ Tape&Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# FDBL86210-F085

ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
<b>OFF CHARACTERISTICS</b>							
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V		150	–	–	V
I <sub>DSS</sub>	Drain to Source Leakage Current	V <sub>DS</sub> = 150 V, V <sub>GS</sub> = 0 V	T <sub>J</sub> = 25°C	–	–	1	μA
			T <sub>J</sub> = 175°C (Note 4)	–	–	1	mA
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±20 V		–	–	±100	nA

## ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	2.0	2.8	4.0	V	
r <sub>D(on)</sub>	Drain to Source On Resistance	I <sub>D</sub> = 80 A, V <sub>GS</sub> = 10 V	T <sub>J</sub> = 25°C	–	5	6.3	mΩ
			T <sub>J</sub> = 175°C (Note 4)	–	14	17.5	mΩ

## DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 75 V, V <sub>GS</sub> = 0 V, f = 1 MHz	–	5805	–	pF	
C <sub>oss</sub>	Output Capacitance		–	536	–	pF	
C <sub>rss</sub>	Reverse Transfer Capacitance		–	16	–	pF	
R <sub>g</sub>	Gate Resistance	f = 1 MHz	–	2.2	–	Ω	
Q <sub>g(ToT)</sub>	Total Gate Charge at 10 V	V <sub>GS</sub> = 0 to 10 V	V <sub>DD</sub> = 75 V, I <sub>D</sub> = 80 A	–	70	90	nC
	Threshold Gate Charge	V <sub>GS</sub> = 0 to 2 V		–	10.5	13	nC
Q <sub>gs</sub>	Gate to Source Gate Charge	V <sub>DD</sub> = 75 V, I <sub>D</sub> = 80 A	–	32.5	–	nC	
Q <sub>gd</sub>	Gate to Drain "Miller" Charge		–	10	–	nC	

## SWITCHING CHARACTERISTICS

t <sub>on</sub>	Turn-On Time	V <sub>DD</sub> = 75 V, I <sub>D</sub> = 80 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω	–	–	80	ns
t <sub>d(on)</sub>	Turn-On Delay Time		–	39	–	ns
t <sub>r</sub>	Rise Time		–	30	–	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		–	70	–	ns
t <sub>f</sub>	Fall Time		–	23	–	ns
t <sub>off</sub>	Turn-Off Time		–	–	130	ns

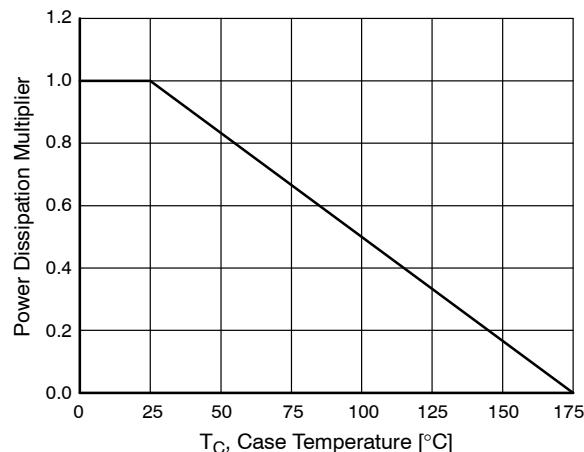
## DRAIN-SOURCE DIODE CHARACTERISTIC

V <sub>SD</sub>	Source to Drain Diode Voltage	I <sub>SD</sub> = 80 A, V <sub>GS</sub> = 0 V	–	–	1.25	V
		I <sub>SD</sub> = 40 A, V <sub>GS</sub> = 0 V	–	–	1.2	V
T <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 80 A, dI <sub>SD</sub> /dt = 100 A/μs, V <sub>DD</sub> = 120 V	–	108	125	ns
			–	323	467	nC

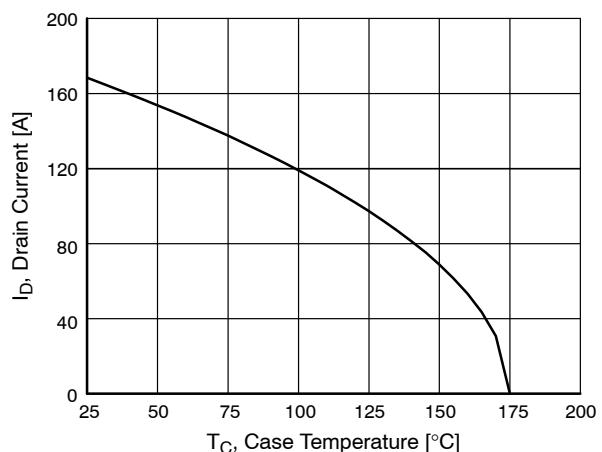
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T<sub>J</sub> = 175°C. Product is not tested to this condition in production.

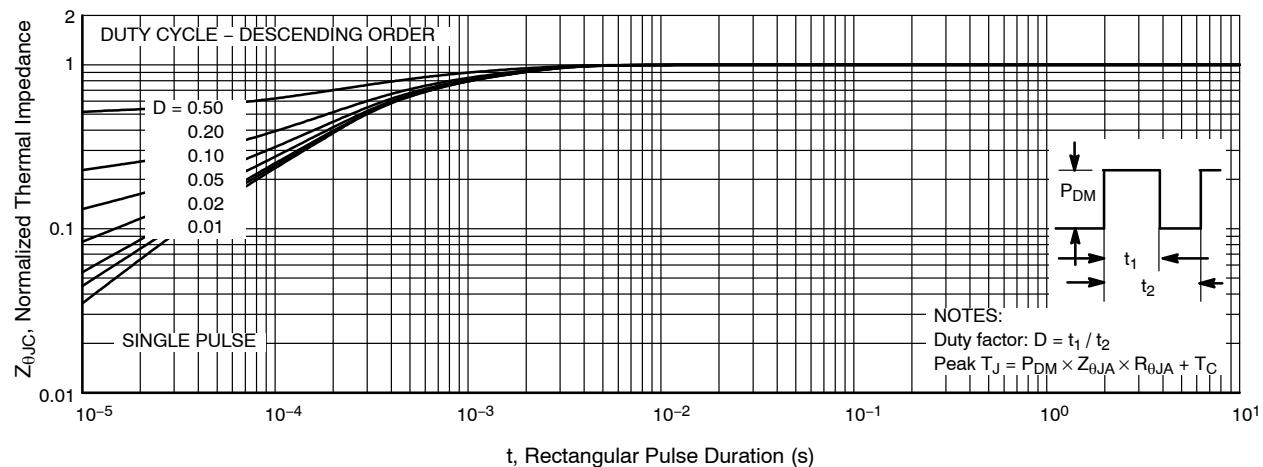
## TYPICAL CHARACTERISTICS



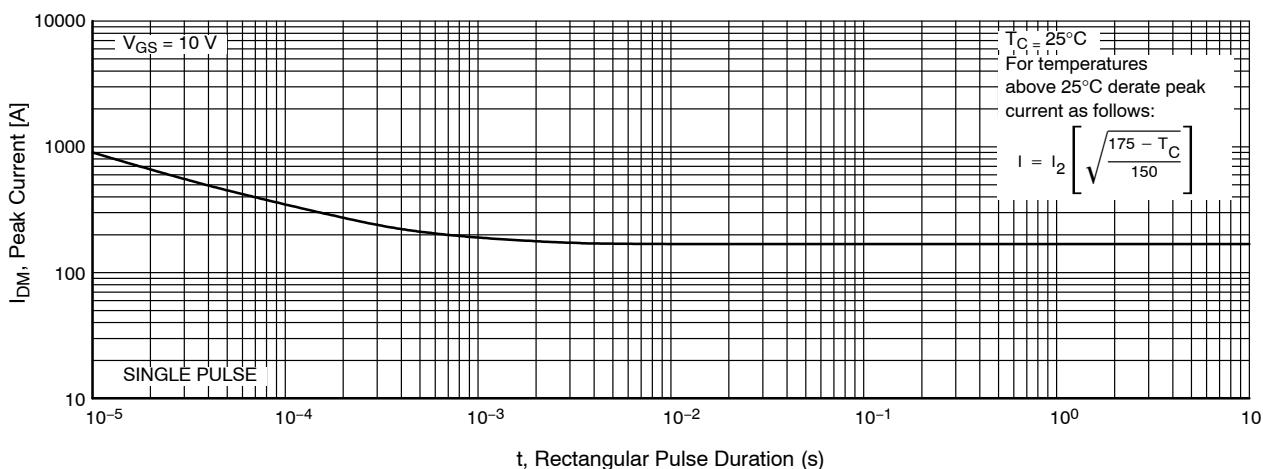
**Figure 1. Normalized Power Dissipation vs. Case Temperature**



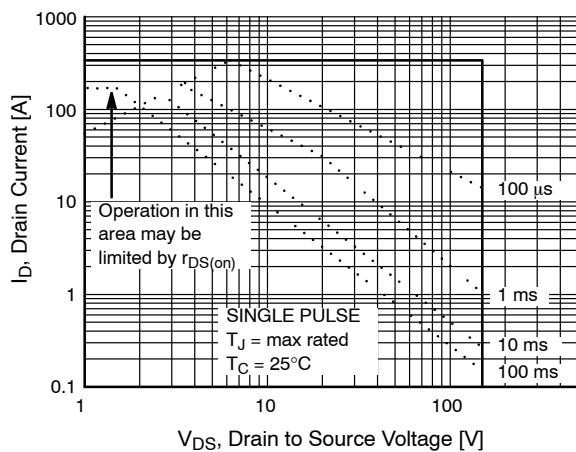
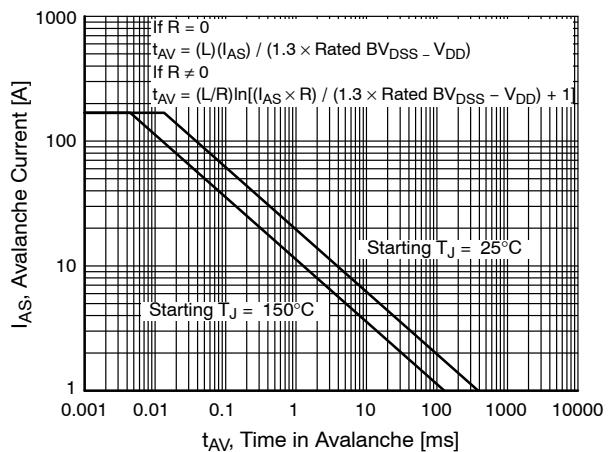
**Figure 2. Maximum Continuous Drain Current vs. Case Temperature**



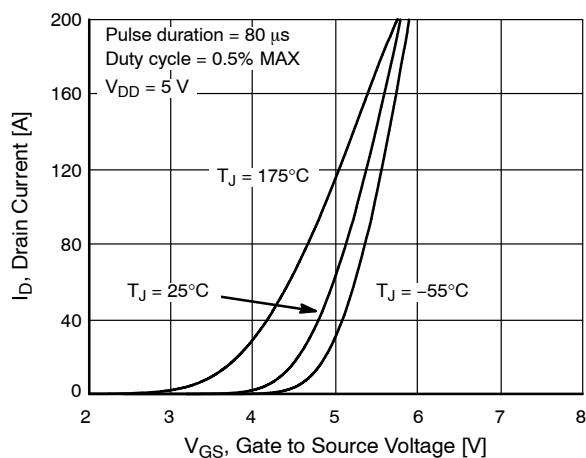
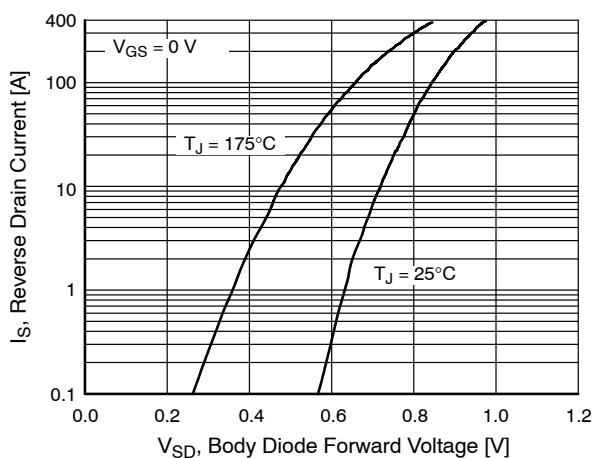
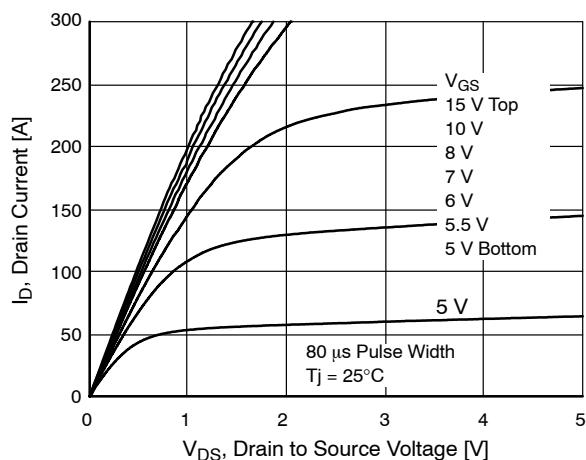
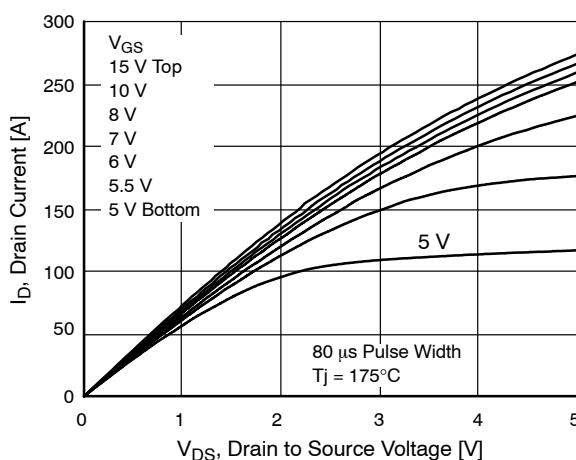
**Figure 3. Normalized Maximum Transient Thermal Impedance**



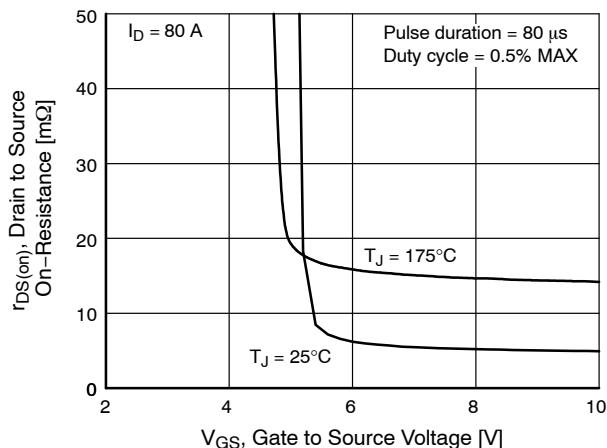
**Figure 4. Peak Current Capability**

**TYPICAL CHARACTERISTICS (continued)**

**Figure 5. Forward Bias Safe Operating Area**


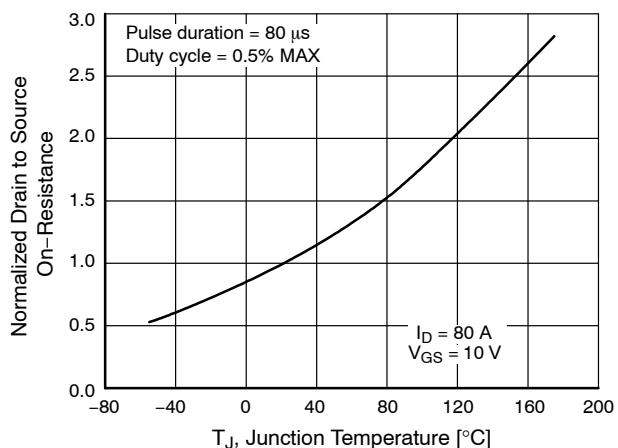
NOTE: Refer to ON Semiconductor Application Notes [AN7514](#) and [AN7515](#).

**Figure 6. Unclamped Inductive Switching Capability**

**Figure 7. Transfer Characteristics**

**Figure 8. Forward Diode Characteristics**

**Figure 9. Saturation Characteristics**

**Figure 10. Saturation Characteristics**

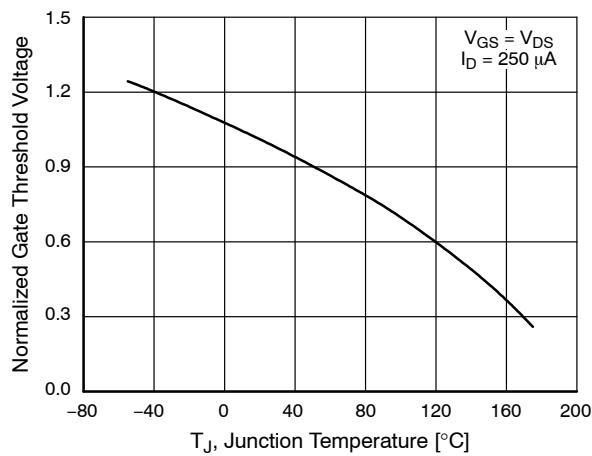
**TYPICAL CHARACTERISTICS (continued)**



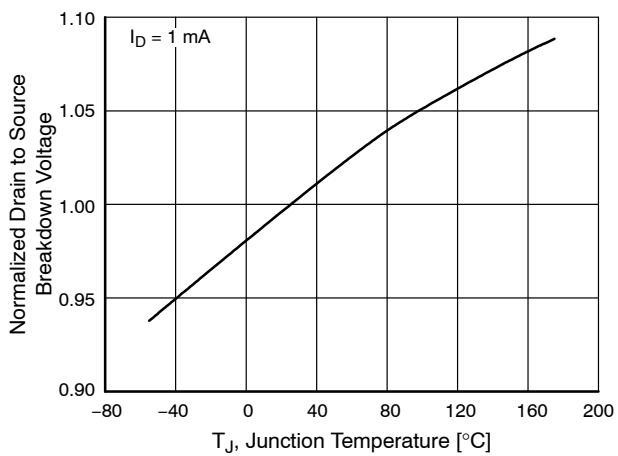
**Figure 11.  $R_{DS(on)}$  vs. Gate Voltage**



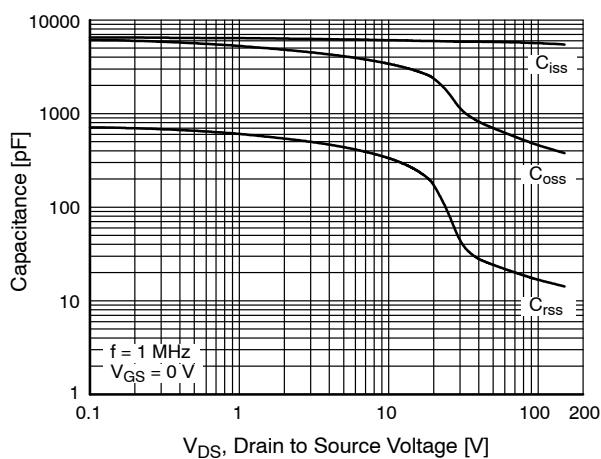
**Figure 12. Normalized  $R_{DS(on)}$  vs. Junction Temperature**



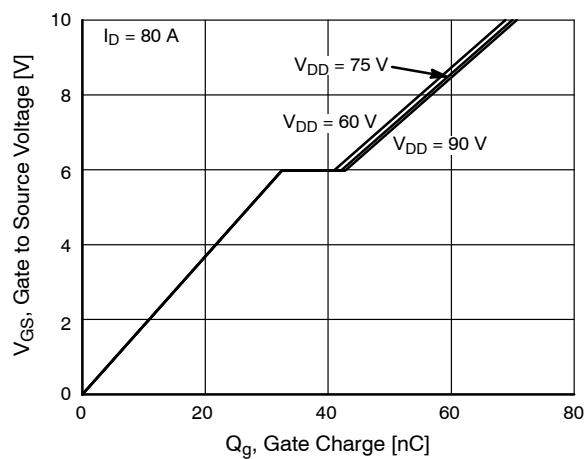
**Figure 13. Normalized Gate Threshold Voltage vs. Temperature**



**Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature**



**Figure 15. Capacitance vs. Drain to Source Voltage**



**Figure 16. Gate Charge vs. Gate to Source Voltage**

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# MECHANICAL CASE OUTLINE

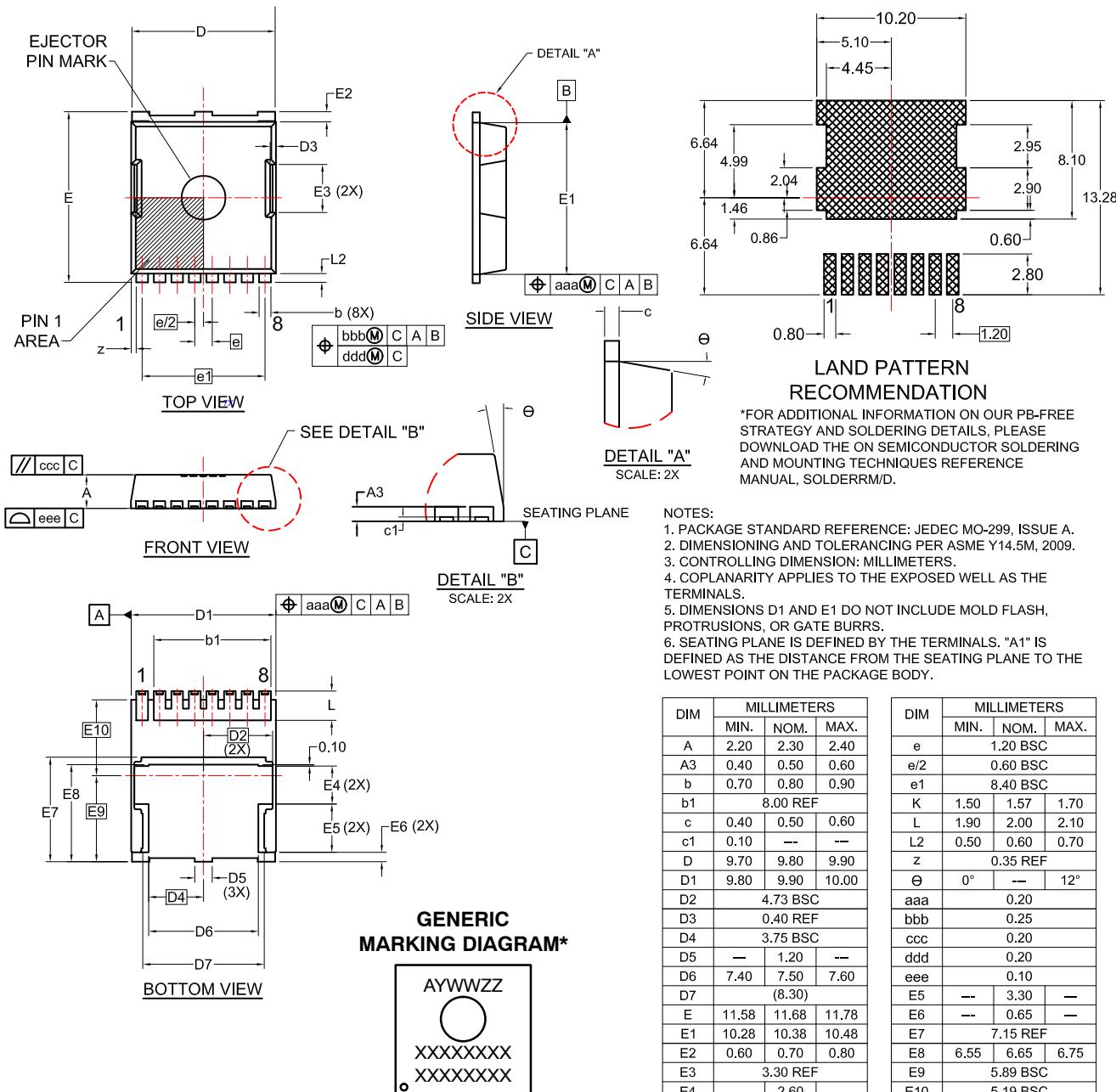
## PACKAGE DIMENSIONS

ON Semiconductor®



**H-PSOF8L 11.68x9.80**  
CASE 100CU  
ISSUE A

DATE 06 JAN 2020



\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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